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16

M16C/65 Group
HARDWARE MANUAL

RENESAS MCU
M16C FAMILY / M16C/60

PRELIMINARY

Hardware Manual

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

HOW TO USE THIS MANUAL

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the M16C/64 Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Technology Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	M16C/65 Group Datasheet	
Hardware manual	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	M16C/65 Group Hardware Manual	This hardware manual
Software manual	Descriptions of CPU instruction set	M16C/60, M16C/20, M16C/Tiny Series Software Manual	REJ09B0137
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Technology Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

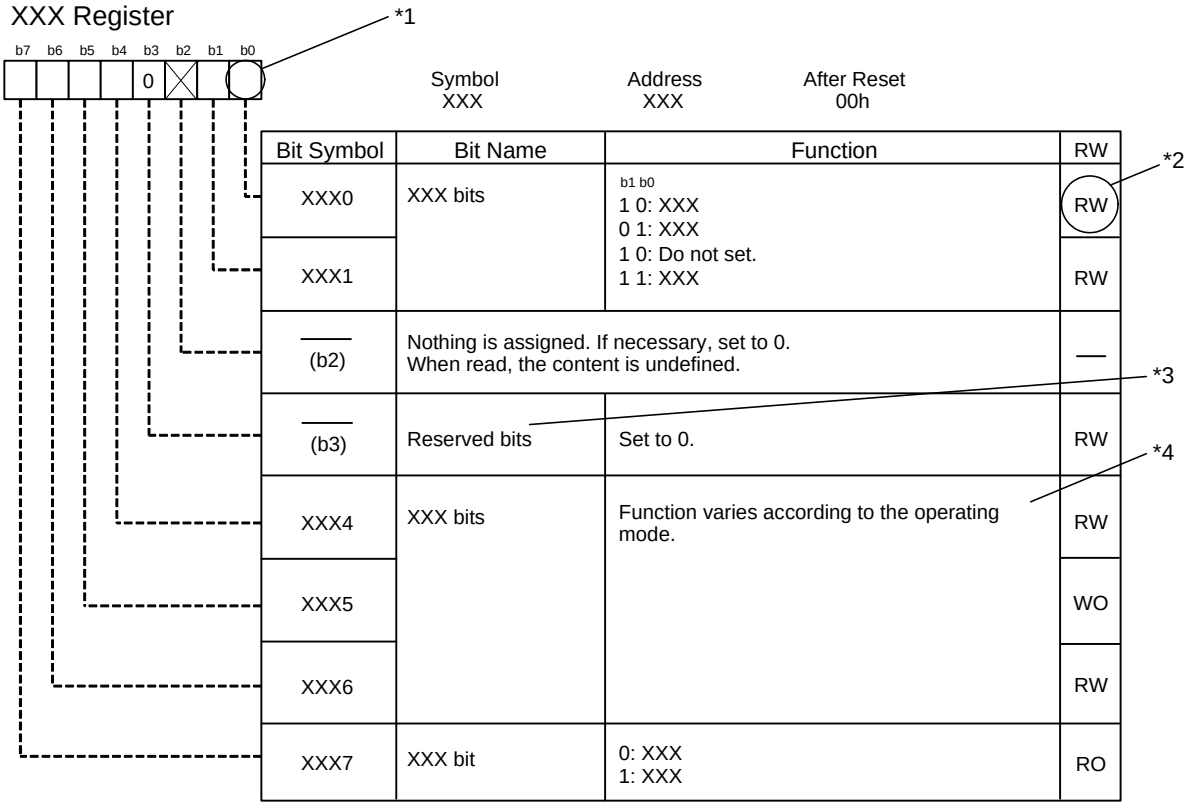
(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.



*1

Blank: Set to 0 or 1 according to the application.
0: Set to 0.
1: Set to 1.
X: Nothing is assigned.

*2

RW: Read and write.
RO: Read only.
WO: Write only.
–: Nothing is assigned.

*3

- Reserved bit
  Reserved bit. Set to specified value.

*4

- Nothing is assigned
  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value
  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.
  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

SFR Page Reference

Address	Register	Symbol	Page
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	60
0005h	Processor Mode Register 1	PM1	154
0006h	System Clock Control Register 0	CM0	103
0007h	System Clock Control Register 1	CM1	105
0008h	Chip Select Control Register	CSR	161
0009h	External Area Recovery Cycle Control Register	EWR	164
000Ah	Protect Register	PRCR	55
000Bh	Data Bank Register	DBR	183
000Ch	Oscillation Stop Detection Register	CM2	107
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	156
0011h	External Area Wait Control Expansion Register	EWC	164
0012h	Peripheral Clock Select Register	PCLKR	109
XXXX X000b		SCM0	
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	288
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	61
0019h	Voltage Detection 2 Circuit Flag Register	VCR1	78
001Ah	Voltage Detection Circuit Operation Enable Register	VCR2	79
001Bh	Chip Select Expansion Control Register	CSE	162
001Ch	PLL Control Register 0	PLC0	110
001Dh			
001Eh	Processor Mode Register 2	PM2	111
001Fh			
0020h			
0021h			
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	112
0023h			
0024h			
0025h			
0026h	Voltage Monitor Function Select Register	VWCE	80
0027h			
0028h	Voltage Detection 1 Level Select Register	VD1LS	80
0029h			
002Ah	Voltage Monitor 0 Circuit Control Register	VW0C	82
002Bh	Voltage Monitor 1 Circuit Control Register	VW1C	83
002Ch	Voltage Monitor 2 Circuit Control Register	VW2C	85
002Dh			
002Eh			
002Fh			
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h			

Address	Register	Symbol	Page
0042h	INT7 Interrupt Control Register	INT7IC	224

Address	Register	Symbol	Page
0043h	INT6 Interrupt Control Register	INT6IC	224
0044h	INT3 Interrupt Control Register	INT3IC	224
0045h	Timer B5 Interrupt Control Register	TB5IC	223
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	223
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	223
0048h	SI/O4 Interrupt Control Register INT5 Interrupt Control Register	S4IC INT5IC	224
0049h	SI/O3 Interrupt Control Register INT4 Interrupt Control Register	S3IC INT4IC	224
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	223
004Bh	DMA0 Interrupt Control Register	DM0IC	223
004Ch	DMA1 Interrupt Control Register	DM1IC	223
004Dh	Key Input Interrupt Control Register	KUPIC	223
004Eh	A/D Conversion Interrupt Control Register	ADIC	223
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	223
0050h	UART2 Receive Interrupt Control Register	S2RIC	223
0051h	UART0 Transmit Interrupt Control Register	S0TIC	223
0052h	UART0 Receive Interrupt Control Register	S0RIC	223
0053h	UART1 Transmit Interrupt Control Register	S1TIC	223
0054h	UART1 Receive Interrupt Control Register	S1RIC	223
0055h	Timer A0 Interrupt Control Register	TA0IC	223
0056h	Timer A1 Interrupt Control Register	TA1IC	223
0057h	Timer A2 Interrupt Control Register	TA2IC	223
0058h	Timer A3 Interrupt Control Register	TA3IC	223
0059h	Timer A4 Interrupt Control Register	TA4IC	223
005Ah	Timer B0 Interrupt Control Register	TB0IC	223
005Bh	Timer B1 Interrupt Control Register	TB1IC	223
005Ch	Timer B2 Interrupt Control Register	TB2IC	223
005Dh	INT0 Interrupt Control Register	INT0IC	224
005Eh	INT1 Interrupt Control Register	INT1IC	224
005Fh	INT2 Interrupt Control Register	INT2IC	224
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	223
006Ah	DMA3 Interrupt Control Register	DM3IC	223
006Bh	UART5 Bus Collision Detection Interrupt Control Register UART5 Bus Collision Detection Interrupt Control Register	U5BCNIC CEC1IC	223
006Ch	UART5 Transmit Interrupt Control Register CEC2 Interrupt Control Register	S5TIC CEC2IC	223
006Dh	UART5 Receive Interrupt Control Register	S5RIC	223
006Eh	UART6 Bus Collision Detection Interrupt Control Register Real-Time Clock Period Interrupt Control Register	U6BCNIC RTCTIC	223
006Fh	UART6 Transmit Interrupt Control Register Real-Time Clock Compare Match Interrupt Control Register	S6TIC RTCCIC	223
0070h	UART6 Receive Interrupt Control Register	S6RIC	223
0071h	UART7 Bus Collision Detection Interrupt Control Register Remote Control Signal Receiver 0 Interrupt Control Register	U7BCNIC PMC0IC	223
0072h	UART7 Transmit Interrupt Control Register Remote Control Signal Receiver 1 Interrupt Control Register	S7TIC PMC1IC	223
0073h	UART7 Receive Interrupt Control Register	S7RIC	223
0074h			
0075h			
0076h			
0077h			
0078h			

Note: 1. Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Page
0079h			
007Ah			
007Bh	IICBus Interface Interrupt Control Register	IICIC	223
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	223
007Dh			
007Eh			
007Fh			
0080h to 017Fh			
0180h 0181h 0182h	DMA0 Source Pointer	SAR0	268
0183h			
0184h 0185h 0186h	DMA0 Destination Pointer	DAR0	268
0187h			
0188h 0189h	DMA0 Transfer Counter	TCR0	269
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	270
018Dh			
018Eh			
018Fh			
0190h 0191h 0192h	DMA1 Source Pointer	SAR1	268
0193h			
0194h 0195h 0196h	DMA1 Destination Pointer	DAR1	268
0197h			
0198h 0199h	DMA1 Transfer Counter	TCR1	269
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	270
019Dh			
019Eh			
019Fh			
01A0h 01A1h 01A2h	DMA2 Source Pointer	SAR2	268
01A3h			
01A4h 01A5h 01A6h	DMA2 Destination Pointer	DAR2	268
01A7h			
01A8h 01A9h	DMA2 Transfer Counter	TCR2	269
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	270
01ADh			
01AEh			
01AFh			
01B0h 01B1h 01B2h	DMA3 Source Pointer	SAR3	268
01B3h			
01B4h 01B5h 01B6h	DMA3 Destination Pointer	DAR3	268
01B7h			
01B8h 01B9h	DMA3 Transfer Counter	TCR3	269
01BAh			

Address	Register	Symbol	Page
01BBh			
01BCh	DMA3 Control Register	DM3CON	270
01BDh			
01BEh			
01BFh			
01C0h 01C1h	Timer B0-1 Register	TB01	341
01C2h 01C3h	Timer B1-1 Register	TB11	341
01C4h 01C5h	Timer B2-1 Register	TB21	341
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	342
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	343
01C9h	Timer B Count Source Select Register 1	TBCS1	343
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	289
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	290
01D1h	Timer A Count Source Select Register 1	TACS1	290
01D2h	Timer A Count Source Select Register 2	TACS2	290
01D3h			
01D4h	16-Bit Pulse Width Modulation Mode Function Select Register	PWMFS	291
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	292
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	293
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	377
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h 01E1h	Timer B3-1 Register	TB31	341
01E2h 01E3h	Timer B4-1 Register	TB41	341
01E4h 01E5h	Timer B5-1 Register	TB51	341
01E6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 2	PPWFS2	342
01E7h			
01E8h	Timer B Count Source Select Register 2	TBCS2	343
01E9h	Timer B Count Source Select Register 3	TBCS3	343
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	PMC0 Function Select Register 0	PMC0CON0	445
01F1h	PMC0 Function Select Register 1	PMC0CON1	447
01F2h	PMC0 Function Select Register 2	PMC0CON2	449
01F3h	PMC0 Function Select Register 3	PMC0CON3	451
01F4h	PMC0 Status Register	PMC0STS	452
01F5h	PMC0 Interrupt Source Select Register	PMC0INT	455
01F6h	PMC0 Compare Control Register	PMC0CPC	460
01F7h	PMC0 Compare Data Register	PMC0CPD	461
01F8h	PMC1 Function Select Register 0	PMC1CON0	445
01F9h	PMC1 Function Select Register 1	PMC1CON1	447
01FAh	PMC1 Function Select Register 2	PMC1CON2	449

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01FBh	PMC1 Function Select Register 3	PMC1CON3	451
01FCh	PMC1 Status Register	PMC1STS	452
01FDh	PMC1 Interrupt Source Select Register	PMC1INT	455
01FEh			
01FFh			
0200h			
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0202h			
0203h			
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0205h	Interrupt Source Select Register 3	IFSR3A	225
0206h	Interrupt Source Select Register 2	IFSR2A	226
0207h	Interrupt Source Select Register	IFSR	227
0208h			
0209h			
020Ah			
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020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	228
020Fh	Address Match Interrupt Enable Register 2	AIER2	228
0210h 0211h 0212h	Address Match Interrupt Register 0	RMAD0	229
0213h			
0214h 0215h 0216h	Address Match Interrupt Register 1	RMAD1	229
0217h			
0218h 0219h 021Ah	Address Match Interrupt Register 2	RMAD2	229
021Bh			
021Ch 021Dh 021Eh	Address Match Interrupt Register 3	RMAD3	229
021Fh			
0220h	Flash Memory Control Register 0	FMR0	130
0221h	Flash Memory Control Register 1	FMR1	701
0222h	Flash Memory Control Register 2	FMR2	131
0223h	Flash Memory Control Register 3	FMR3	703
0224h			
0225h			
0226h			
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0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	704
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
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023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

Address	Register	Symbol	Page
0240h			
0241h			
0242h			
0243h			
0244h	UART0 Special Mode Register 4	U0SMR4	507
0245h	UART0 Special Mode Register 3	U0SMR3	506
0246h	UART0 Special Mode Register 2	U0SMR2	505
0247h	UART0 Special Mode Register	U0SMR	504
0248h	UART0 Transmit/Receive Mode Register	U0MR	498
0249h	UART0 Bit Rate Register	U0BRG	498
024Ah 024Bh	UART0 Transmit Buffer Register	U0TB	495
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	499
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	501
024Eh 024Fh	UART0 Receive Buffer Register	U0RB	496
0250h	UART Transmit/Receive Control Register 2	UCON	503
0251h			
0252h	UART Clock Select Register	UCLKSEL0	494
0253h			
0254h	UART1 Special Mode Register 4	U1SMR4	507
0255h	UART1 Special Mode Register 3	U1SMR3	506
0256h	UART1 Special Mode Register 2	U1SMR2	505
0257h	UART1 Special Mode Register	U1SMR	504
0258h	UART1 Transmit/Receive Mode Register	U1MR	498
0259h	UART1 Bit Rate Register	U1BRG	498
025Ah 025Bh	UART1 Transmit Buffer Register	U1TB	495
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	499
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	501
025Eh 025Fh	UART1 Receive Buffer Register	U1RB	496
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	507
0265h	UART2 Special Mode Register 3	U2SMR3	506
0266h	UART2 Special Mode Register 2	U2SMR2	505
0267h	UART2 Special Mode Register	U2SMR	504
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026Dh	UART2 Transmit/Receive Control Register 1	U2C1	501
026Eh 026Fh	UART2 Receive Buffer Register	U2RB	496
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0272h	SI/O3 Control Register	S3C	558
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0274h	SI/O4 Transmit/Receive Register	S4TRR	557
0275h			
0276h	SI/O4 Control Register	S4C	558
0277h	SI/O4 Bit Rate Register	S4BRG	559
0278h	SI/O3, 4 Control Register 2	S34C2	559
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0280h			
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0282h			

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0283h			
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0285h	UART5 Special Mode Register 3	U5SMR3	506
0286h	UART5 Special Mode Register 2	U5SMR2	505
0287h	UART5 Special Mode Register	U5SMR	504
0288h	UART5 Transmit/Receive Mode Register	U5MR	498
0289h	UART5 Bit Rate Register	U5BRG	498
028Ah 028Bh	UART5 Transmit Buffer Register	U5TB	495
028Ch	UART5 Transmit/Receive Control Register 0	U5C0	499
028Dh	UART5 Transmit/Receive Control Register 1	U5C1	501
028Eh 028Fh	UART5 Receive Buffer Register	U5RB	496
0290h			
0291h			
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0295h	UART6 Special Mode Register 3	U6SMR3	506
0296h	UART6 Special Mode Register 2	U6SMR2	505
0297h	UART6 Special Mode Register	U6SMR	504
0298h	UART6 Transmit/Receive Mode Register	U6MR	498
0299h	UART6 Bit Rate Register	U6BRG	498
029Ah 029Bh	UART6 Transmit Buffer Register	U6TB	495
029Ch	UART6 Transmit/Receive Control Register 0	U6C0	499
029Dh	UART6 Transmit/Receive Control Register 1	U6C1	501
029Eh 029Fh	UART6 Receive Buffer Register	U6RB	496
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02A1h			
02A2h			
02A3h			
02A4h	UART7 Special Mode Register 4	U7SMR4	507
02A5h	UART7 Special Mode Register 3	U7SMR3	506
02A6h	UART7 Special Mode Register 2	U7SMR2	505
02A7h	UART7 Special Mode Register	U7SMR	504
02A8h	UART7 Transmit/Receive Mode Register	U7MR	498
02A9h	UART7 Bit Rate Register	U7BRG	498
02AAh 02ABh	UART7 Transmit Buffer Register	U7TB	495
02ACh	UART7 Transmit/Receive Control Register 0	U7C0	499
02ADh	UART7 Transmit/Receive Control Register 1	U7C1	501
02AEh 02AFh	UART7 Receive Buffer Register	U7RB	496
02B0h	I2C0 Data Shift Register	S00	573
02B1h			
02B2h	I2C0 Address Register 0	S0D0	574
02B3h	I2C0 Control Register	S1D0	575
02B4h	I2C0 Clock Control Register	S20	578
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	581
02B6h	I2C0 Control Register 1	S3D0	582
02B7h	I2C0 Control Register 2	S4D0	587
02B8h	I2C0 Status Register 0	S10	589
02B9h	I2C0 Status Register 1	S11	594
02BAh	I2C0 Address Register 1	S0D1	574
02BBh	I2C0 Address Register 2	S0D2	574
02BCh			
02BDh			
02BEh			
02BFh			
02C0h to 02FFh			
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	345
0301h			
0302h 0303h	Timer A1-1 Register	TA11	295

Address	Register	Symbol	Page
0304h 0305h	Timer A2-1 Register	TA21	295
0306h 0307h	Timer A4-1 Register	TA41	295
0308h	Three-Phase PWM Control Register 0	INVC0	369
0309h	Three-Phase PWM Control Register 1	INVC1	371
030Ah	Three-Phase Output Buffer Register 0	IDB0	373
030Bh	Three-Phase Output Buffer Register 1	IDB1	373
030Ch	Dead Time Timer	DTT	373
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	374
030Eh	Position-Data-Retain Function Control Register	PDRF	376
030Fh			
0310h 0311h	Timer B3 Register	TB3	340
0312h 0313h	Timer B4 Register	TB4	340
0314h 0315h	Timer B5 Register	TB5	340
0316h			
0317h			
0318h	Port Function Control Register	PFCR	377
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	346
031Ch	Timer B4 Mode Register	TB4MR	346
031Dh	Timer B5 Mode Register	TB5MR	346
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	296
0321h			
0322h	One-Shot Start Flag	ONSF	297
0323h	Trigger Select Register	TRGSR	298
0324h	Up/Down Flag	UDF	299
0325h			
0326h 0327h	Timer A0 Register	TA0	294
0328h 0329h	Timer A1 Register	TA1	294
032Ah 032Bh	Timer A2 Register	TA2	294
032Ch 032Dh	Timer A3 Register	TA3	294
032Eh 032Fh	Timer A4 Register	TA4	294
0330h 0331h	Timer B0 Register	TB0	340
0332h 0333h	Timer B1 Register	TB1	340
0334h 0335h	Timer B2 Register	TB2	340
0336h	Timer A0 Mode Register	TA0MR	300
0337h	Timer A1 Mode Register	TA1MR	300
0338h	Timer A2 Mode Register	TA2MR	300
0339h	Timer A3 Mode Register	TA3MR	300
033Ah	Timer A4 Mode Register	TA4MR	300
033Bh	Timer B0 Mode Register	TB0MR	346
033Ch	Timer B1 Mode Register	TB1MR	346
033Dh	Timer B2 Mode Register	TB2MR	346
033Eh	Timer B2 Special Mode Register	TB2SC	375
033Fh			
0340h	Real-Time Clock Second Data Register	RTCSEC	406
0341h	Real-Time Clock Minute Data Register	RTCMIN	407
0342h	Real-Time Clock Hour Data Register	RTCHR	408
0343h	Real-Time Clock Day Data Register	RTCWK	409
0344h	Real-Time Clock Control Register 1	RTCCR1	410
0345h	Real-Time Clock Control Register 2	RTCCR2	412

Note: 1. Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Page
0346h	Real-Time Clock Count Source Select Register	RTCCSR	414
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	415
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	416
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	417
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h	CEC Function Control Register 1	CECC1	622619
0351h	CEC Function Control Register 2	CECC2	623620
0352h	CEC Function Control Register 3	CECC3	625621
0353h	CEC Function Control Register 4	CECC4	627
0354h	CEC Flag Register	CECFLG	629
0355h	CEC Interrupt Source Select Register	CISEL	630
0356h	CEC Transmit Buffer Register 1	CCTB1	631
0357h	CEC Transmit Buffer Register 2	CCTB2	631
0358h	CEC Receive Buffer Register 1	CCRB1	632
0359h	CEC Receive Buffer Register 2	CCRB2	632
035Ah	CEC Receive Follower Address Set Register 1	CRADRI1	633
035Bh	CEC Receive Follower Address Set Register 2	CRADRI2	633
035Ch			
035Dh			
035Eh			
035Fh			
0360h	Pull-Up Control Register 0	PUR0	205
0361h	Pull-Up Control Register 1	PUR1	206
0362h	Pull-Up Control Register 2	PUR2	207
0363h	Pull-Up Control Register 3	PUR3	208
0364h			
0365h			
0366h	Port Control Register	PCR	209
0367h			
0368h			
0369h	NMI/SD Digital Filter Register	NMIDF	213
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			
0370h	PWM Control Register 0	PWMCON0	432
0371h			
0372h	PWM0 Prescaler	PWMPRE0	433
0373h	PWM0 Register	PWMREG0	434
0374h	PWM1 Prescaler	PWMPRE1	433
0375h	PWM1 Register	PWMREG1	434
0376h	PWM Control Register 1	PWMCON1	435
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	257
037Dh	Watchdog Timer Reset Register	WDTR	258
037Eh	Watchdog Timer Start Register	WDTS	258
037Fh	Watchdog Timer Control Register	WDC	259
0380h			
0381h			
0382h			
0383h			
0384h			
0385h			
0386h			
0387h			

Address	Register	Symbol	Page
0388h			
0389h			
038Ah			
038Bh			
038Ch			
038Dh			
038Eh			
038Fh			
0390h	DMA2 Source Select Register	DM2SL	271
0391h			
0392h	DMA3 Source Select Register	DM3SL	271
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	271
0399h			
039Ah	DMA1 Source Select Register	DM1SL	271
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			
03A0h			
03A1h			
03A2h	Open-Circuit Detection Assist Function Register	AINRST	655
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h 03B5h	SFR Snoop Address Register	CRCSAR	690
03B6h	CRC Mode Register	CRCMR	690
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh 03BDh	CRC Data Register	CRCD	689
03BEh	CRC Input Register	CRCIN	689
03BFh			
03C0h 03C1h	A/D Register 0	AD0	661
03C2h 03C3h	A/D Register 1	AD1	661
03C4h 03C5h	A/D Register 2	AD2	661
03C6h 03C7h	A/D Register 3	AD3	661
03C8h 03C9h	A/D Register 4	AD4	661

Note: 1. Blank columns are all reserved space. No access is allowed.

Address	Register	Symbol	Page
03CAh 03CBh	A/D Register 5	AD5	661
03CCh 03CDh	A/D Register 6	AD6	661
03CEh 03CFh	A/D Register 7	AD7	661
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	657
03D5h			
03D6h	A/D Control Register 0	ADCON0	658
03D7h	A/D Control Register 1	ADCON1	660
03D8h	D/A0 Register	DA0	685
03D9h			
03DAh	D/A1 Register	DA1	685
03DBh			
03DCh	D/A Control Register	DACON	685
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	210
03E1h	Port P1 Register	P1	210
03E2h	Port P0 Direction Register	PD0	212
03E3h	Port P1 Direction Register	PD1	212
03E4h	Port P2 Register	P2	210
03E5h	Port P3 Register	P3	210
03E6h	Port P2 Direction Register	PD2	212
03E7h	Port P3 Direction Register	PD3	212
03E8h	Port P4 Register	P4	210
03E9h	Port P5 Register	P5	210
03EAh	Port P4 Direction Register	PD4	212
03EBh	Port P5 Direction Register	PD5	212
03ECh	Port P6 Register	P6	210
03EDh	Port P7 Register	P7	210
03EEh	Port P6 Direction Register	PD6	212
03EFh	Port P7 Direction Register	PD7	212
03F0h	Port P8 Register	P8	210
03F1h	Port P9 Register	P9	210
03F2h	Port P8 Direction Register	PD8	212
03F3h	Port P9 Direction Register	PD9	212
03F4h	Port P10 Register	P10	210
03F5h	Port P11 Register	P11	210
03F6h	Port P10 Direction Register	PD10	212
03F7h	Port P11 Direction Register	PD11	212
03F8h	Port P12 Register	P12	210
03F9h	Port P13 Register	P13	210
03FAh	Port P12 Direction Register	PD12	212
03FBh	Port P13 Direction Register	PD13	212
03FCh	Port P14 Register	P14	210
03FDh			
03FEh	Port P14 Direction Register	PD14	212
03FFh			
D000h to D07Fh			

Address	Register	Symbol	Page
D080h D081h	PMC0 Header Pattern Set Register (Min)	PMC0HDPMIN	456
D082h D083h	PMC0 Header Pattern Set Register (Max)	PMC0HDPMAX	456
D084h	PMC0 Data0 Pattern Set Register (Min)	PMC0D0PMIN	457
D085h	PMC0 Data0 Pattern Set Register (Max)	PMC0D0PMAX	457
D086h	PMC0 Data1 Pattern Set Register (Min)	PMC0D1PMIN	457
D087h	PMC0 Data1 Pattern Set Register (Max)	PMC0D1PMAX	457
D088h D089h	PMC0 Measurements Register	PMC0TIM	458
D08Ah D08Bh	PMC0 Counter Value Register	PMC0BC	458
D08Ch	PMC0 Receive Data Store Register 0	PMC0DAT0	459
D08Dh	PMC0 Receive Data Store Register 1	PMC0DAT1	459
D08Eh	PMC0 Receive Data Store Register 2	PMC0DAT2	459
D08Fh	PMC0 Receive Data Store Register 3	PMC0DAT3	459
D090h	PMC0 Receive Data Store Register 4	PMC0DAT4	459
D091h	PMC0 Receive Data Store Register 5	PMC0DAT5	459
D092h	PMC0 Receive Bit Count Register	PMC0RBIT	458
D093h			
D094h D095h	PMC1 Hedder Pattern Set Register (Min)	PMC1HDPMIN	456
D096h D097h	PMC1 Header Pattern Set Register (Max)	PMC1HDPMAX	456
D098h	PMC1 Data0 Pattern Set Register (Min)	PMC1D0PMIN	457
D099h	PMC1 Data0 Pattern Set Register (Max)	PMC1D0PMAX	457
D09Ah	PMC1 Data1 Pattern Set Register (Min)	PMC1D1PMIN	457
D09Bh	PMC1 Data1 Pattern Set Register (Max)	PMC1D1PMAX	457
D09Ch D09Dh	PMC1 Measurements Register	PMC1TIM	458
D09Eh D09Fh	PMC1 Counter Value Register	PMC1BC	458

Note: 1. Blank columns are all reserved space. No access is allowed.

FFFFFh	Optional Function Select Address 1	OFS1	63

Note: 1. OFS1 address is not an SFR.

1. Overview

1.1 Features

The M16C/65 Group microcomputer (MCU) incorporates the M16C/60 Series CPU core and flash memory, employing sophisticated instructions for a high level of efficiency. This MCU has 1 Mbyte of address space (expandable to 4 Mbytes), and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the M16C/65 Group supports operating modes that allow additional power control. The MCU also uses an anti-noise configuration to reduce emissions of electromagnetic noise and is designed to withstand electromagnetic interference (EMI). By integrating many of the peripheral functions, including the multifunction timer and serial interface, the number of system components has been reduced.

1.1.1 Applications

Audio components, cameras, televisions, household appliances, office equipment, communication devices, mobile devices, industrial equipment, etc.

1.2 Specifications

The M16C/65 Group includes 128-pin, 100-pin, and 80-pin packages. Table 1.1 to Table 1.6 list specifications.

Table 1.1 Specifications (128-Pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 core (multiplier: 16-bit × 16-bit → 32-bit, multiply and accumulate instruction: 16-bit × 16-bit + 32-bit →32-bit) • Number of basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC1 = 3.0 to 5.5 V) • Operating modes: Single-chip, memory expansion, and microprocessor
Memory	ROM, RAM, data flash	See Table 1.7 “Product List”.
Voltage Detection	Voltage detector	• Power-on reset • 3 voltage detection points (detection level of voltage detection 0 and 1 selectable)
Clock	Clock generator	• 5 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ± 10%), PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection and re-oscillation detection function • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 • Power save: Wait mode, stop mode • Real time clock
External Bus Expansion	Bus and memory expansion	• Address space: 1 Mbyte • External bus interface: 0 to 8 wait states, 4 chip select outputs, memory area expansion function (extension enable up to 4 Mbytes), 3 V and 5 V interfaces • Bus format: Separate bus or multiplexed bus selectable, data bus width selectable (8 or 16 bits), number of address buses selectable (12, 16, or 20)
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 111, selectable pull-up resistor • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt input: 13 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 8, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15 bits × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)

Table 1.2 Specifications (128-Pin Package) (2/2)

Item	Function	Specification
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer function	Three-phase inverter control (timer A1, timer A2, timer A4, timer B2), on-chip dead time timer
	Real-time clock	Count: second, minute, hour, day of week
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5 to UART7	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus (1), special mode 2 SIM (UART2)
	SI/O3, SI/O4	Clock synchronization only × 2 channels
	Multi-master I^2C bus interface	1 channel
	CEC function (3)	CEC transmit/receive, arbitration lost detection, ACK signal generation, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		Programming and erasure power supply voltage: 2.7 to 5.5 V Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) Program security: ROM code protect, ID code check
Debug Function		Functions on-chip debug, on-board flash rewrite function, address match × 4
Operation Frequency/Supply Voltage		25 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1 32 MHz/VCC1 = 3.0 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		TBD (32 MHz/VCC1 = VCC2 = 3 V) TBD (VCC1 = VCC2 = 3 V, in stop mode)
Operating Temperature		-20°C to 85°C, -40°C to 85°C (2)
Package		128-pin LQFP: PLQP0128KB-A (Previous package code: 128P6Q-A)

Notes:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. See Table 1.7 “Product List” for the operating temperature.
3. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

Table 1.3 Specifications (100-Pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 core (multiplier: 16-bit × 16-bit → 32-bit, multiply and accumulate instruction: 16-bit × 16-bit + 32-bit →32-bit) • Number of basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC1 = 3.0 to 5.5 V) • Operating modes: Single-chip, memory expansion, and microprocessor
Memory	ROM, RAM, data flash	See Table 1.7 “Product List”.
Voltage Detection	Voltage detector	• Power-on reset • 3 voltage detection points (detection level of voltage detection 0 and 1 selectable)
Clock	Clock generator	• 5 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ± 10%), PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection and re-oscillation detection function • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 • Power save: Wait mode, stop mode • Real time clock
External Bus Expansion	Bus and memory expansion	• Address space: 1 Mbyte • External bus interface: 0 to 8wait states, 4 chip select outputs, memory area expansion function (extension enable up to 4-Mbyte), 3 V, 5 V interface • Bus format: Separate bus or multiplexed bus selectable, data bus width selectable (8 or 16 bits), number of address buses selectable (12, 16, or 20)
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 85, selectable pull-up resistor • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt input: 13 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 8, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15 bits × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)

Table 1.4 Specifications (100-Pin Package) (2/2)

Item	Function	Specification
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode Event counter two-phase pulse signal processing (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Three-phase motor control timer function	Three-phase inverter control (timer A1, timer A2, timer A4, timer B2), on-chip dead time timer
	Real-time clock	Count: second, minute, hour, day of week
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit) • Operating frequency of 32 kHz
Serial Interface	UART0 to UART2, UART5 to UART7	Clock synchronous/asynchronous × 6 channels I^2C-bus, IEBus (1), special mode 2 SIM (UART2)
	SI/O3, SI/O4	Clock synchronization only × 2 channels
	Multi-master I^2C bus interface	1 channel
	CEC function (3)	CEC transmit/receive, arbitration lost detection, ACK signal generation, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		Programming and erasure power supply voltage: 2.7 to 5.5 V Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) Program security: ROM code protect, ID code check
Debug Function		Functions on-chip debug, on-board flash rewrite function, address match × 4
Operation Frequency/Supply Voltage		25 MHz/VCC1 = 2.7 to 5.5 V, VCC2 = 2.7 V to VCC132 MHz/VCC1 = 3.0 to 5.5 V, VCC2 = 2.7 V to VCC1
Current Consumption		TBD (32 MHz/VCC1 = VCC2 = 3 V) TBD (VCC1 = VCC2 = 3 V, in stop mode)
Operating Temperature		-20°C to 85°C, -40°C to 85°C (2)
Package		100-pin QFP: PRQP0100JD-B (Previous package code: 100P6F-A) 100-pin LQFP: PLQP0100KB-A (Previous package code: 100P6Q-A)

Notes:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. See Table 1.7 “Product List” for the operating temperature.
3. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

Table 1.5 Specifications (80-Pin Package) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 core (multiplier: 16-bit × 16-bit → 32-bit, multiply and accumulate instruction: 16-bit × 16-bit + 32-bit →32-bit) • Number of basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC1 = 3.0 to 5.5 V) • Operating modes: Single-chip
Memory	ROM, RAM, data flash	See Table 1.7 “Product List”.
Voltage Detection	Voltage detector	• Power-on reset • 3 voltage detection points (detection level of voltage detection 0 and 1 selectable)
Clock	Clock generator	• 5 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), high-speed on-chip oscillator (40 MHz ± 10%), PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop detection and re-oscillation detection function • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, and 16 • Power save: Wait mode, stop mode • Real time clock
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 68, selectable pull-up resistor • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt input: 10 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 5, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		15 bits × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)
Timer	Timer A	16-bit timer × 5 Timer mode × 5 Event counter mode, one shot timer mode, pulse width modulation (PWM) mode × 3 Event counter two-phase pulse signal processing (two-phase encoder input) × 2 Programmable output mode × 1
	Timer B	16-bit timer × 6 Timer mode × 6 Event counter mode, pulse period measurement mode, pulse width measurement mode × 5
	Real-time clock	Count: second, minute, hour, day of week
	PWM function	8 bits × 2
	Remote control signal receiver	• 2 circuits • 4 wave pattern matchings (differentiate wave pattern for headers, data 0, data 1, and special data) • 6-byte receive buffer (1 circuit) • Operating frequency of 32 kHz

Table 1.6 Specifications (80-Pin Package) (2/2)

Item	Function	Specification
Serial Interface	UART0 to UART2, UART5	Clock synchronous/asynchronous × 3 channels I²C-bus, IEBus (1), special mode 2 SIM (UART2) Clock asynchronous × 1 channel I²C-bus, IEBus (1)
	SI/O3, SI/O4	Clock synchronization only × 2 channels (SI/O3 is used for transmission only)
	Multi-master I²C bus interface	1 channel
	CEC function (3)	CEC transmit/receive, arbitration lost detection, ACK signal generation, operation frequency of 32 kHz
A/D Converter		10-bit resolution × 26 channels, including sample and hold function Conversion time: 1.72 µs
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash Memory		Programming and erasure power supply voltage: 2.7 to 5.5 V Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) Program security: ROM code protect, ID code check
Debug Function		Functions on-chip debug, on-board flash rewrite function, address match × 4
Operation Frequency/Supply Voltage		25 MHz/VCC1 = 2.7 to 5.5 V 32 MHz/VCC1 = 3.0 to 5.5 V
Current Consumption		TBD (32 MHz/VCC1 = 3 V) TBD (VCC1 = 3 V, in stop mode)
Operating Temperature		-20°C to 85°C, -40°C to 85°C (2)
Package		80-pin LQFP: PLQP080JA-A (Previous package code: FP-80W)

Notes:
1. IEBus is a registered trademark of NEC Electronics Corporation.
2. See Table 1.7 “Product List” for the operating temperature.
3. The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the High-Definition Multimedia Interface (HDMI). HDMI and High-Definition Multimedia Interface are registered trademarks of HDMI Licensing, LLC.

1.3 Product List

Table 1.7 lists product information. Figure 1.1 shows Correspondence of Part No., with Memory Size and Package, and Figure 1.2 shows Marking Diagram of Flash Memory Package (Top View).

Table 1.7 Product List

Part No.	ROM Capacity			RAM Capacity	Package Code	Remarks
	Program ROM1	Program ROM2	Data Flash			
R5F36506NFA (P)	128 Kbytes	16 Kbytes	4 Kbytes × 2 blocks	12 Kbytes	PRQP0100JD-B	Operating temperature -20°C to 85°C
R5F36506NFB (P)					PLQP0100KB-A	
R5F36526NFP (P)					PLQP0080JA-A	
R5F36506DFA (P)					PRQP0100JD-B	Operating temperature -40°C to 85°C
R5F36506DFB (P)					PLQP0100KB-A	
R5F36526DFP (P)					PLQP0080JA-A	
R5F3651ENFC (P)	256 Kbytes	16 Kbytes	4 Kbytes × 2 blocks	20 Kbytes	PLQP0128KB-A	Operating temperature -20°C to 85°C
R5F3650ENFA (P)					PRQP0100JD-B	
R5F3650ENFB (P)					PLQP0100KB-A	
R5F3651EDFC (P)					PLQP0128KB-A	Operating temperature -40°C to 85°C
R5F3650EDFA (D)					PRQP0100JD-B	
R5F3650EDFB (D)					PLQP0100KB-A	
R5F3651KNFC (P)	384 Kbytes	16 Kbytes	4 Kbytes × 2 blocks	31 Kbytes	PLQP0128KB-A	Operating temperature -20°C to 85°C
R5F3650KNFB (P)					PRQP0100JD-B	
R5F3650KNFA (P)					PLQP0100KB-A	
R5F3651KDFC (P)					PLQP0128KB-A	Operating temperature -40°C to 85°C
R5F3650KDFB (P)					PRQP0100JD-B	
R5F3650KDFA (P)					PLQP0100KB-A	
R5F3651MNFC (P)	512 Kbytes	16 Kbytes	4 Kbytes × 2 blocks	31 Kbytes	PLQP0128KB-A	Operating temperature -20°C to 85°C
R5F3650MNFA (P)					PRQP0100JD-B	
R5F3650MNFB (P)					PLQP0100KB-A	
R5F3651MDFC (P)					PLQP0128KB-A	Operating temperature -40°C to 85°C
R5F3650MDFA (P)					PRQP0100JD-B	
R5F3650MDFB (P)					PLQP0100KB-A	
R5F3651RNFC (P)	640 Kbytes	16 Kbytes	4 Kbytes × 2 blocks	47 Kbytes	PLQP0128KB-A	Operating temperature -20°C to 85°C
R5F3650RNFB (P)					PRQP0100JD-B	
R5F3650RNFA (P)					PLQP0100KB-A	
R5F3651RDFC (P)					PLQP0128KB-A	Operating temperature -40°C to 85°C
R5F3650RDFB (P)					PRQP0100JD-B	
R5F3650RDFA (P)					PLQP0100KB-A	
R5F3651TNFC (D)	768 Kbytes	16 Kbytes	4 Kbytes × 2 blocks	47 Kbytes	PLQP0128KB-A	Operating temperature -20°C to 85°C
R5F3650TNFA (P)					PRQP0100JD-B	
R5F3650TNFB (P)					PLQP0100KB-A	
R5F3651TDFC (D)					PLQP0128KB-A	Operating temperature -40°C to 85°C
R5F3650TDFA (P)					PRQP0100JD-B	
R5F3650TDFB (P)					PLQP0100KB-A	

(D): Under development
(P): Planning
Note:
1. Previous package codes are as follows.
PLQP0128KB-A: 128P6Q-A, PRQP0100JD-B: 100P6F-A, PLQP0100KB-A: 100P6Q-A,
PLQP0080JA-A: FP-80W

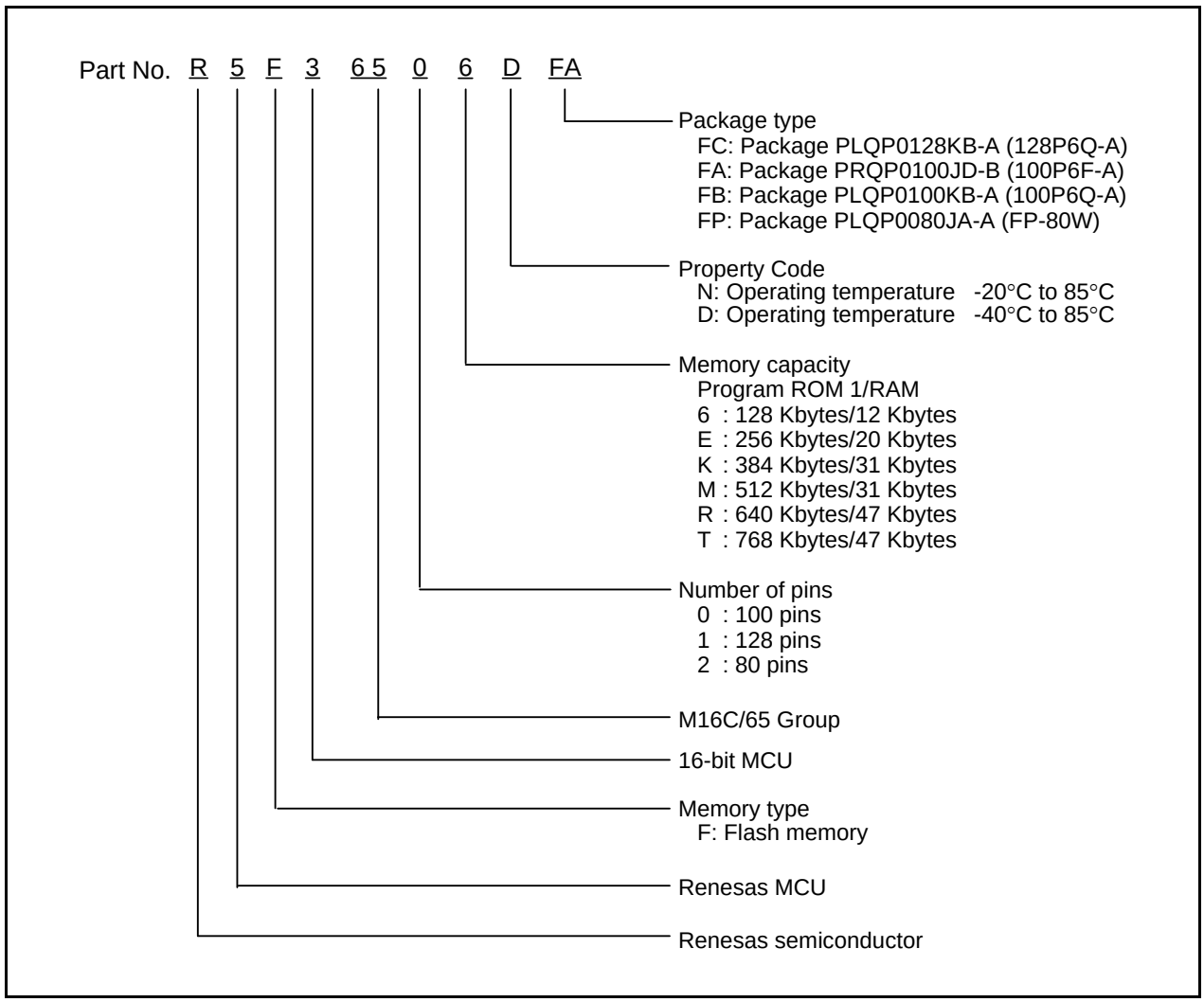


Figure 1.1 Correspondence of Part No., with Memory Size and Package

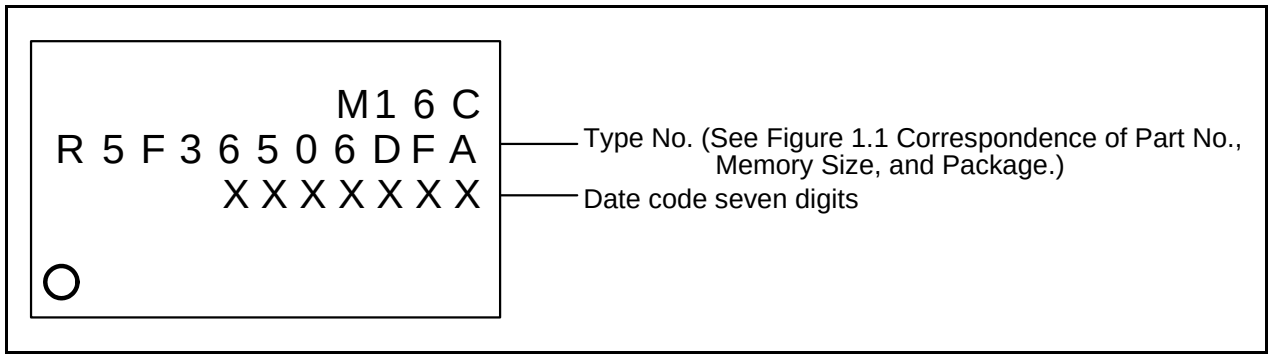


Figure 1.2 Marking Diagram of Flash Memory Package (Top View)

1.4 Block Diagram

Figure 1.3 to Figure 1.5 show block diagrams.

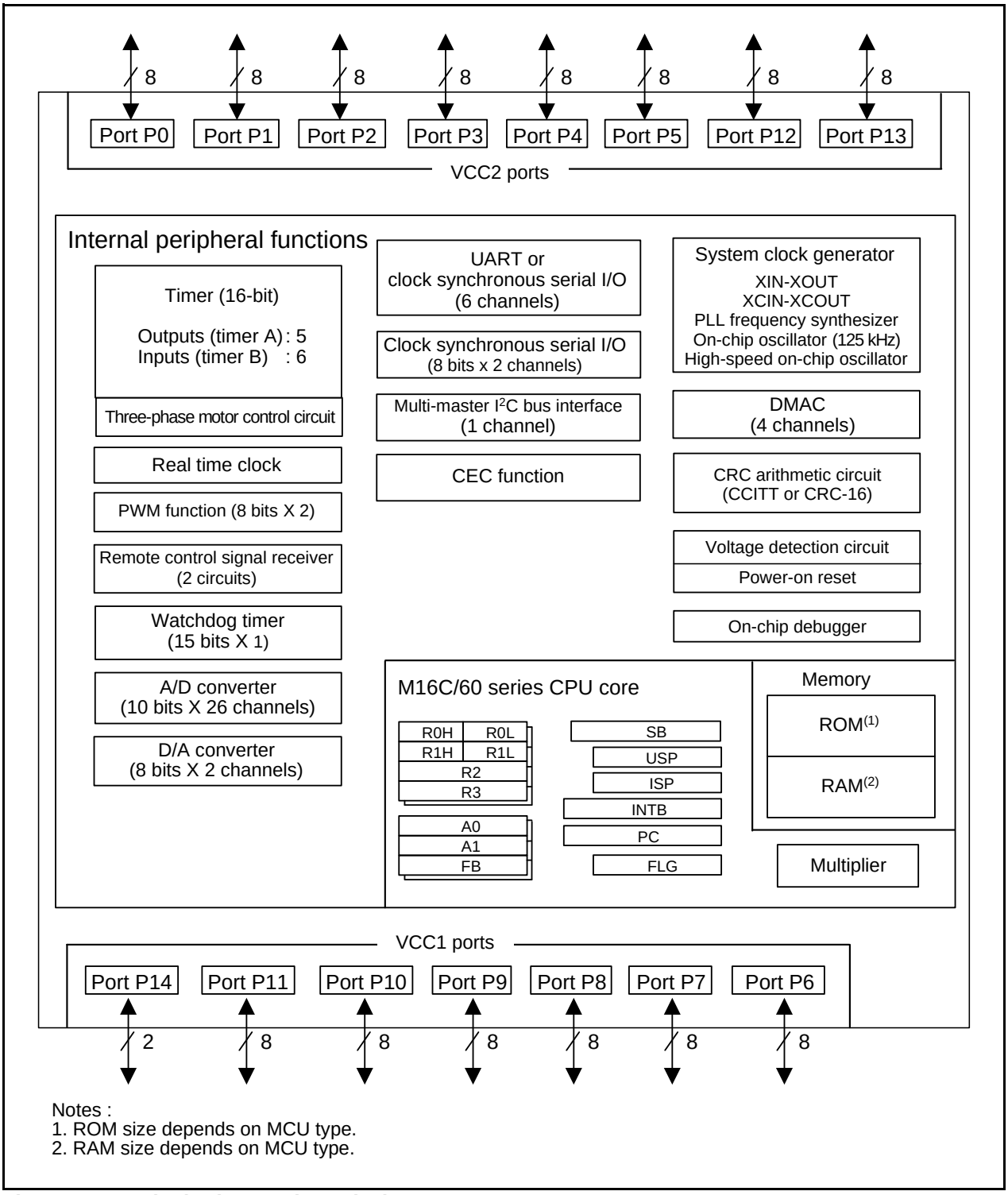


Figure 1.3 Block Diagram (128 pins)

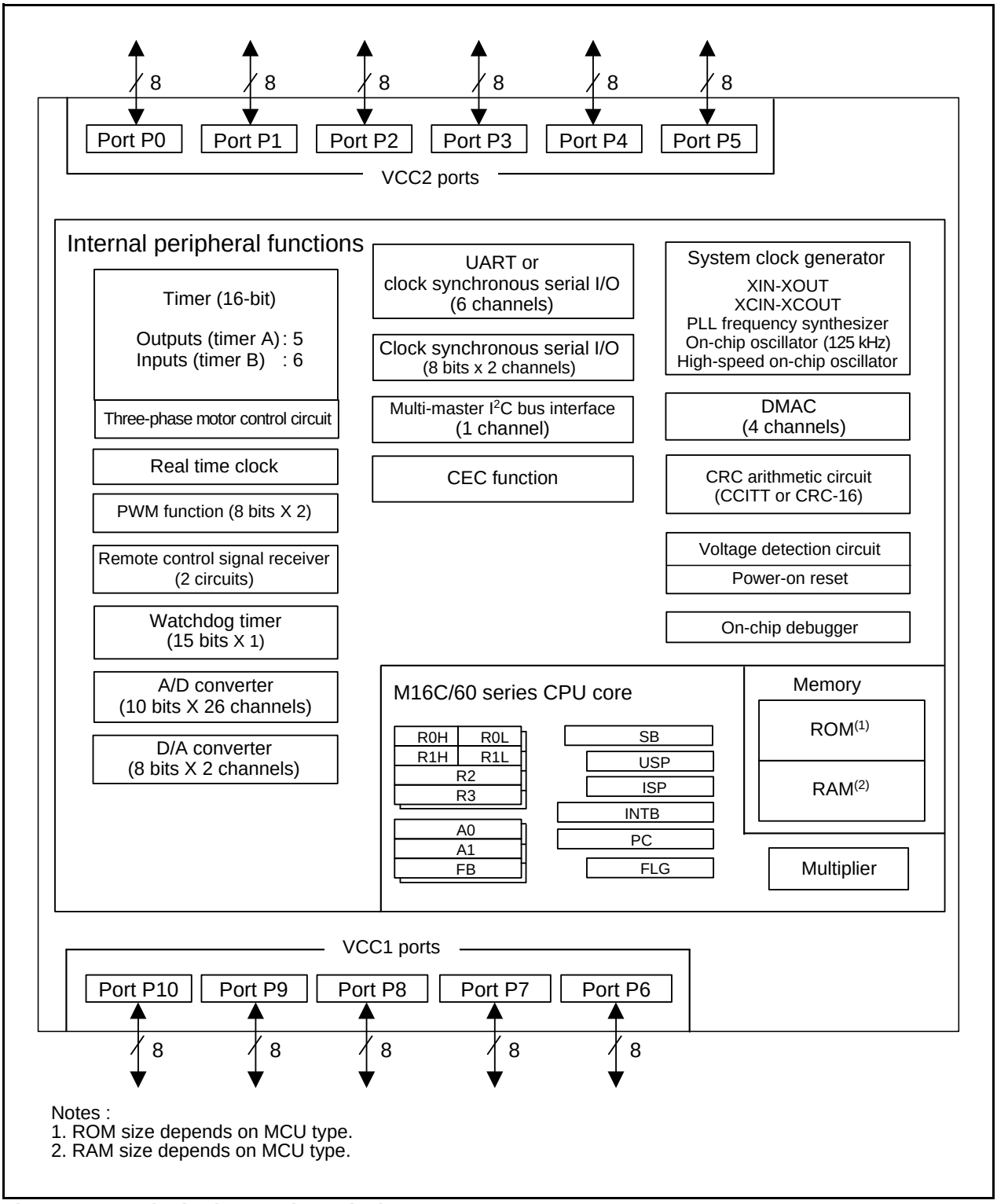
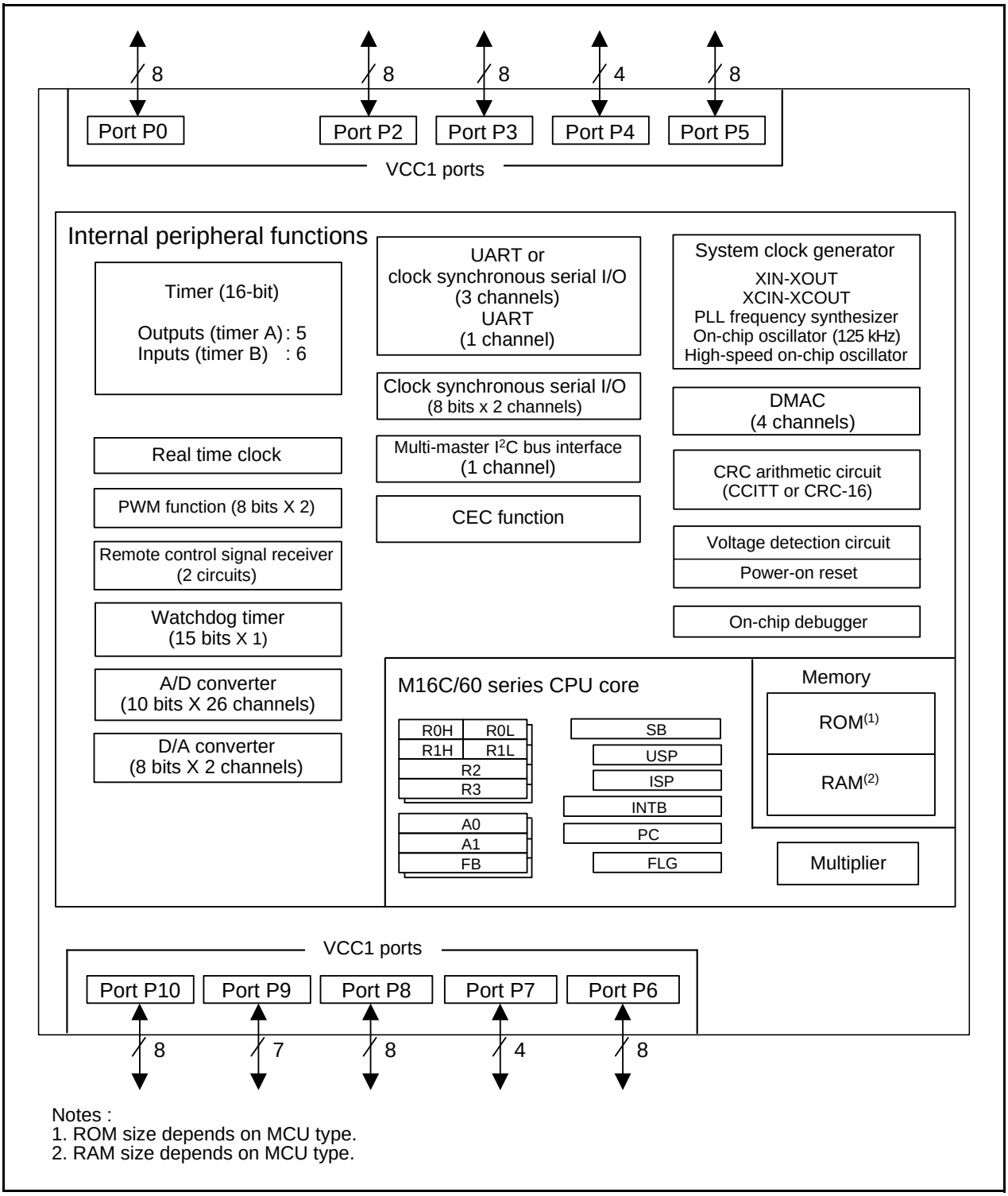


Figure 1.4 Block Diagram (100 pins)

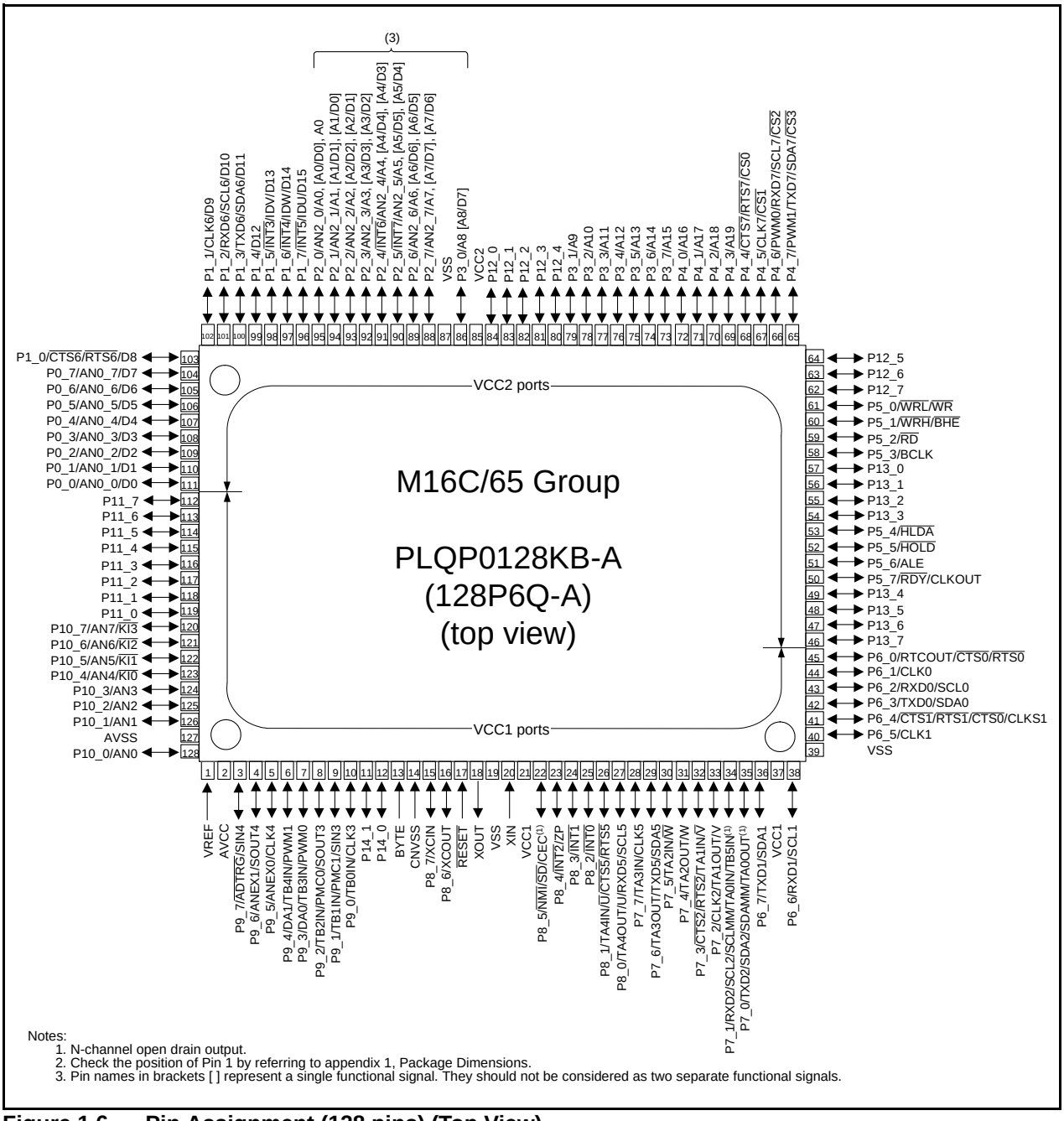


Notes :
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

Figure 1.5 Block Diagram (80 pins)

1.5 Pin Assignments

Figure 1.6 to Figure 1.9 show pin assignments (top view). Table 1.8 to Table 1.14 list pin names.



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.6 Pin Assignment (128 pins) (Top View)

Table 1.8 Pin Names, 128-Pin Package (1/3)

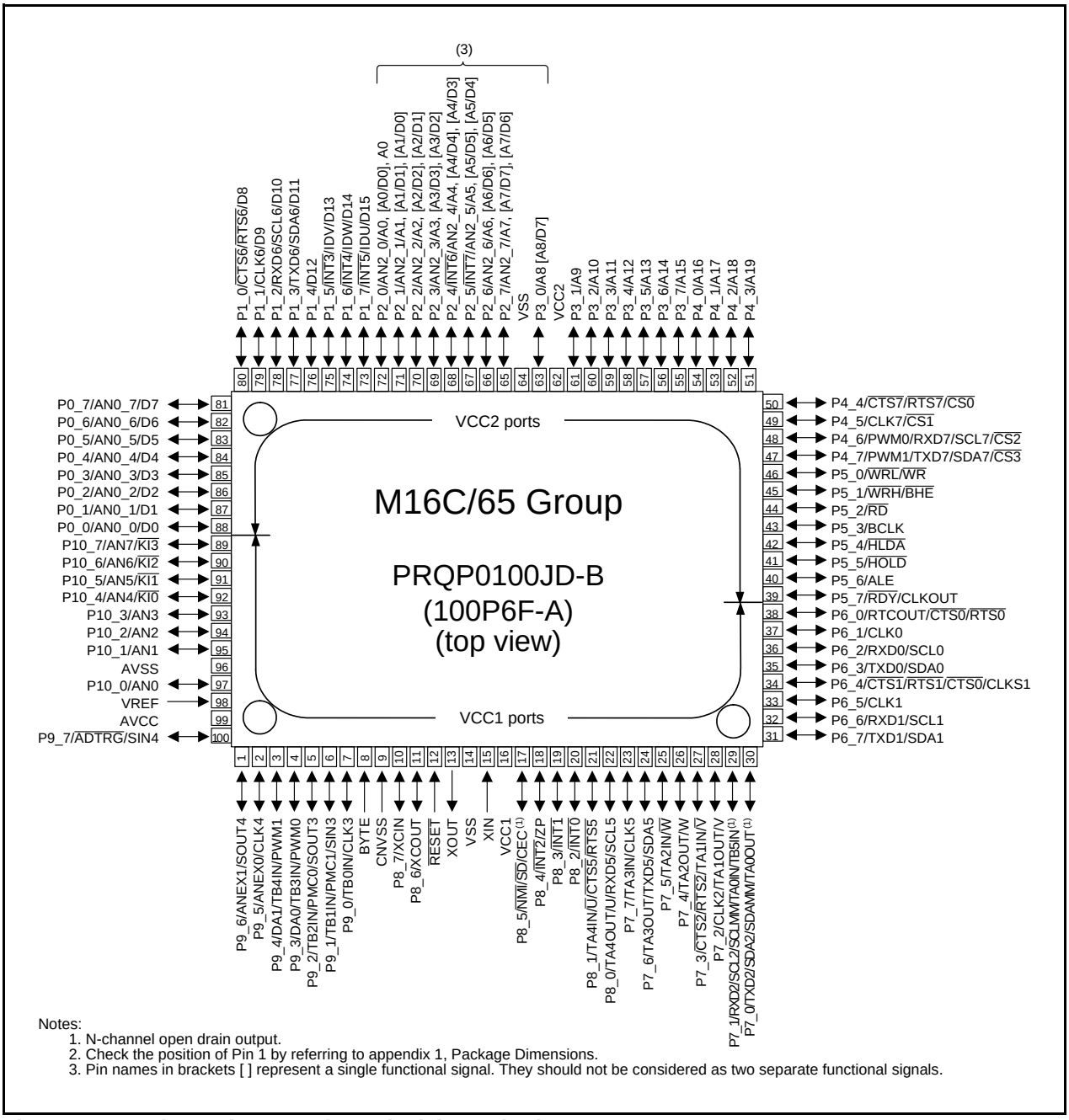
Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
1	VREF						
2	AVCC						
3		P9_7			SIN4	$\overline{\text{ADTRG}}$	
4		P9_6			SOUT4	ANEX1	
5		P9_5			CLK4	ANEX0	
6		P9_4		TB4IN/PWM1		DA1	
7		P9_3		TB3IN/PWM0		DA0	
8		P9_2		TB2IN/PMC0	SOUT3		
9		P9_1		TB1IN/PMC1	SIN3		
10		P9_0		TB0IN	CLK3		
11		P14_1					
12		P14_0					
13	BYTE						
14	CNVSS						
15	XCIN	P8_7					
16	XCOUT	P8_6					
17	$\overline{\text{RESET}}$						
18	XOUT						
19	VSS						
20	XIN						
21	VCC1						
22		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$	CEC		
23		P8_4	$\overline{\text{INT2}}$	ZP			
24		P8_3	$\overline{\text{INT1}}$				
25		P8_2	$\overline{\text{INT0}}$				
26		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$		
27		P8_0		TA4OUT/U	RXD5/SCL5		
28		P7_7		TA3IN	CLK5		
29		P7_6		TA3OUT	TXD5/SDA5		
30		P7_5		TA2IN/$\overline{\text{W}}$			
31		P7_4		TA2OUT/W			
32		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$		
33		P7_2		TA1OUT/V	CLK2		
34		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
35		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
36		P6_7			TXD1/SDA1		
37	VCC1						
38		P6_6			RXD1/SCL1		
39	VSS						
40		P6_5			CLK1		
41		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1		
42		P6_3			TXD0/SDA0		
43		P6_2			RXD0/SCL0		
44		P6_1			CLK0		
45		P6_0		RTCOUT	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
46		P13_7					
47		P13_6					
48		P13_5					
49		P13_4					
50	CLKOUT	P5_7					$\overline{\text{RDY}}$

Table 1.9 Pin Names, 128-Pin Package (2/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
51		P5_6					ALE
52		P5_5					$\overline{\text{HOLD}}$
53		P5_4					$\overline{\text{HLDA}}$
54		P13_3					
55		P13_2					
56		P13_1					
57		P13_0					
58		P5_3					BCLK
59		P5_2					$\overline{\text{RD}}$
60		P5_1					$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
61		P5_0					$\overline{\text{WRL}}$/$\overline{\text{WR}}$
62		P12_7					
63		P12_6					
64		P12_5					
65		P4_7		PWM1	TXD7/SDA7		$\overline{\text{CS3}}$
66		P4_6		PWM0	RXD7/SCL7		$\overline{\text{CS2}}$
67		P4_5			CLK7		$\overline{\text{CS1}}$
68		P4_4			$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$		$\overline{\text{CS0}}$
69		P4_3					A19
70		P4_2					A18
71		P4_1					A17
72		P4_0					A16
73		P3_7					A15
74		P3_6					A14
75		P3_5					A13
76		P3_4					A12
77		P3_3					A11
78		P3_2					A10
79		P3_1					A9
80		P12_4					
81		P12_3					
82		P12_2					
83		P12_1					
84		P12_0					
85	VCC2						
86		P3_0					A8, [A8/D7]
87	VSS						
88		P2_7				AN2_7	A7, [A7/D7], [A7/D6]
89		P2_6				AN2_6	A6, [A6/D6], [A6/D5]
90		P2_5	$\overline{\text{INT7}}$			AN2_5	A5, [A5/D5], [A5/D4]
91		P2_4	$\overline{\text{INT6}}$			AN2_4	A4[A4/D4], [A4/D3]
92		P2_3				AN2_3	A3, [A3/D3], [A3/D2]
93		P2_2				AN2_2	A2, [A2/D2], [A2/D1]
94		P2_1				AN2_1	A1, [A1/D1], [A1/D0]
95		P2_0				AN2_0	A0, [A0/D0], A0
96		P1_7	$\overline{\text{INT5}}$	IDU			D15
97		P1_6	$\overline{\text{INT4}}$	IDW			D14
98		P1_5	$\overline{\text{INT3}}$	IDV			D13
99		P1_4					D12
100		P1_3			TXD6/SDA6		D11

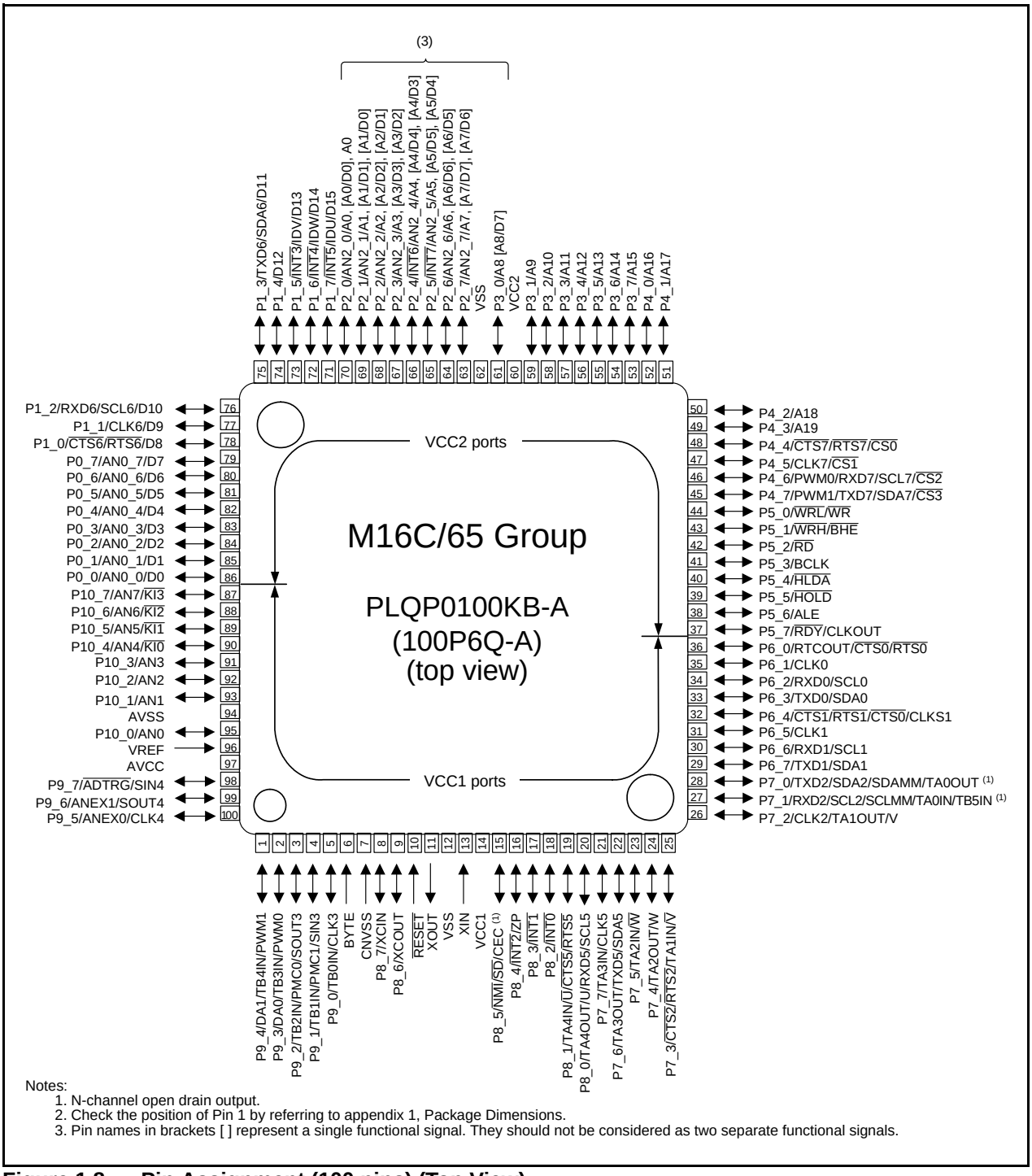
Table 1.10 Pin Names, 128-Pin Package (3/3)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
101		P1_2			RXD6/SCL6		D10
102		P1_1			CLK6		D9
103		P1_0			$\overline{CTS6}$/$\overline{RTS6}$		D8
104		P0_7				AN0_7	D7
105		P0_6				AN0_6	D6
106		P0_5				AN0_5	D5
107		P0_4				AN0_4	D4
108		P0_3				AN0_3	D3
109		P0_2				AN0_2	D2
110		P0_1				AN0_1	D1
111		P0_0				AN0_0	D0
112		P11_7					
113		P11_6					
114		P11_5					
115		P11_4					
116		P11_3					
117		P11_2					
118		P11_1					
119		P11_0					
120		P10_7	$\overline{KI3}$			AN7	
121		P10_6	$\overline{KI2}$			AN6	
122		P10_5	$\overline{KI1}$			AN5	
123		P10_4	$\overline{KI0}$			AN4	
124		P10_3				AN3	
125		P10_2				AN2	
126		P10_1				AN1	
127	AVSS						
128		P10_0				AN0	



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

Figure 1.7 Pin Assignment (100 pins) (Top View)



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.
3. Pin names in brackets [ ] represent a single functional signal. They should not be considered as two separate functional signals.

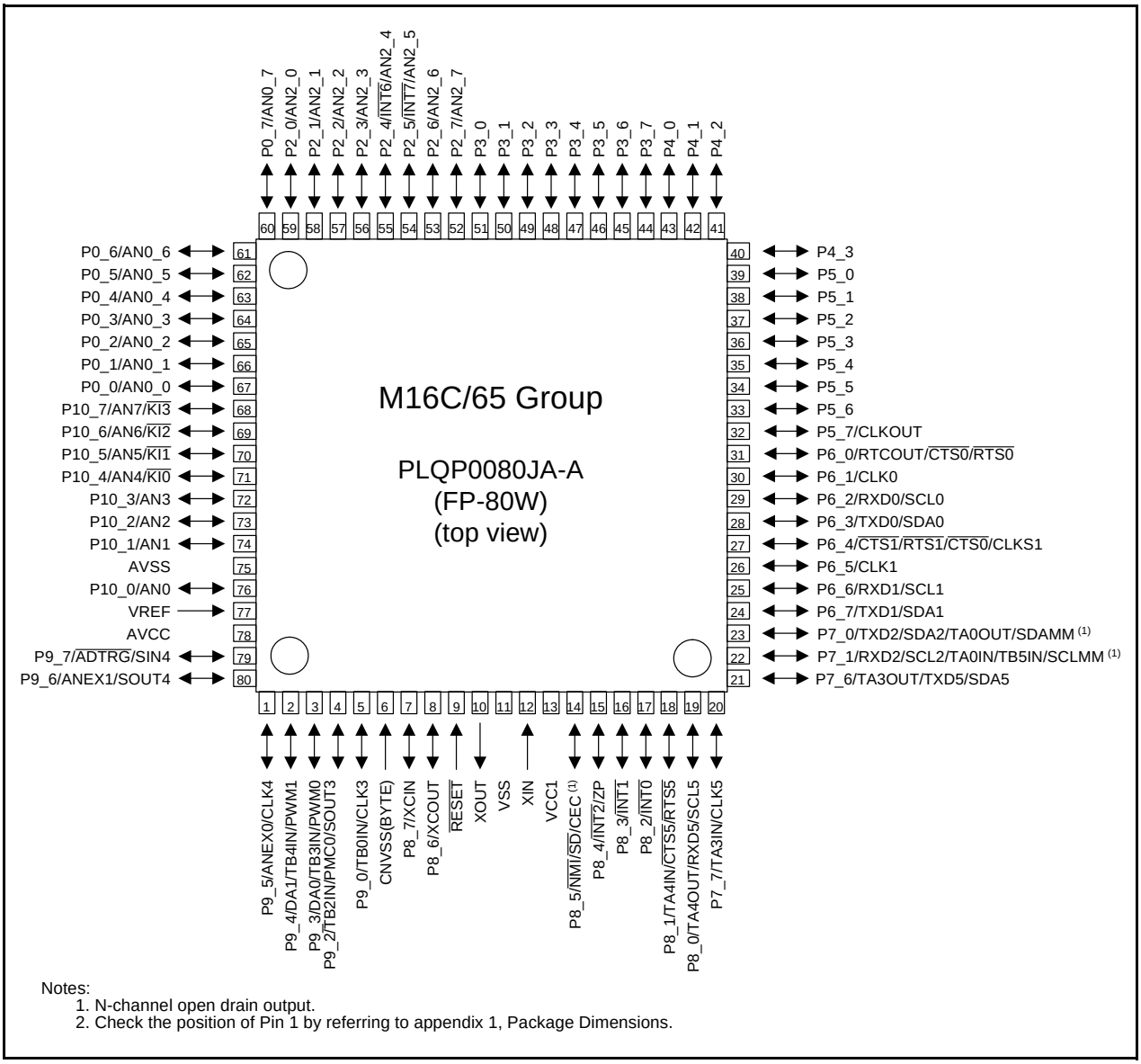
Figure 1.8 Pin Assignment (100 pins) (Top View)

Table 1.11 Pin Names, 100-Pin Package (1/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
1	99		P9_6			SOUT4	ANEX1	
2	100		P9_5			CLK4	ANEX0	
3	1		P9_4		TB4IN/PWM1		DA1	
4	2		P9_3		TB3IN/PWM0		DA0	
5	3		P9_2		TB2IN/PMC0	SOUT3		
6	4		P9_1		TB1IN/PMC1	SIN3		
7	5		P9_0		TB0IN	CLK3		
8	6	BYTE						
9	7	CNVSS						
10	8	XCIN	P8_7					
11	9	XCOUT	P8_6					
12	10	$\overline{\text{RESET}}$						
13	11	XOUT						
14	12	VSS						
15	13	XIN						
16	14	VCC1						
17	15		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$	CEC		
18	16		P8_4	$\overline{\text{INT2}}$	ZP			
19	17		P8_3	$\overline{\text{INT1}}$				
20	18		P8_2	$\overline{\text{INT0}}$				
21	19		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$		
22	20		P8_0		TA4OUT/U	RXD5/SCL5		
23	21		P7_7		TA3IN	CLK5		
24	22		P7_6		TA3OUT	TXD5/SDA5		
25	23		P7_5		TA2IN/$\overline{\text{W}}$			
26	24		P7_4		TA2OUT/W			
27	25		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$		
28	26		P7_2		TA1OUT/V	CLK2		
29	27		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM		
30	28		P7_0		TA0OUT	TXD2/SDA2/SDAMM		
31	29		P6_7			TXD1/SDA1		
32	30		P6_6			RXD1/SCL1		
33	31		P6_5			CLK1		
34	32		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/ CLKS1		
35	33		P6_3			$\overline{\text{TXD0}}$/SDA0		
36	34		P6_2			$\overline{\text{RXD0}}$/SCL0		
37	35		P6_1			CLK0		
38	36		P6_0		RTCOUT	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
39	37	CLKOUT	P5_7					$\overline{\text{RDY}}$
40	38		P5_6					ALE
41	39		P5_5					$\overline{\text{HOLD}}$
42	40		P5_4					$\overline{\text{HLDA}}$
43	41		P5_3					BCLK
44	42		P5_2					$\overline{\text{RD}}$
45	43		P5_1					$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
46	44		P5_0					$\overline{\text{WRL}}$/$\overline{\text{WR}}$
47	45		P4_7		PWM1	TXD7/SDA7		$\overline{\text{CS3}}$
48	46		P4_6		PWM0	RXD7/SCL7		$\overline{\text{CS2}}$
49	47		P4_5			CLK7		$\overline{\text{CS1}}$
50	48		P4_4			$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$		$\overline{\text{CS0}}$

Table 1.12 Pin Names, 100-Pin Package (2/2)

Pin No.		Control Pin	Port	I/O Pin for Peripheral Function				Bus Control Pin
FA	FB			Interrupt	Timer	Serial interface	A/D converter, D/A converter	
51	49		P4_3					A19
52	50		P4_2					A18
53	51		P4_1					A17
54	52		P4_0					A16
55	53		P3_7					A15
56	54		P3_6					A14
57	55		P3_5					A13
58	56		P3_4					A12
59	57		P3_3					A11
60	58		P3_2					A10
61	59		P3_1					A9
62	60	VCC2						
63	61		P3_0					A8, [A8/D7]
64	62	VSS						
65	63		P2_7				AN2_7	A7, [A7/D7], [A7/D6]
66	64		P2_6				AN2_6	A6, [A6/D6], [A6/D5]
67	65		P2_5	$\overline{INT7}$			AN2_5	A5, [A5/D5], [A5/D4]
68	66		P2_4	$\overline{INT6}$			AN2_4	A4, [A4/D4], [A4/D3]
69	67		P2_3				AN2_3	A3, [A3/D3], [A3/D2]
70	68		P2_2				AN2_2	A2, [A2/D2], [A2/D1]
71	69		P2_1				AN2_1	A1, [A1/D1], [A1/D0]
72	70		P2_0				AN2_0	A0, [A0/D0], A0
73	71		P1_7	$\overline{INT5}$	IDU			D15
74	72		P1_6	$\overline{INT4}$	IDW			D14
75	73		P1_5	$\overline{INT3}$	IDV			D13
76	74		P1_4					D12
77	75		P1_3			TXD6/SDA6		D11
78	76		P1_2			RXD6/SCL6		D10
79	77		P1_1			CLK6		D9
80	78		P1_0			$\overline{CTS6}/\overline{RTS6}$		D8
81	79		P0_7				AN0_7	D7
82	80		P0_6				AN0_6	D6
83	81		P0_5				AN0_5	D5
84	82		P0_4				AN0_4	D4
85	83		P0_3				AN0_3	D3
86	84		P0_2				AN0_2	D2
87	85		P0_1				AN0_1	D1
88	86		P0_0				AN0_0	D0
89	87		P10_7	$\overline{KI3}$			AN7	
90	88		P10_6	$\overline{KI2}$			AN6	
91	89		P10_5	$\overline{KI1}$			AN5	
92	90		P10_4	$\overline{KI0}$			AN4	
93	91		P10_3				AN3	
94	92		P10_2				AN2	
95	93		P10_1				AN1	
96	94	AVSS						
97	95		P10_0				AN0	
98	96	VREF						
99	97	AVCC						
100	98		P9_7			SIN4	$\overline{ADTRG}$	



Notes:
1. N-channel open drain output.
2. Check the position of Pin 1 by referring to appendix 1, Package Dimensions.

Figure 1.9 Pin Assignment (80 pins) (Top View)

Table 1.13 Pin Names, 80-Pin Package (1/2)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function			
			Interrupt	Timer	Serial interface	A/D converter, D/A converter
1		P9_5			CLK4	ANEX0
2		P9_4		TB4IN/PWM1		DA1
3		P9_3		TB3IN/PWM0		DA0
4		P9_2		TB2IN/PMC0	SOUT3	
5		P9_0		TB0IN	CLK3	
6	CNVSS					
7	XCIN	P8_7				
8	XCOUT	P8_6				
9	$\overline{\text{RESET}}$					
10	XOUT					
11	VSS					
12	XIN					
13	VCC1					
14		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$	CEC	
15		P8_4	$\overline{\text{INT2}}$	ZP		
16		P8_3	$\overline{\text{INT1}}$			
17		P8_2	$\overline{\text{INT0}}$			
18		P8_1		TA4IN	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$	
19		P8_0		TA4OUT	RXD5/SCL5	
20		P7_7		TA3IN	SCL5	
21		P7_6		TA3OUT	TXD5/SDA5	
22		P7_1		TA0IN/TB5IN	RXD2/SCL2/SCLMM	
23		P7_0		TA0OUT	TXD2/SDA2/SDAMM	
24		P6_7			TXD1/SDA1	
25		P6_6			RXD1/SCL1	
26		P6_5			CLK1	
27		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/ CLKS1	
28		P6_3			TXD0/SDA0	
29		P6_2			RXD0/SCL0	
30		P6_1			CLK0	
31		P6_0		RTCOUT	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	
32	CLKOUT	P5_7				
33		P5_6				
34		P5_5				
35		P5_4				
36		P5_3				
37		P5_2				
38		P5_1				
39		P5_0				
40		P4_3				

Table 1.14 Pin Names, 80-Pin Package (2/2)

Pin No.	Control Pin	Port	I/O Pin for Peripheral Function			
			Interrupt	Timer	Serial interface	A/D converter, D/A converter
41		P4_2				
42		P4_1				
43		P4_0				
44		P3_7				
45		P3_6				
46		P3_5				
47		P3_4				
48		P3_3				
49		P3_2				
50		P3_1				
51		P3_0				
52		P2_7				AN2_7
53		P2_6				AN2_6
54		P2_5	$\overline{INT7}$			AN2_5
55		P2_4	$\overline{INT6}$			AN2_4
56		P2_3				AN2_3
57		P2_2				AN2_2
58		P2_1				AN2_1
59		P2_0				AN2_0
60		P0_7				AN0_7
61		P0_6				AN0_6
62		P0_5				AN0_5
63		P0_4				AN0_4
64		P0_3				AN0_3
65		P0_2				AN0_2
66		P0_1				AN0_1
67		P0_0				AN0_0
68		P10_7	$\overline{KI3}$			AN7
69		P10_6	$\overline{KI2}$			AN6
70		P10_5	$\overline{KI1}$			AN5
71		P10_4	$\overline{KI0}$			AN4
72		P10_3				AN3
73		P10_2				AN2
74		P10_1				AN1
75	AVSS					
76		P10_0				AN0
77	VREF					
78	AVCC					
79		P9_7			SIN4	$\overline{ADTRG}$
80		P9_6			SOUT4	ANEX1

1.6 Pin Functions

Table 1.15 Pin Functions (128-Pin Package) (1/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1 VCC2 VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2) and 0 V to the VSS pin. (1)
Analog power supply input	AVCC AVSS	I	VCC1	Apply the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Low active input pin. Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor mode. Connect the CNVSS pin to VSS via a resistor to start up after a reset in single-chip mode. To start up in microprocessor mode, connect it to VCC1.
External data bus width select input	BYTE	I	VCC1	Input pin to select the data bus of the external area. The data bus is 16 bits when it is low and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with separate bus
	D8 to D15	I/O	VCC2	Inputs or outputs data (D8 to D15) while accessing an external area with 16-bit separate bus
	A0 to A19	O	VCC2	Outputs address bits A0 to A19
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with 8-bit multiplexed bus
	A1/D0 to A8/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with 16-bit multiplexed bus
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Low active output pins. Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ by a program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ selected If the external data bus is 16 bits, data is written to an even address in external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ selected Data is written to external area when $\overline{\text{WR}}$ is driven low. Data in external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ for external 8-bit data bus.
	ALE	O	VCC2	Output ALE signal to latch address.
	$\overline{\text{HOLD}}$	I	VCC2	Low active input pin. The MCU is placed in hold state while the $\overline{\text{HOLD}}$ pin is driven low.
	$\overline{\text{HLDA}}$	O	VCC2	Low active output pin. In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	Low active input pin. The MCU bus is placed in wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

Note:
1. VCC1 is hereinafter referred to as VCC unless otherwise noted.

Table 1.16 Pin Functions (128-Pin Package) (2/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Main clock input	XIN	I	VCC1	I/O pins for the main clock oscillator. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (1). To apply an external clock, connect it to XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillator. Connect a crystal oscillator between XCIN and XCOUT (1). To apply an external clock, connect it to XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs BCLK signal
Clock output	CLKOUT	O	VCC2	This pin outputs the clock having the same frequency as fC, f8, or f32.
$\overline{INT}$ interrupt input	$\overline{INT0}$ to $\overline{INT2}$	I	VCC1	Input pins for $\overline{INT}$ interrupt
	$\overline{INT3}$ to $\overline{INT7}$	I	VCC2	
$\overline{NMI}$ interrupt input	$\overline{NMI}$	I	VCC1	Input pin for $\overline{NMI}$ interrupt
Key input interrupt input	$\overline{KI0}$ to $\overline{KI3}$	I	VCC1	Input pins for key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	Timer A0 to A4 I/O pins (TA0OUT as an output pin is N-channel open drain output)
	TA0IN to TA4IN	I	VCC1	Timer A0 to A4 input pins
	ZP	I	VCC1	Input pin for Z-phase
Timer B	TB0IN to TB5IN	I	VCC1	Timer B0 to B5 input pins
Three-phase motor control timer	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	VCC1	Output pins for three-phase motor control timer output
	$\overline{SD}$	I	VCC1	Forced cutoff input
	IDU, IDV, IDW	I	VCC2	Input for position data
Real time clock output	RTCOUT	O	VCC1	Output for real time clock
PWM output	PWM0, PWM1	O	VCC1, VCC2	PWM output
Remote control signal receiver input	PMC0, PMC1	I	VCC1	Input for remote control signal receiver
Serial interface UART0 to UART2, UART5 to UART7	$\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$	I	VCC1	Input pins to control data transmission
	$\overline{CTS6}$, $\overline{CTS7}$	I	VCC2	
	$\overline{RTS0}$ to $\overline{RTS2}$, $\overline{RTS5}$	O	VCC1	Output pins to control data reception
	$\overline{RTS6}$, $\overline{RTS7}$	O	VCC2	
	CLK0 to CLK2, CLK5	I/O	VCC1	Transmit/receive clock I/O pins
	CLK6, CLK7	I/O	VCC2	
	RXD0 to RXD2, RXD5	I	VCC1	Serial data input pins
	RXD6, RXD7	I	VCC2	
	TXD0 to TXD2, TXD5	O	VCC1	Serial data output pins (2)
	TXD6, TXD7	O	VCC2	
	CLKS1	O	VCC1	Output pin for transmit/receive clock multiple-pin output function

Notes:
1. Contact the oscillator manufacturer regarding the oscillation characteristics.
2. TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi (i = 0, 1, 5 to 7), SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins by a program.

Table 1.17 Pin Functions (128-Pin Package) (3/3)

Signal Name	Pin Name	I/O	Power Supply	Description
UART0 to UART2, UART5 to UART7 I^2C mode	SDA0 to SDA2, SDA5	I/O	VCC1	I^2C mode serial data I/O pins
	SDA6, SDA7	I/O	VCC2	
	SCL0 to SCL2, SCL5	I/O	VCC1	I^2C mode transmit/receive clock I/O pins
	SCL6, SCL7	I/O	VCC2	
Serial interface SI/03, SI/04	CLKS3, CLKS4	I/O	VCC1	Transmit/receive clock I/O pins
	SIN3, SIN4	I	VCC1	Serial data input pins
	SOUT3, SOUT4	O	VCC1	Serial data output pins
Multi-master I^2C-bus Interface	SDAMM	I/O	VCC1	Serial data I/O pin (Output is N-channel open drain)
	SCLMM	I/O	VCC1	Transmit/receive clock I/O pin (Output is N-channel open drain)
CEC I/O	CEC	I/O	VCC1	CEC I/O pin (Output is N-channel open drain)
Reference voltage input	VREF	I	VCC1	Reference voltage input pins for the A/D converter and D/A converter
A/D converter	AN0 to AN7	I	VCC1	Analog input pins for the A/D converter
	AN0_0 to AN0_7 AN2_0 to AN2_7	I	VCC2	
	$\overline{\text{ADTRG}}$	I	VCC1	Input pin for an external A/D trigger
	ANEX0, ANEX1	I	VCC1	Extended analog input pin for the A/D converter
D/A converter	DA0, DA1	O	VCC1	Output pin for the D/A converter
I/O port	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7 P12_0 to P12_7 P13_0 to P13_7	I/O	VCC2	8-bit CMOS I/O ports. A direction register determines whether each pin is used as an input port or an output port. A pull-up resistor may be enabled or disabled for input ports in 4-bit units.
	P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_7 P10_0 to P10_7 P11_0 to P11_7	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. However, P7_0, P7_1, and P8_5 are N-channel open drain output ports. No pull-up resistor is provided. P8_5 is an input port for verifying the $\overline{\text{NMI}}$ pin level and shares a pin with $\overline{\text{NMI}}$.
	P14_0, P14_1	I/O	VCC1	I/O ports having equivalent functions to P0

Table 1.18 Pin Functions (100-Pin Package) (1/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1 VCC2 VSS	I	-	Apply 2.7 to 5.5 V to pins VCC1 and VCC2 (VCC1 ≥ VCC2) and 0 V to the VSS pin. (1)
Analog power supply input	AVCC AVSS	I	VCC1	Apply the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Low active input pin. Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor mode. Connect the CNVSS pin to VSS via a resistor to start up after a reset in single-chip mode. To start up in microprocessor mode, connect it to VCC1.
External data bus width select input	BYTE	I	VCC1	Input pin to select the data bus of the external area. The data bus is 16 bits when it is low, and 8 bits when it is high. This pin must be fixed either high or low. Connect the BYTE pin to VSS in single-chip mode.
Bus control pins	D0 to D7	I/O	VCC2	Inputs or outputs data (D0 to D7) while accessing an external area with separate bus
	D8 to D15	I/O	VCC2	Inputs or outputs data (D8 to D15) while accessing an external area with 16-bit separate bus
	A0 to A19	O	VCC2	Outputs address bits A0 to A19
	A0/D0 to A7/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A0 to A7) by timesharing, while accessing an external area with 8-bit multiplexed bus
	A1/D0 to A8/D7	I/O	VCC2	Inputs or outputs data (D0 to D7) and outputs address bits (A1 to A8) by timesharing, while accessing an external area with 16-bit multiplexed bus
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	VCC2	Outputs chip-select signals $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ to specify an external area
	$\overline{\text{WRL}}$/$\overline{\text{WR}}$ $\overline{\text{WRH}}$/$\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	VCC2	Low active output pins. Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$), and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{BHE}}$ and $\overline{\text{WR}}$ by a program. • $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ selected If the external data bus is 16 bits, data is written to an even address in an external area when $\overline{\text{WRL}}$ is driven low. Data is written to an odd address when $\overline{\text{WRH}}$ is driven low. Data is read when $\overline{\text{RD}}$ is driven low. • $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ selected Data is written to external area when $\overline{\text{WR}}$ is driven low. Data in an external area is read when $\overline{\text{RD}}$ is driven low. An odd address is accessed when $\overline{\text{BHE}}$ is driven low. Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$, and $\overline{\text{RD}}$ for external 8-bit data bus.
	ALE	O	VCC2	Outputs ALE signal to latch address.
	$\overline{\text{HOLD}}$	I	VCC2	Low active input pin. The MCU is placed in a hold state while the $\overline{\text{HOLD}}$ pin is driven low.
	$\overline{\text{HLDA}}$	O	VCC2	Low active output pin. In a hold state, $\overline{\text{HLDA}}$ outputs a low-level signal.
	$\overline{\text{RDY}}$	I	VCC2	Low active input pin. The MCU bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is driven low.

Power supply: VCC2 is used to supply power to external bus associated pins. The dual power supply configuration allows VCC2 to interface at a different voltage than VCC1.

Note:
1. VCC1 is hereinafter referred to as VCC unless otherwise noted.

Table 1.19 Pin Functions (100-Pin Package) (2/3)

Signal Name	Pin Name	I/O	Power Supply	Description
Main clock input	XIN	I	VCC1	I/O pins for the main clock oscillator. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (1). To apply an external clock, connect it to XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillator. Connect a crystal oscillator between XCIN and XCOUT (1). To apply an external clock, connect it to XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs BCLK signal
Clock output	CLKOUT	O	VCC2	This pin outputs the clock having the same frequency as fC, f8, or f32.
$\overline{INT}$ interrupt input	$\overline{INT0}$ to $\overline{INT2}$	I	VCC1	Input pins for $\overline{INT}$ interrupt
	$\overline{INT3}$ to $\overline{INT7}$	I	VCC2	
$\overline{NMI}$ interrupt input	$\overline{NMI}$	I	VCC1	Input pin for $\overline{NMI}$ interrupt
Key input interrupt input	$\overline{KI0}$ to $\overline{KI3}$	I	VCC1	Input pins for key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	Timer A0 to A4 I/O pins (TA0OUT as an output pin is N-channel open drain output)
	TA0IN to TA4IN	I	VCC1	Timer A0 to A4 input pins
	ZP	I	VCC1	Input pin for Z-phase
Timer B	TB0IN to TB5IN	I	VCC1	Timer B0 to B5 input pins
Three-phase motor control timer	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	VCC1	Output pins for three-phase motor control timer output
	$\overline{SD}$	I	VCC1	Forced cutoff input
	IDU, IDV, IDW	I	VCC2	Input for position data
Real time clock output	RTCOUT	O	VCC1	Output for real time clock
PWM output	PWM0, PWM1	O	VCC1, VCC2	PWM output
Remote control signal receiver input	PMC0, PMC1	I	VCC1	Input for remote control signal receiver
Serial interface UART0 to UART2, UART5 to UART7	$\overline{CTS0}$ to $\overline{CTS2}$, $\overline{CTS5}$	I	VCC1	Input pins to control data transmission
	$\overline{CTS6}$, $\overline{CTS7}$	I	VCC2	
	$\overline{RTS0}$ to $\overline{RTS2}$, $\overline{RTS5}$	O	VCC1	Output pins to control data reception
	$\overline{RTS6}$, $\overline{RTS7}$	O	VCC2	
	CLK0 to CLK2, CLK5	I/O	VCC1	Transmit/receive clock I/O pins
	CLK6, CLK7	I/O	VCC2	
	RXD0 to RXD2, RXD5	I	VCC1	Serial data input pins
	RXD6, RXD7	I	VCC2	
	TXD0 to TXD2, TXD5	O	VCC1	Serial data output pins (2)
	TXD6, TXD7	O	VCC2	
	CLKS1	O	VCC1	Output pin for transmit/receive clock multiple-pin output function

Notes:
1. Contact the oscillator manufacturer regarding the oscillation characteristics.
2. TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi (i = 0, 1, 5 to 7), SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins by a program.

Table 1.20 Pin Functions (100-Pin Package) (3/3)

Signal Name	Pin Name	I/O	Power Supply	Description
UART0 to UART2, UART5 to UART7 I^2C mode	SDA0 to SDA2, SDA5	I/O	VCC1	I^2C mode serial data I/O pins
	SDA6, SDA7	I/O	VCC2	
	SCL0 to SCL2, SCL5	I/O	VCC1	I^2C mode transmit/receive clock I/O pins
	SCL6, SCL7	I/O	VCC2	
Serial interface SI/03, SI/04	CLKS3, CLKS4	I/O	VCC1	Transmit/receive clock I/O pins
	SIN3, SIN4	I	VCC1	Serial data input pins
	SOUT3, SOUT4	O	VCC1	Serial data output pins
Multi-master I^2C-bus Interface	SDAMM	I/O	VCC1	Serial data I/O pin (output is N-channel open drain)
	SCLMM	I/O	VCC1	Transmit/receive clock I/O pin (output is N-channel open drain)
CEC I/O	CEC	I/O	VCC1	CEC I/O pin (output is N-channel open drain)
Reference voltage input	VREF	I	VCC1	Reference voltage input pins for the A/D converter and D/A converter
A/D converter	AN0 to AN7	I	VCC1	Analog input pins for the A/D converter
	AN0_0 to AN0_7 AN2_0 to AN2_7	I	VCC2	
	$\overline{\text{ADTRG}}$	I	VCC1	Input pin for an external A/D trigger
	ANEX0, ANEX1	I	VCC1	Extended analog input pin for the A/D converter
D/A converter	DA0, DA1	O	VCC1	Output pin for the D/A converter
I/O port	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7	I/O	VCC2	8-bit CMOS I/O ports. A direction register determines whether each pin is used as an input port or an output port. A pull-up resistor may be enabled or disabled for input ports in 4-bit units.
	P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_7 P10_0 to P10_7	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. However, P7_0, P7_1, and P8_5 are N-channel open drain output ports. No pull-up resistor is provided. P8_5 is an input port for verifying the $\overline{\text{NMI}}$ pin level and shares a pin with $\overline{\text{NMI}}$.

Table 1.21 Pin Functions (80-Pin Package) (1/2)

Signal Name	Pin Name	I/O	Power Supply	Description
Power supply input	VCC1 VSS	I	-	Apply 2.7 to 5.5 V to the VCC1 pin and 0 V to the VSS pin.
Analog power supply input	AVCC AVSS	I	VCC1	Apply the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	$\overline{\text{RESET}}$	I	VCC1	Low active input pin. Driving this pin low resets the MCU.
CNVSS	CNVSS	I	VCC1	Input pin to switch processor mode. Connect the CNVSS pin to VSS via a resistor to start up after a reset in single-chip mode.
Main clock input	XIN	I	VCC1	I/O pins for the main clock oscillator. Connect a ceramic resonator or crystal oscillator between XIN and XOUT (1). To apply an external clock, connect it to XIN and leave XOUT open.
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillator. Connect a crystal oscillator between XCIN and XCOUT (1). To apply an external clock, connect it to XCIN and leave XCOUT open.
Sub clock output	XCOUT	O	VCC1	
Clock output	CLKOUT	O	VCC1	This pin outputs the clock having the same frequency as fC, f8, or f32.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input pins for $\overline{\text{INT}}$ interrupt
	$\overline{\text{INT6}}$, $\overline{\text{INT7}}$	I	VCC1	
$\overline{\text{NMI}}$ interrupt input	$\overline{\text{NMI}}$	I	VCC1	Input pin for $\overline{\text{NMI}}$ interrupt
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input pins for key input interrupt
Timer A	TA0OUT TA3OUT TA4OUT	I/O	VCC1	Timer A0, timer A3, timer A4 I/O pins (TA0OUT as an output pin is N-channel open drain output)
	TA0IN, TA3IN, TA4IN	I	VCC1	Timer A0, timer A3, timer A4 input pins
	ZP	I	VCC1	Input pin for Z-phase
Timer B	TB0IN, TB2IN to TB5IN	I	VCC1	Timer B0, timers B2 to B5 input pins
Real time clock output	RTCOUT	O	VCC1	Output for real time clock
PWM output	PWM0, PWM1	O	VCC1	PWM output
Remote control signal receiver input	PMC0	I	VCC1	Input for remote control signal receiver

Note:
1. Contact the oscillator manufacturer regarding oscillation characteristics.

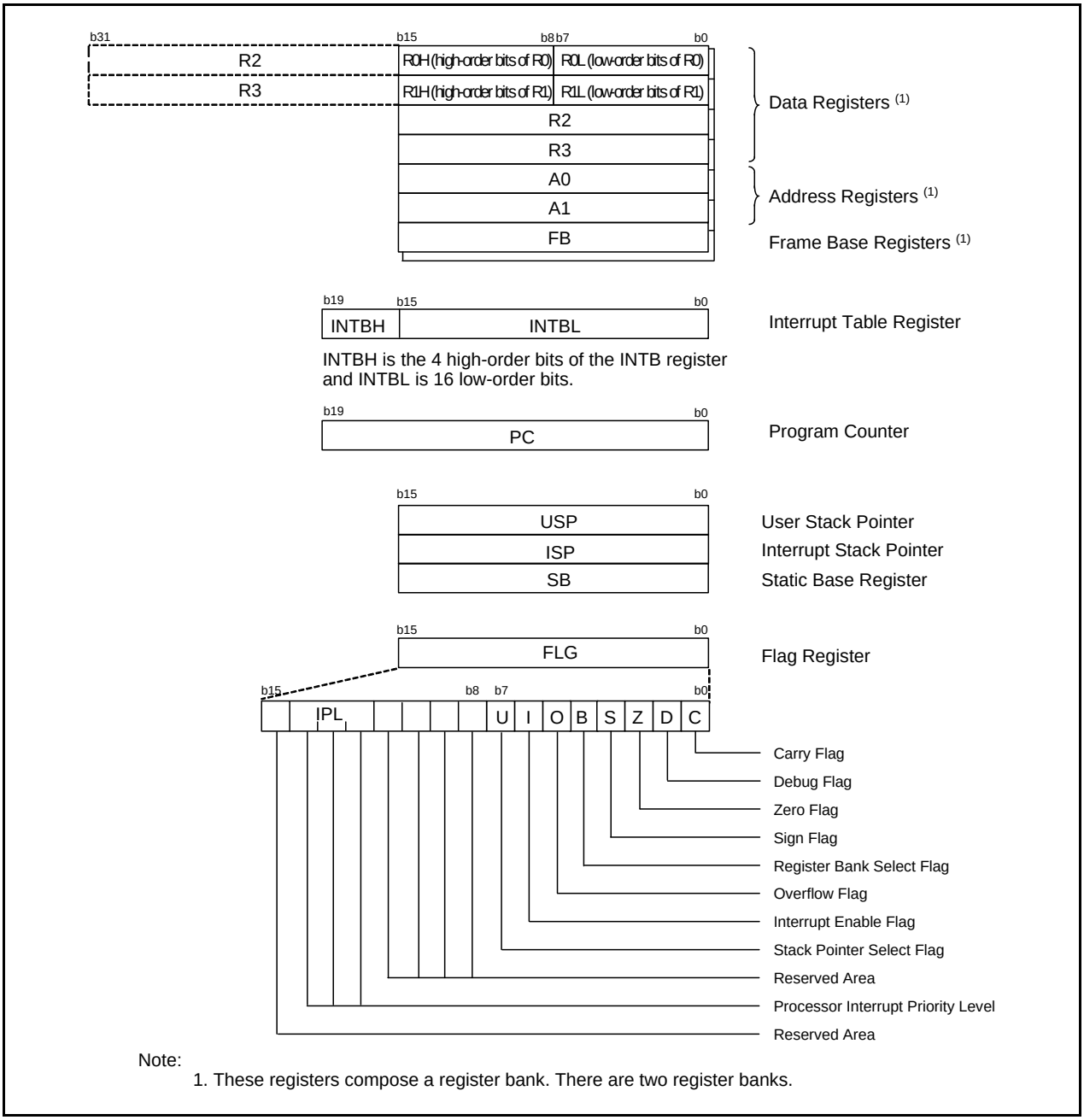
Table 1.22 Pin Functions (80-Pin Package) (2/2)

Signal Name	Pin Name	I/O	Power Supply	Description
Serial interface UART0 to UART2, UART5	$\overline{CTS0}$, $\overline{CTS1}$, $\overline{CTS5}$	I	VCC1	Input pins to control data transmission
	$\overline{RTS0}$, $\overline{RTS1}$, $\overline{RTS5}$	O	VCC1	Output pins to control data reception
	CLK0, CLK1, CLK5	I/O	VCC1	Transmit/receive clock I/O pins
	RXD0 to RXD2, RXD5	I	VCC1	Serial data input pins
	TXD0 to TXD2, TXD5	O	VCC1	Serial data output pins (1)
	CLKS1	O	VCC1	Output pin for transmit/receive clock multiple-pin output function
UART0 to UART2, UART5 I^2C mode	SDA0 to SDA2, SDA5	I/O	VCC1	I^2C mode serial data I/O pins
	SCL0 to SCL2, SCL5	I/O	VCC1	I^2C mode transmit/receive clock I/O pins
Serial interface SI/03, SI/04	CLKS3, CLKS4	I/O	VCC1	Transmit/receive clock I/O pins
	SIN4	I	VCC1	Serial data input pins
	SOUT3, SOUT4	O	VCC1	Serial data output pins
Multi-master I^2C-bus Interface	SDAMM	I/O	VCC1	Serial data I/O pin (output is N-channel open drain)
	SCLMM	I/O	VCC1	Transmit/receive clock I/O pin (output is N-channel open drain)
CEC I/O	CEC	I/O	VCC1	CEC I/O pin (output is N-channel open drain)
Reference voltage input	VREF	I	VCC1	Reference voltage input pins for the A/D converter and D/A converter
A/D converter	AN0 to AN7	I	VCC1	Analog input pins for the A/D converter
	AN0_0 to AN0_7 AN2_0 to AN2_7	I	VCC1	
	$\overline{ADTRG}$	I	VCC1	Input pin for an external A/D trigger
	ANEX0, ANEX1	I	VCC1	Extended analog input pin for the A/D converter
D/A converter	DA0, DA1	O	VCC1	Output pin for the D/A converter
I/O port	P0_0 to P0_7 P2_0 to P2_7 P3_0 to P3_7 P5_0 to P5_7 P6_0 to P6_7 P8_0 to P8_7 P10_0 to P10_7	I/O	VCC1	8-bit CMOS I/O ports. A direction register determines whether each pin is used as an input port or an output port. A pull-up resistor may be enabled or disabled for input ports in 4-bit units. P8_5 is an N-channel open drain output port. No pull-up resistor is provided. P8_5 is an input port for verifying the $\overline{NMI}$ pin level and shares a pin with $\overline{NMI}$.
	P4_0 to P4_3 P7_0, P7_1 P7_6, P7_7 P9_0, P9_2 to P9_7	I/O	VCC1	I/O ports having equivalent functions to P0. However, P7_0 and P7_1 are N-channel open drain output ports. No pull-up resistor is provided.

Note:
1. TXD2, SDA2, and SCL2 are N-channel open drain output pins. TXDi (i = 0, 1, 5), SDAi, and SCLi can be selected as CMOS output pins or N-channel open drain output pins by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. Seven registers (R0, R1, R2, R3, A0, A1, and FB) out of thirteen compose a register bank. There are two sets of register banks.



Note:
1. These registers compose a register bank. There are two register banks.

Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers used for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order (R0H/R1H) and low-order (R0L/R1L) bits to be used separately as 8-bit data registers. R0 can be combined with R2 and used as a 32-bit data register (R2R0). Also, R3R1 is the combination of R3 and R1.

2.2 Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for indirect addressing, relative addressing, transfer, arithmetic and logic operations. A0 can be combined with A1 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

The FB is a 16-bit register that is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

The INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

The PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP are each comprised of 16 bits. The U flag is used to switch between USP and ISP.

2.7 Static Base Register (SB)

The SB is a 16-bit register used for SB-relative addressing.

2.8 Flag Register (FLG)

The FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C Flag)

The C flag retains a carry, borrow, or shift-out bit generated by the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z Flag)

The Z flag becomes 1 when an arithmetic operation results in 0. Otherwise it becomes 0.

2.8.4 Sign Flag (S Flag)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when the B flag is set to 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O Flag)

The O flag is set to 1 when an arithmetic operation results in an overflow. Otherwise it is set to 0.

2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables maskable interrupts.
Maskable interrupts are disabled when the I flag is set to 0, and enabled when it is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is set to 0. USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt number 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

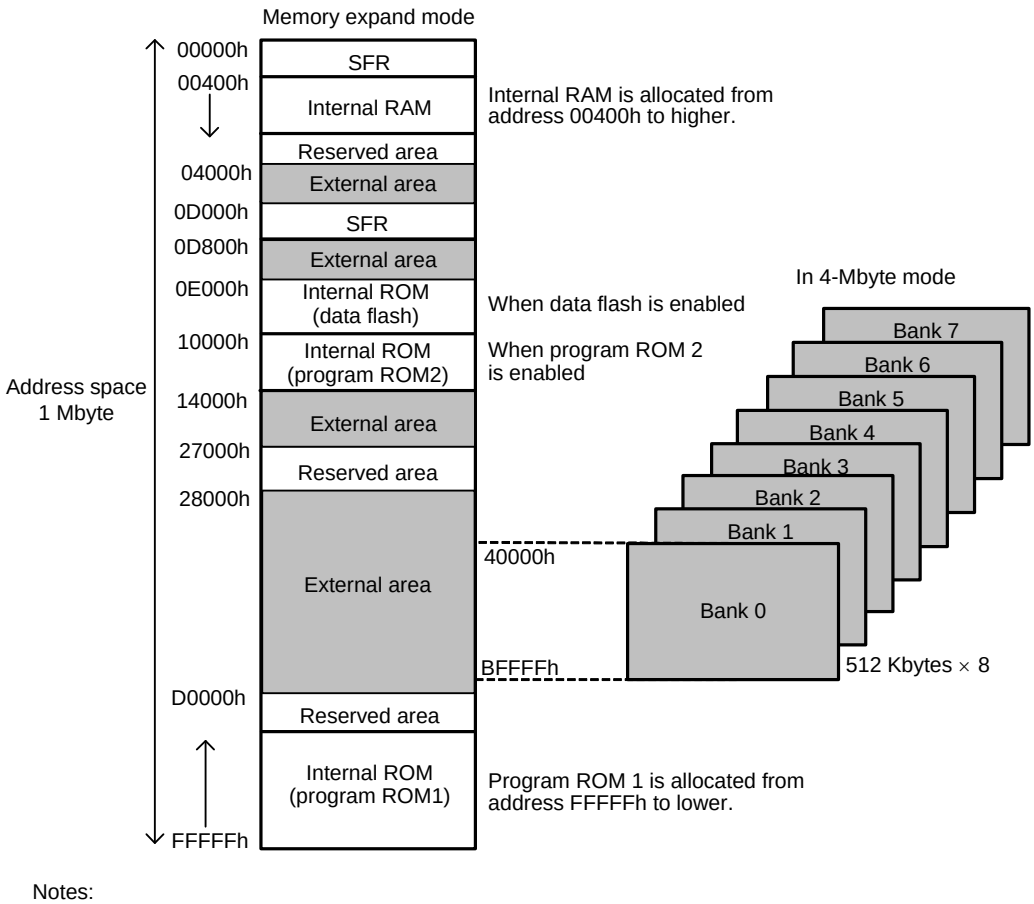
2.8.10 Reserved Space

Only write 0 to bits assigned as reserved bits. The read value is undefined.

3. Address Space

3.1 Address Space

The M16C/65 Group has a 1 Mbyte address space from address 00000h to FFFFFh. Address space is expandable to 4 Mbytes with the memory capacity-enhancing feature. Address 40000h to BFFFFh can be used as external areas from bank 0 to bank 7. Figure 3.1 shows Address Space. The accessible area depends on processor mode and control bit status.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following conditions:
   - The PM13 bit in the PM1 register is set to 0
     (addresses from 04000h to 0CFFFh and from 80000h to CFFFFh are used as external areas)
   - The IRON bit in the PRG2C register is set to 0
     (addresses from 40000h to 7FFFFh are used as an external area)

Figure 3.1 Address Space

3.2 Memory Map

Special Function Registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank spaces within SFRs are reserved, and should not be accessed by the user.

Internal RAM is allocated from address 00400h and higher, with 10 Kbytes of internal RAM addressed from 00400h to 02BFFh. Internal RAM is used not only for data storage, but also for the stack area when subroutines are called or when an interrupt request is acknowledged.

The internal ROM is flash memory. Three internal ROM areas are available: data flash, program ROM 1, and program ROM 2.

The data flash is addressed from 0E000h to 0FFFFh. This data flash space is used not only for data storage, but also for program storage.

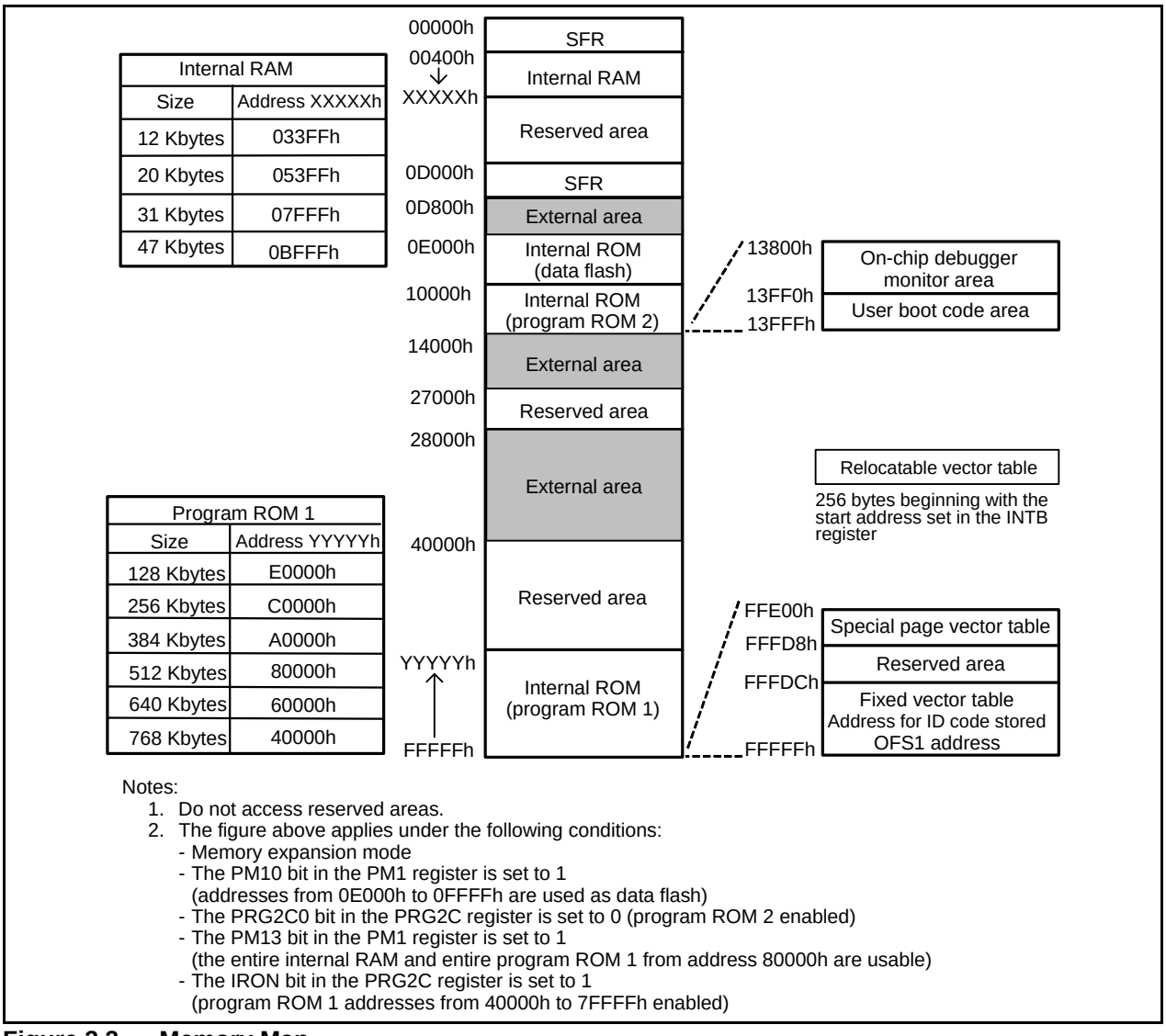
Program ROM 2 is assigned addresses 10000h to 13FFFh. Program ROM 1 is assigned addresses FFFFFh and lower, with the 64-Kbyte program ROM 1 space addressed to F0000h to FFFFFh.

The special page vectors are assigned addresses FFE00h to FFFD7h. They are used for the JMPS instruction and JSRS instruction. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts is assigned addresses FFFDCh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.

Figure 3.2 shows the Memory Map.

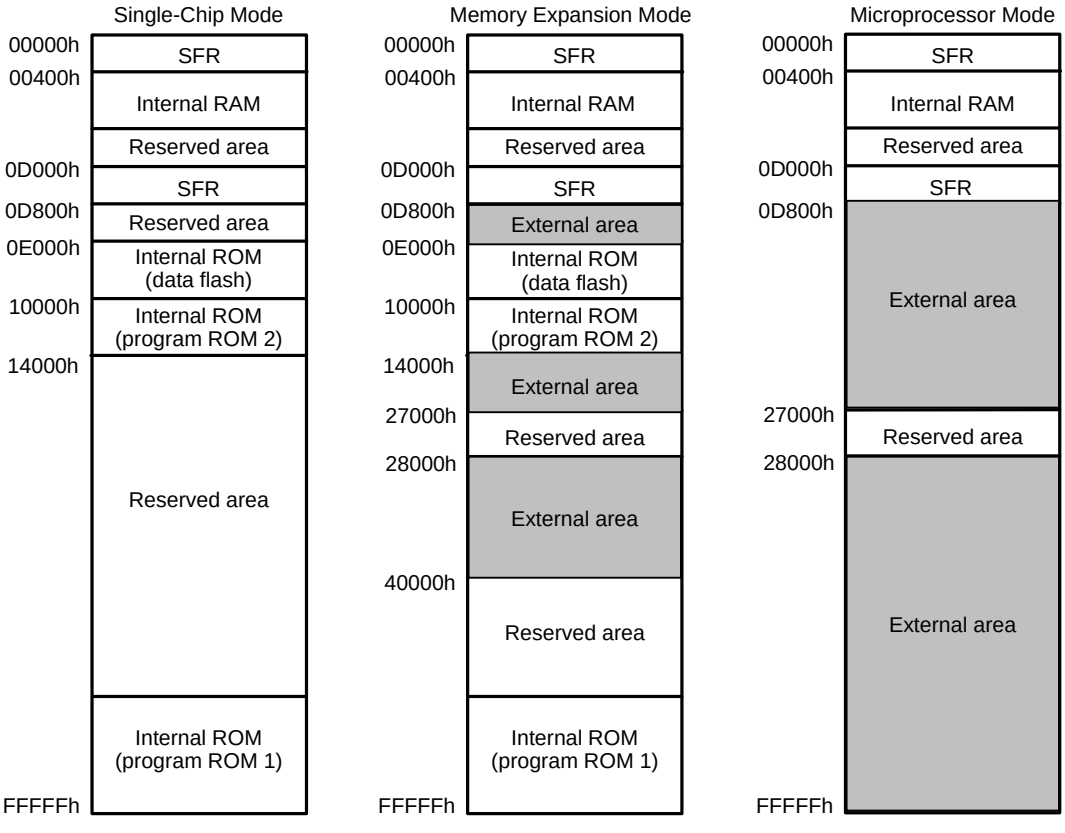


Notes:
1. Do not access reserved areas.
2. The figure above applies under the following conditions:
   - Memory expansion mode
   - The PM10 bit in the PM1 register is set to 1
     (addresses from 0E000h to 0FFFFh are used as data flash)
   - The PRG2C0 bit in the PRG2C register is set to 0 (program ROM 2 enabled)
   - The PM13 bit in the PM1 register is set to 1
     (the entire internal RAM and entire program ROM 1 from address 80000h are usable)
   - The IRON bit in the PRG2C register is set to 1
     (program ROM 1 addresses from 40000h to 7FFFFh enabled)

Figure 3.2 Memory Map

3.3 Accessible Area in Each Mode

The accessible area varies depending on processor mode and control bit status. Figure 3.3 shows Accessible Area in Each Mode.
In single-chip mode, the SFRs, internal RAM, and internal ROM can be accessed.
In memory expansion mode, the SFRs, internal RAM, internal ROM, and external areas can be accessed. Address space is expandable to 4 Mbytes with the memory capacity-enhancing feature.
In microprocessor mode, the SFRs, internal RAM, and external areas can be accessed. Address space is expandable to 4 Mbytes with the memory capacity-enhancing feature. Assign ROM to the fixed vector table addresses from FFFDCh to FFFFFh.



Notes:
1. Do not access reserved areas.
2. The figure above applies under the following conditions:
   Single-chip mode and memory expansion mode
   - The PM10 bit in the PM1 register is set to 1
     (addresses from 0E000h to 0FFFFh are used as data flash)
   - The PRG2C0 bit in the PRG2C register is set to 0 (program ROM 2 enabled)
   - The PM13 bit in the PM1 register is set to 1
     (the entire internal RAM and entire program ROM 1 from address 80000h are usable)
   - The IRON bit in the PRG2C register is set to 1
     (program ROM 1 addresses from 40000h to 7FFFFh enabled)

   Microprocessor mode
   - The PM10 bit is set to 0 (addresses from 0E000h to 0FFFFh are used as $\overline{CS2}$ area)
   - The PRG2C0 bit is set to 1 (program ROM 2 disabled)

Figure 3.3 Accessible Area in Each Mode

4. Special Function Registers (SFRs)

4.1 SFRs

An SFR is a control register for a peripheral function. Table 4.1 to Table 4.15 list SFR information.

Table 4.1 SFR Information (1/16) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	0000 0000b (CNVSS pin is low) 0000 0011b (CNVSS pin is high) (2)
0005h	Processor Mode Register 1	PM1	0000 1000b
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h	Chip Select Control Register	CSR	01h
0009h	External Area Recovery Cycle Control Register	EWR	XXXX XX00b
000Ah	Protect Register	PRCR	00h
000Bh	Data Bank Register	DBR	00h
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b (3)
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0011h	External Area Wait Control Expansion Register	EWC	00h
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0013h			
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	XX00 001Xb (hardware reset) (4)
0019h	Voltage Detection 2 Circuit Flag Register	VCR1	0000 X000b (2)
001Ah	Voltage Detection Circuit Operation Enable Register	VCR2	000X 0000b (2), (5) 001X 0000b (2), (6)
001Bh	Chip Select Expansion Control Register	CSE	00h
001Ch	PLL Control Register 0	PLC0	0X01 X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
001Fh			

Notes: X: Undefined

1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillation stop detection reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect the following bits: Bits PM01 and PM00 in the PM0 register, VCR1 register, and VCR2 register.
3. Oscillation stop detection reset does not affect bits CM20, CM21, and CM27.
4. The state of bits in the RSTFR register depends on a reset type.
5. When the LVDAS bit of address OFS1 is 1 at hardware reset
6. This value shows the value after any of the following resets.
   - Voltage monitor 0 reset
   - When the LVDAS bit of address OFS1 is 0 at hardware reset
   - Power-on reset

Table 4.2 SFR Information (2/16) (1)

Address	Register	Symbol	After Reset
0020h			
0021h			
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	XXXX XX00b
0023h			
0024h			
0025h			
0026h	Voltage Monitor Function Select Register	VWCE	00h (5)
0027h			
0028h	Voltage Detection 1 Level Select Register	VD1LS	0000 1010b (5)
0029h			
002Ah	Voltage Monitor 0 Circuit Control Register	VW0C	1100 1X10b (2), (3) 1100 1X11b (2), (4)
002Bh	Voltage Monitor 1 Circuit Control Register	VW1C	1000 XX10b (6)
002Ch	Voltage Monitor 2 Circuit Control Register	VW2C	1000 0X10b (6)
002Dh			
002Eh			
002Fh			
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h			
0042h	$\overline{\text{INT7}}$ Interrupt Control Register	INT7IC	XX00 X000b
0043h	$\overline{\text{INT6}}$ Interrupt Control Register	INT6IC	XX00 X000b
0044h	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register UART0 Bus Collision Detection Interrupt Control Register	TB3IC U0BCNIC	XXXX X000b
0048h	SI/O4 Interrupt Control Register $\overline{\text{INT5}}$ Interrupt Control Register	S4IC INT5IC	XX00 X000b
0049h	SI/O3 Interrupt Control Register $\overline{\text{INT4}}$ Interrupt Control Register	S3IC INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b

Notes: X: Undefined

1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillation stop detection reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect the following register or bit: VW0C register and VW2C3 bit in the VW2C register.
3. When the LVDAS bit of address OFS1 is 1 at hardware reset
4. This value shows the value after any of the following resets.
   - Voltage monitor 0 reset
   - When the LVDAS bit of address OFS1 is 0 at hardware reset
   - Power-on reset
5. Hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 1 reset, or voltage monitor 2 reset
6. Hardware reset, power-on reset, or voltage monitor 0 reset

Table 4.3 SFR Information (3/16) (1)

Address	Register	Symbol	After Reset
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register CEC1 Interrupt Control Register	U5BCNIC CEC1IC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register CEC2 Interrupt Control Register	S5TIC, CEC2IC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b
006Eh	UART6 Bus Collision Detection Interrupt Control Register Real-Time Clock Period Interrupt Control Register	U6BCNIC RTCTIC	XXXX X000b
006Fh	UART6 Transmit Interrupt Control Register Real-Time Clock Compare Match Interrupt Control Register	S6TIC RTCCIC	XXXX X000b
0070h	UART6 Receive Interrupt Control Register	S6RIC	XXXX X000b
0071h	UART7 Bus Collision Detection Interrupt Control Register Remote Control Signal Receiver 0 Interrupt Control Register	U7BCNIC PMC0IC	XXXX X000b
0072h	UART7 Transmit Interrupt Control Register Remote Control Signal Receiver 1 Interrupt Control Register	S7TIC PMC1IC	XXXX X000b
0073h	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh	IICBus Interface Interrupt Control Register	IICIC	XXXX X000b
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	XXXX X000b
007Dh			
007Eh			
007Fh			
0080h to 017Fh			

Note: X: Undefined
1. The blank areas are reserved. No access is allowed.

Table 4.4 SFR Information (4/16) (1)

Address	Register	Symbol	After Reset
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0183h			
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0187h			
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0193h			
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0197h			
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01ADh			
01AEh			
01AFh			

Note: X: Undefined

1. The blank areas are reserved. No access is allowed.

Table 4.5 SFR Information (5/16) (1)

Address	Register	Symbol	After Reset
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-Bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

Note: X: Undefined

1. The blank areas are reserved. No access is allowed.

Table 4.6 SFR Information (6/16) (1)

Address	Register	Symbol	After Reset
01E0h	Timer B3-1 Register	TB31	XXh
01E1h			XXh
01E2h	Timer B4-1 Register	TB41	XXh
01E3h			XXh
01E4h	Timer B5-1 Register	TB51	XXh
01E5h			XXh
01E6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 2	PPWFS2	XXXX X000b
01E7h			
01E8h	Timer B Count Source Select Register 2	TBCS2	00h
01E9h	Timer B Count Source Select Register 3	TBCS3	X0h
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	PMC0 Function Select Register 0	PMC0CON0	00h
01F1h	PMC0 Function Select Register 1	PMC0CON1	00XX 0000b
01F2h	PMC0 Function Select Register 2	PMC0CON2	00h
01F3h	PMC0 Function Select Register 3	PMC0CON3	00h
01F4h	PMC0 Status Register	PMC0STS	00h
01F5h	PMC0 Interrupt Source Select Register	PMC0INT	00h
01F6h	PMC0 Compare Control Register	PMC0CPC	XXX0 X000b
01F7h	PMC0 Compare Data Register	PMC0CPD	00h
01F8h	PMC1 Function Select Register 0	PMC1CON0	XXX0 X000b
01F9h	PMC1 Function Select Register 1	PMC1CON1	XXXX 0X00b
01FAh	PMC1 Function Select Register 2	PMC1CON2	00h
01FBh	PMC1 Function Select Register 3	PMC1CON3	00h
01FCh	PMC1 Status Register	PMC1STS	X000 X00Xb
01FDh	PMC1 Interrupt Source Select Register	PMC1INT	X000 X00Xb
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b

Note: X: Undefined

1. The blank areas are reserved. No access is allowed.

Table 4.7 SFR Information (7/16) (1)

Address	Register	Symbol	After Reset
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h	Flash Memory Control Register 3	FMR3	XXXX 0000b
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

Note: X: Undefined
1. The blank areas are reserved. No access is allowed.

Table 4.8 SFR Information (8/16) (1)

Address	Register	Symbol	After Reset
0240h			
0241h			
0242h			
0243h			
0244h	UART0 Special Mode Register 4	U0SMR4	00h
0245h	UART0 Special Mode Register 3	U0SMR3	000X 0X0Xb
0246h	UART0 Special Mode Register 2	U0SMR2	X000 0000b
0247h	UART0 Special Mode Register	U0SMR	X000 0000b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	00XX 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h	UART Transmit/Receive Control Register 2	UCON	X000 0000b
0251h			
0252h	UART Clock Select Register	UCLKSEL0	X0h
0253h			
0254h	UART1 Special Mode Register 4	U1SMR4	00h
0255h	UART1 Special Mode Register 3	U1SMR3	000X 0X0Xb
0256h	UART1 Special Mode Register 2	U1SMR2	X000 0000b
0257h	UART1 Special Mode Register	U1SMR	X000 0000b
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	00XX 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

Note: X: Undefined

1. The blank areas are reserved. No access is allowed.

Table 4.9 SFR Information (9/16) (1)

Address	Register	Symbol	After Reset
0270h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0271h			
0272h	SI/O3 Control Register	S3C	0100 0000b
0273h	SI/O3 Bit Rate Register	S3BRG	XXh
0274h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0275h			
0276h	SI/O4 Control Register	S4C	0100 0000b
0277h	SI/O4 Bit Rate Register	S4BRG	XXh
0278h	SI/O3, 4 Control Register 2	S34C2	00XX X0X0b
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h	UART5 Special Mode Register 4	U5SMR4	00h
0285h	UART5 Special Mode Register 3	U5SMR3	000X 0X0Xb
0286h	UART5 Special Mode Register 2	U5SMR2	X000 0000b
0287h	UART5 Special Mode Register	U5SMR	X000 0000b
0288h	UART5 Transmit/Receive Mode Register	U5MR	00h
0289h	UART5 Bit Rate Register	U5BRG	XXh
028Ah	UART5 Transmit Buffer Register	U5TB	XXh
028Bh			XXh
028Ch	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
028Dh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
028Eh	UART5 Receive Buffer Register	U5RB	XXh
028Fh			XXh
0290h			
0291h			
0292h			
0293h			
0294h	UART6 Special Mode Register 4	U6SMR4	00h
0295h	UART6 Special Mode Register 3	U6SMR3	000X 0X0Xb
0296h	UART6 Special Mode Register 2	U6SMR2	X000 0000b
0297h	UART6 Special Mode Register	U6SMR	X000 0000b
0298h	UART6 Transmit/Receive Mode Register	U6MR	00h
0299h	UART6 Bit Rate Register	U6BRG	XXh
029Ah	UART6 Transmit Buffer Register	U6TB	XXh
029Bh			XXh
029Ch	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
029Dh	UART6 Transmit/Receive Control Register 1	U6C1	0000 0010b
029Eh	UART6 Receive Buffer Register	U6RB	XXh
029Fh			XXh

Note: X: Undefined

1. The blank areas are reserved. No access is allowed.

Table 4.10 SFR Information (10/16) (1)

Address	Register	Symbol	After Reset
02A0h			
02A1h			
02A2h			
02A3h			
02A4h	UART7 Special Mode Register 4	U7SMR4	00h
02A5h	UART7 Special Mode Register 3	U7SMR3	000X 0X0Xb
02A6h	UART7 Special Mode Register 2	U7SMR2	X000 0000b
02A7h	UART7 Special Mode Register	U7SMR	X000 0000b
02A8h	UART7 Transmit/Receive Mode Register	U7MR	00h
02A9h	UART7 Bit Rate Register	U7BRG	XXh
02AAh	UART7 Transmit Buffer Register	U7TB	XXh
02ABh			XXh
02ACh	UART7 Transmit/Receive Control Register 0	U7C0	0000 1000b
02ADh	UART7 Transmit/Receive Control Register 1	U7C1	0000 0010b
02AEh	UART7 Receive Buffer Register	U7RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	00h
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h to 02FFh			
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	000X XXXXb
0301h			
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
030Fh			

Note: X: Undefined
1. The blank areas are reserved. No access is allowed.

Table 4.11 SFR Information (11/16) (1)

Address	Register	Symbol	After Reset
0310h	Timer B3 Register	TB3	XXh
0311h			XXh
0312h	Timer B4 Register	TB4	XXh
0313h			XXh
0314h	Timer B5 Register	TB5	XXh
0315h			XXh
0316h			
0317h			
0318h	Port Function Control Register	PFCR	0011 1111b
0319h			
031Ah			
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	00h
0321h			
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Up/Down Flag	UDF	00h
0325h			
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh
0330h	Timer B0 Register	TB0	XXh
0331h			XXh
0332h	Timer B1 Register	TB1	XXh
0333h			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
033Eh	Timer B2 Special Mode Register	TB2SC	XXXX XX00b
033Fh			

Note: X: Undefined

1. The blank areas are reserved. No access is allowed.

Table 4.12 SFR Information (12/16) (1)

Address	Register	Symbol	After Reset
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h	CEC Function Control Register 1	CECC1	XXXX X000b
0351h	CEC Function Control Register 2	CECC2	00h
0352h	CEC Function Control Register 3	CECC3	XXXX 0000b
0353h	CEC Function Control Register 4	CECC4	00h
0354h	CEC Flag Register	CECFLG	00h
0355h	CEC Interrupt Source Select Register	CISEL	00h
0356h	CEC Transmit Buffer Register 1	CCTB1	00h
0357h	CEC Transmit Buffer Register 2	CCTB2	XXXX XX00b
0358h	CEC Receive Buffer Register 1	CCRB1	00h
0359h	CEC Receive Buffer Register 2	CCRB2	XXXX X000b
035Ah	CEC Receive Follower Address Set Register 1	CRADRI1	00h
035Bh	CEC Receive Follower Address Set Register 2	CRADRI2	00h
035Ch			
035Dh			
035Eh			
035Fh			
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	0000 0000b (2) 0000 0010b
0362h	Pull-Up Control Register 2	PUR2	00h
0363h	Pull-Up Control Register 3	PUR3	00h
0364h			
0365h			
0366h	Port Control Register	PCR	0000 0XX0b
0367h			
0368h			
0369h	NMI/SD Digital Filter Register	NMIDF	XXXX X000b
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			

Notes: X: Undefined

1. The blank areas are reserved. No access is allowed.
2. Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:
   - 00000000b when a low-level signal is input to the CNVSS pin
   - 00000010b when a high-level signal is input to the CNVSS pin

   Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, or oscillation stop detection reset are as follows:
   - 00000000b when bits PM01 and PM00 in the PM0 register are 00b (single-chip mode).
   - 00000010b when bits PM01 and PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).

Table 4.13 SFR Information (13/16) (1)

Address	Register	Symbol	After Reset
0370h	PWM Control Register 0	PWMCON0	00h
0371h			
0372h	PWM0 Prescaler	PWMPRE0	00h
0373h	PWM0 Register	PWMREG0	00h
0374h	PWM1 Prescaler	PWMPRE1	00h
0375h	PWM1 Register	PWMREG1	00h
0376h	PWM Control Register 1	PWMCON1	00h
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h (2)
037Dh	Watchdog Timer Reset Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h			
0381h			
0382h			
0383h			
0384h			
0385h			
0386h			
0387h			
0388h			
0389h			
038Ah			
038Bh			
038Ch			
038Dh			
038Eh			
038Fh			
0390h	DMA2 Source Select Register	DM2SL	00h
0391h			
0392h	DMA3 Source Select Register	DM3SL	00h
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	00h
0399h			
039Ah	DMA1 Source Select Register	DM1SL	00h
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			

Notes:
X: Undefined

1. The blank areas are reserved. No access is allowed.
2. When the CSPROINT bit in the OFS1 address is 0, value after reset is 10000000b

Table 4.14 SFR Information (14/16) (1)

Address	Register	Symbol	After Reset
03A0h			
03A1h			
03A2h	Open-Circuit Detection Assist Function Register	AINRST	XX00 0000b
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb

Note: X: Undefined

1. The blank areas are reserved. No access is allowed.

Table 4.15 SFR Information (15/16) (1)

Address	Register	Symbol	After Reset
03D0h			
03D1h			
03D2h			
03D3h			
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D5h			
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b
03D8h	D/A0 Register	DA0	00h
03D9h			
03DAh	D/A1 Register	DA1	00h
03DBh			
03DCh	D/A Control Register	DACON	00h
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register	PD11	00h
03F8h	Port P12 Register	P12	XXh
03F9h	Port P13 Register	P13	XXh
03FAh	Port P12 Direction Register	PD12	00h
03FBh	Port P13 Direction Register	PD13	00h
03FCh	Port P14 Register	P14	XXh
03FDh			
03FEh	Port P14 Direction Register	PD14	XXXX XX00b
03FFh			
0400h to D07Fh			

Note: X: Undefined
1. The blank areas are reserved. No access is allowed.

Table 4.16 SFR Information (16/16) (1)

Address	Register	Symbol	After Reset
D080h	PMC0 Header Pattern Set Register (Min)	PMC0HDPMIN	00h
D081h			XXXX X000b
D082h	PMC0 Header Pattern Set Register (Max)	PMC0HDPMAX	00h
D083h			XXXX X000b
D084h	PMC0 Data0 Pattern Set Register (Min)	PMC0D0PMIN	00h
D085h	PMC0 Data0 Pattern Set Register (Max)	PMC0D0PMAX	00h
D086h	PMC0 Data1 Pattern Set Register (Min)	PMC0D1PMIN	00h
D087h	PMC0 Data1 Pattern Set Register (Max)	PMC0D1PMAX	00h
D088h	PMC0 Measurements Register	PMC0TIM	0000h
D089h			
D08Ah	PMC0 Counter Value Register	PMC0BC	0000h
D08Bh			
D08Ch	PMC0 Receive Data Store Register 0	PMC0DAT0	00h
D08Dh	PMC0 Receive Data Store Register 1	PMC0DAT1	00h
D08Eh	PMC0 Receive Data Store Register 2	PMC0DAT2	00h
D08Fh	PMC0 Receive Data Store Register 3	PMC0DAT3	00h
D090h	PMC0 Receive Data Store Register 4	PMC0DAT4	00h
D091h	PMC0 Receive Data Store Register 5	PMC0DAT5	00h
D092h	PMC0 Receive Bit Count Register	PMC0RBIT	XX00 0000b
D093h			
D094h	PMC1 Hedder Pattern Set Register (Min)	PMC1HDPMIN	00h
D095h			XXXX X000b
D096h	PMC1 Header Pattern Set Register (Max)	PMC1HDPMAX	00h
D097h			XXXX X000b
D098h	PMC1 Data0 Pattern Set Register (Min)	PMC1D0PMIN	00h
D099h	PMC1 Data0 Pattern Set Register (Max)	PMC1D0PMAX	00h
D09Ah	PMC1 Data1 Pattern Set Register (Min)	PMC1D1PMIN	00h
D09Bh	PMC1 Data1 Pattern Set Register (Max)	PMC1D1PMAX	00h
D09Ch	PMC1 Measurements Register	PMC1TIM	00h
D09Dh			00h
D09Eh	PMC1 Counter Value Register	PMC1BC	00h
D09Fh			00h

Note: X: Undefined
1. The blank areas are reserved. No access is allowed.

4.2 Notes on SFRs

4.2.1 Register Settings

Table 4.17 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.

Table 4.17 Registers with Write-Only Bits

Register	Symbol	Address
Watchdog Timer Reset Register	WDTR	037Dh
Watchdog Timer Start Register	WDTS	037Eh
Timer A0 Register	TA0	0327h to 0326h
Timer A1 Register	TA1	0329h to 0328h
Timer A2 Register	TA2	032Bh to 032Ah
Timer A3 Register	TA3	032Dh to 032Ch
Timer A4 Register	TA4	032Fh to 032Eh
Timer A1-1 Register	TA11	0303h to 0302h
Timer A2-1 Register	TA21	0305h to 0304h
Timer A4-1 Register	TA41	0307h to 0306h
Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
Dead Time Timer	DTT	030Ch
Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	030Dh
UART0 Bit Rate Register	U0BRG	0249h
UART1 Bit Rate Register	U1BRG	0259h
UART2 Bit Rate Register	U2BRG	0269h
UART5 Bit Rate Register	U5BRG	0289h
UART6 Bit Rate Register	U6BRG	0299h
UART7 Bit Rate Register	U7BRG	02A9h
UART0 Transmit Buffer Register	U0TB	024Bh to 024Ah
UART1 Transmit Buffer Register	U1TB	025Bh to 025Ah
UART2 Transmit Buffer Register	U2TB	026Bh to 026Ah
UART5 Transmit Buffer Register	U5TB	028Bh to 028Ah
UART6 Transmit Buffer Register	U6TB	029Bh to 029Ah
UART7 Transmit Buffer Register	U7TB	02ABh to 02AAh
SI/O3 Bit Rate Register	S3BRG	0273h
SI/O4 Bit Rate Register	S4BRG	0277h
I2C0 Control Register 1	S3D0	02B6h
I2C0 Status Register 0	S10	02B8h

5. Protection

5.1 Introduction

In the event that a program runs out of control, this function protects the important registers listed below so that they will not be rewritten easily.

5.2 Register

Table 5.1 Register Structure

Address	Register Name	Register Symbol	After Reset
000Ah	Protect Register	PRCR	00h

5.2.1 Protect Register (PRCR)

Protect Register

b7	b6	b5	b4	b3	b2	b1	b0
0		0	0				

Symbol: PRCR
Address: 000Ah
After Reset: 00h

Bit Symbol	Bit Name	Function	RW
PRC0	Protect bit 0	Enable write to registers CM0, CM1, CM2, PLC0, PCLKR, and FRA0 0 : Write protected 1 : Write enabled	RW
PRC1	Protect bit 1	Enable write to registers PM0, PM1, PM2, TB2SC, INVC0, and INVC1 0 : Write protected 1 : Write enabled	RW
PRC2	Protect bit 2	Enable write to registers PD9, S3C, and S4C 0 : Write protected 1 : Write enabled	RW
PRC3	Protect bit 3	Enable write to registers VCR2, VWCE, VD1LS, VW0C, VW1C, and VW2C 0 : Write protected 1 : Write enabled	RW
— (b5-b4)	Reserved bits	Set to 0	RW
PRC6	Protect bit 6	Enable write to the PRG2C register 0 : Write protected 1 : Write enabled	RW
— (b7)	Reserved bit	Set to 0	RW

PRC6, PRC3, PRC1, PRC0 (Protect Bits 6, 3, 1, 0) (b6, b3, b1, b0)

When setting bits PRC6, PRC3, PRC1, and PRC0 to 1 (write enabled) by a program, the bits remain 1 (write enabled). To change registers protected by these bits, follow the procedures below:

(1) Set the PRCi (i = 0, 1, 3, 6) to 1.
(2) Write to the register protected by the PRCi bit.
(3) Set the PRCi bit to 0 (write protected).

PRC2 (Protect Bit 2) (b2)

After setting the PRC2 bit to 1 (write enabled), by writing to a given SFR, the PRC2 bit becomes 0. Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. The procedure is shown below. Make sure there are no interrupts or DMA transfers between procedure 1 and 2.

(1) Set the PRC2 bit to 1.
(2) Write to the register protected by the PRC2 bit.

5.3 Notes on Protection

After setting the PRC2 bit to 1 (write enabled), by writing to a given SFR, the PRC2 bit becomes 0. Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. Make sure there are no interrupts or DMA transfers between the instruction that sets the PRC2 bit to 1 and the next instruction.

6. Resets

6.1 Introduction

The following resets can be used to reset the MCU: hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 1 reset, voltage monitor 2 reset, oscillation stop detection reset, watchdog timer reset, and software reset.
Table 6.1 lists the Types of Resets, Figure 6.1 shows the Reset Circuit Block Diagram, and Table 6.2 lists the I/O Pins.

Table 6.1 Types of Resets

Reset Name	Trigger
Hardware reset	A low-level signal is applied to the $\overline{\text{RESET}}$ pin.
Power-on reset	The rise of the voltage on VCC1
Voltage monitor 0 reset	The drop of the voltage on VCC1 (reference voltage: Vdet0)
Voltage monitor 1 reset	The drop of the voltage on VCC1 (reference voltage: Vdet1)
Voltage monitor 2 reset	The drop of the voltage on VCC1 (reference voltage: Vdet2)
Oscillation stop detection reset	The main clock oscillator stop is detected.
Watchdog timer reset	Watchdog timer underflows.
Software reset	Setting the PM03 bit in the PM0 register to 1

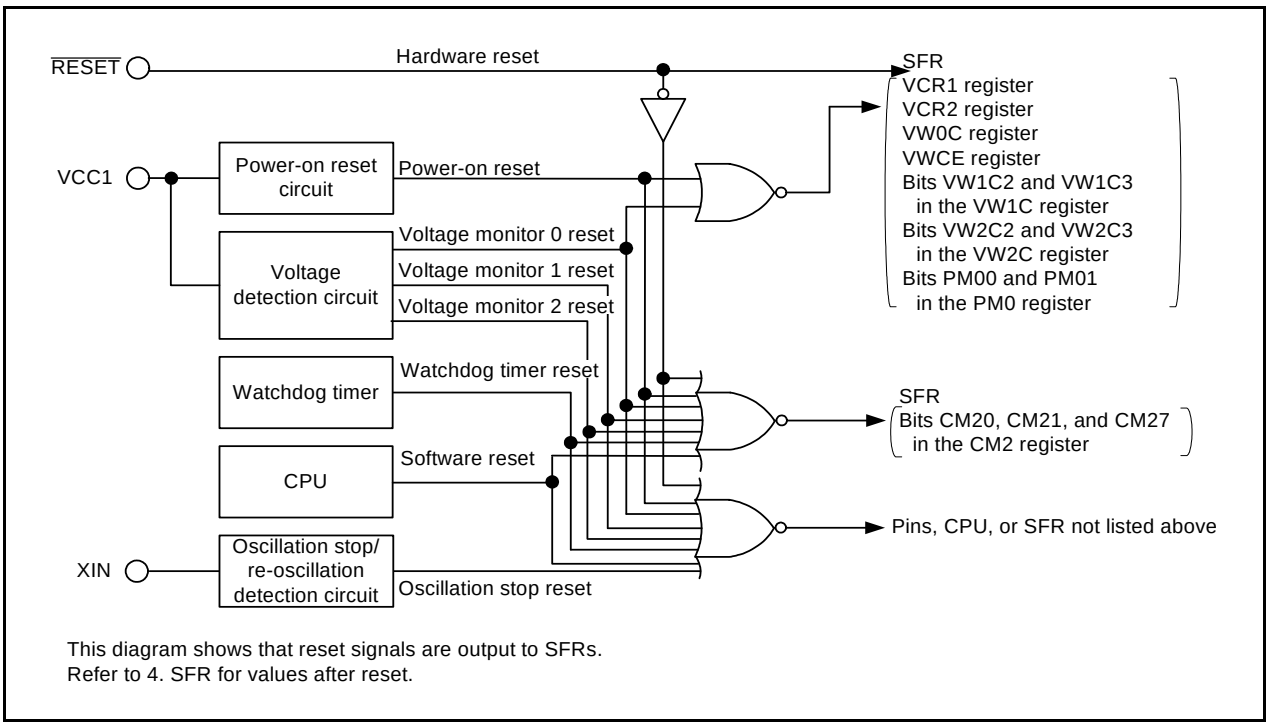


Figure 6.1 Reset Circuit Block Diagram

Table 6.2 I/O Pins

I/O Pin	I/O Type	Function
$\overline{\text{RESET}}$	Input	Hardware reset input
VCC1	Input	Power input. The power-on reset, voltage monitor 0 reset, voltage monitor 1 reset, and voltage monitor 2 reset are generated by monitoring VCC1.

Table 6.2 I/O Pins

I/O Pin	I/O Type	Function
XIN	Input	Main clock input. The oscillation stop detection reset is generated by monitoring the main clock.

6.2 Registers

Refer to 7. “Voltage Detector” for registers used for the voltage monitor 0 reset, voltage monitor 1 reset, and voltage monitor 2 reset. Refer to 15. “Watchdog Timer” for registers used for the watchdog timer reset. Refer to 8.7 “Oscillation Stop/Re-Oscillation Detect Function” for registers used for oscillation stop detection reset.

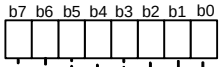
Table 6.3 Register Structure

Address	Register Name	Register Symbol	After Reset
0004h	Processor Mode Register 0	PM0	0000 0000b (CNVSS pin is low) 0000 0011b (CNVSS pin is high)
0018h	Reset Source Determine Register	RSTFR	XX00 001Xb (hardware reset) (1)

Note:
1. When not using the cold start-up/warm start-up discrimination flag in hardware reset.

6.2.1 Processor Mode Register 0 (PM0)

Processor Mode Register 0



Symbol	Address	After Reset
PM0	0004h	0000 0000b (CNVSS pin is held low) 0000 0011b (CNVSS pin is held high)

Bit Symbol	Bit Name	Function	RW
PM00	Processor mode bit	b1 b0 0 0 : Single-chip mode 0 1 : Memory expansion mode 1 0 : Do not set 1 1 : Microprocessor mode	RW
PM01			RW
PM02	R/W mode select bit	0 : $\overline{RD}$, $\overline{BHE}$, $\overline{WR}$ 1 : $\overline{RD}$, $\overline{WRH}$, $\overline{WRL}$	RW
PM03	Software reset bit	Setting this bit to 1 resets the MCU. Read as 0.	RW
PM04	Multiplexed bus space select bit	b5 b4 0 0 : Multiplexed bus is unused (separate bus in the entire $\overline{CS}$ space) 0 1 : Allocated to $\overline{CS2}$ space 1 0 : Allocated to $\overline{CS1}$ space 1 1 : Allocated to the entire $\overline{CS}$ space	RW
PM05			RW
PM06	Port P4_0 to P4_3 function select bit	0 : Address output 1 : Port function (address is not output)	RW
PM07	BCLK output disable bit	0 : BCLK is output 1 : BCLK is not output (pin is left in high-impedance)	RW

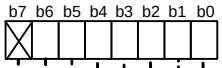
Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
The software reset, watchdog timer reset, oscillation stop detection reset, voltage monitor 1 reset, and voltage monitor 2 reset have no effect on bits PM01 to PM00.

PM03 (Software Reset Bit) (b3)

The software reset is generated by setting the PM03 bit to 1.

6.2.2 Reset Source Determine Register (RSTFR)

Reset Source Determine Register



Symbol: RSTFR | Address: 0018h | After Reset: See Table 6.4

Bit Symbol	Bit Name	Function	RW
CWR	Cold start-up/warm start-up discrimination flag	0 : Cold start 1 : Warm start	RW
HWR	Hardware reset detection flag	0 : Not detected 1 : Detected	RO
SWR	Software reset detection flag	0 : Not detected 1 : Detected	RO
WDR	Watchdog timer reset detection flag	0 : Not detected 1 : Detected	RO
LVD1R	Voltage monitor 1 reset detection flag	0 : Not detected 1 : Detected	RO
LVD2R	Voltage monitor 2 reset detection flag	0 : Not detected 1 : Detected	RO
OSDR	Oscillation stop detection reset detection flag	0 : Not detected 1 : Detected	RW
— (b7)	Reserved bit	If necessary, set to 0. Read as undefined value.	RW

Table 6.4 Bit Values in the RSTFR Register after Reset

Reset	Bits in the RSTFR Register						
	OSDR	LVD2R	LVD1R	WDR	SWR	HWR	CWR
Hardware reset	No change	0	0	0	0	1	No change
Power-on reset	0	0	0	0	0	0	0
Voltage monitor 0 reset	0	0	0	0	0	0	0
Voltage monitor 1 reset	0	0	1	0	0	0	No change
Voltage monitor 2 reset	0	1	0	0	0	0	No change
Oscillation stop detection reset	1	0	0	0	0	0	No change
Watchdog timer reset	0	0	0	1	0	0	No change
Software reset	0	0	0	0	1	0	No change

CWR (Cold Start-Up/Warm Start-Up Discrimination Flag) (b0)

Condition to become 0:

- Power-on
- Power-on reset, voltage monitor 0 reset

Condition to become 1:

- Writing 1 to the CWR bit

OSDR (Oscillation Stop Detection Reset Detection Flag) (b6)

This bit becomes 0 by writing a 0 by a program. Writing a 1 has no effect.

6.3 Optional Function Select Area

In the optional function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.
The optional function select area is not an SFR, and therefore cannot be rewritten by a program. Set a proper value when writing a program in flash memory. The entire optional function select area becomes FFh when the block including the optional function select area is erased.

6.3.1 Optional Function Select Address 1 (OFS1)

Optional Function Select Address 1

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	Factory Setting
			1			1		OFS1	FFFFFh	FFh

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Watchdog timer starts automatically after reset. 1 : Watchdog timer is in a stopped state after reset.	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect cancel bit	0 : ROM code protection cancelled. 1 : ROMCP1 bit enabled.	RW
ROMCP1	ROM code protect bit	0 : ROM code protection enabled. 1 : ROM code protection disabled.	RW
— (b4)	Reserved bit	Set to 1.	RW
VDSEL1	Vdet0 select bit 1	0 : 2.85 V (Vdet0_2) 1 : 1.90 V (Vdet0_0)	RW
LVDAS	Voltage detection 0 circuit start bit	0 : Voltage monitor 0 reset enabled after hardware reset. 1 : Voltage monitor 0 reset disabled after hardware reset.	RW
CSPROINI	After-reset count source protection mode select bit	0 : Count source protection mode enabled after reset. 1 : Count source protection mode disabled after reset.	RW

WDTON (Watchdog Timer Start Select Bit) (b0)
CSPROINI (After-Reset Count Source Protection Mode Select Bit) (b7)

These bits select the state of watchdog timer after reset.
Set the WDTON bit to 0 (watchdog timer starts automatically after reset) when setting the CSPROINI bit to 0 (count source protection mode enabled after reset).
Refer to 15. “Watchdog Timer” for details of the watchdog timer and count source protection mode.

ROMCR (ROM Code Protect Cancel Bit) (b2)
ROMCP1 (ROM Code Protect Bit) (b3)

This bit prevents reading and changing of flash memory in parallel I/O mode.

Table 6.5 ROM Code Protection

Bit Setting		ROM Code Protection
ROMCR bit	ROMCP1	
0	0	Cancelled
0	1	
1	0	Enabled
1	1	Cancelled

VDSEL1 (Vdet0 Select Bit 1) (b5)

Set the VDSEL1 bit to 0 (Vdet0 is 2.85 V) when using power-on reset or voltage monitor 0 reset. Refer to 6.4.10 “Cold Start-Up/Warm Start-Up Discrimination”.

LVDAS (Voltage Detection 0 Circuit Start Bit) (b6)

Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after hardware reset) when using power-on reset.

6.4 Operations

6.4.1 Status After Reset

The status of SFRs after reset depends on the reset type. Refer to values after reset in 4. “Special Function Registers (SFRs)”. Table 6.6 lists Pin Status When $\overline{\text{RESET}}$ Pin Level is Low, Figure 6.2 shows CPU Register Status after Reset, and Figure 6.3 shows Reset Sequence.

Table 6.6 Pin Status When $\overline{\text{RESET}}$ Pin Level is Low

Pin Name	Status (1)			
	Single-Chip Mode (CNVSS = VSS)	Microprocessor Mode (CNVSS = VCC1, P5_5 = high)		Boot Mode (CNVSS = VCC1, P5_5 = low)
		BYTE = VSS	BYTE = VCC1	
P0	Input port	Data input	Data input	Input port
P1	Input port	Data input	Input port	Input port
P2, P3, P4_0 to P4_3	Input port	Address output (undefined)	Address output (undefined)	Input port
P4_4	Input port	$\overline{\text{CS0}}$ output (High level is output)	$\overline{\text{CS0}}$ output (High level is output)	Input port
P4_5 to P4_7	Input port	Input port (pulled high)	Input port (pulled high)	Input port
P5_0	Input port	$\overline{\text{WR}}$ output (High level is output)	$\overline{\text{WR}}$ output (High level is output)	$\overline{\text{CE}}$ input (2)
P5_1	Input port	$\overline{\text{BHE}}$ output (undefined)	$\overline{\text{BHE}}$ output (undefined)	Input port
P5_2	Input port	$\overline{\text{RD}}$ output (High level is output)	$\overline{\text{RD}}$ output (High level is output)	Input port
P5_3	Input port	BCLK output	BCLK output	Input port
P5_4	Input port	$\overline{\text{HLDA}}$ output (The output value depends on the input to the $\overline{\text{HOLD}}$ pin)	$\overline{\text{HLDA}}$ output (The output value depends on the input to the $\overline{\text{HOLD}}$ pin)	Input port
P5_5	Input port	$\overline{\text{HOLD}}$ input (2)	$\overline{\text{HOLD}}$ input (2)	$\overline{\text{EPM}}$ input (3)
P5_6	Input port	ALE output (Low level is output)	ALE output (Low level is output)	Input port
P5_7	Input port	$\overline{\text{RDY}}$ input	$\overline{\text{RDY}}$ input	Input port
P6, P7, P8, P9, P10	Input port	Input port	Input port	Input port

Notes:
1. These two columns show the valid pin state when the internal power supply voltage has stabilized after power on. The pin state is undefined until the internal power supply voltage stabilizes.
2. Input a high-level signal.
3. Input a low-level signal.

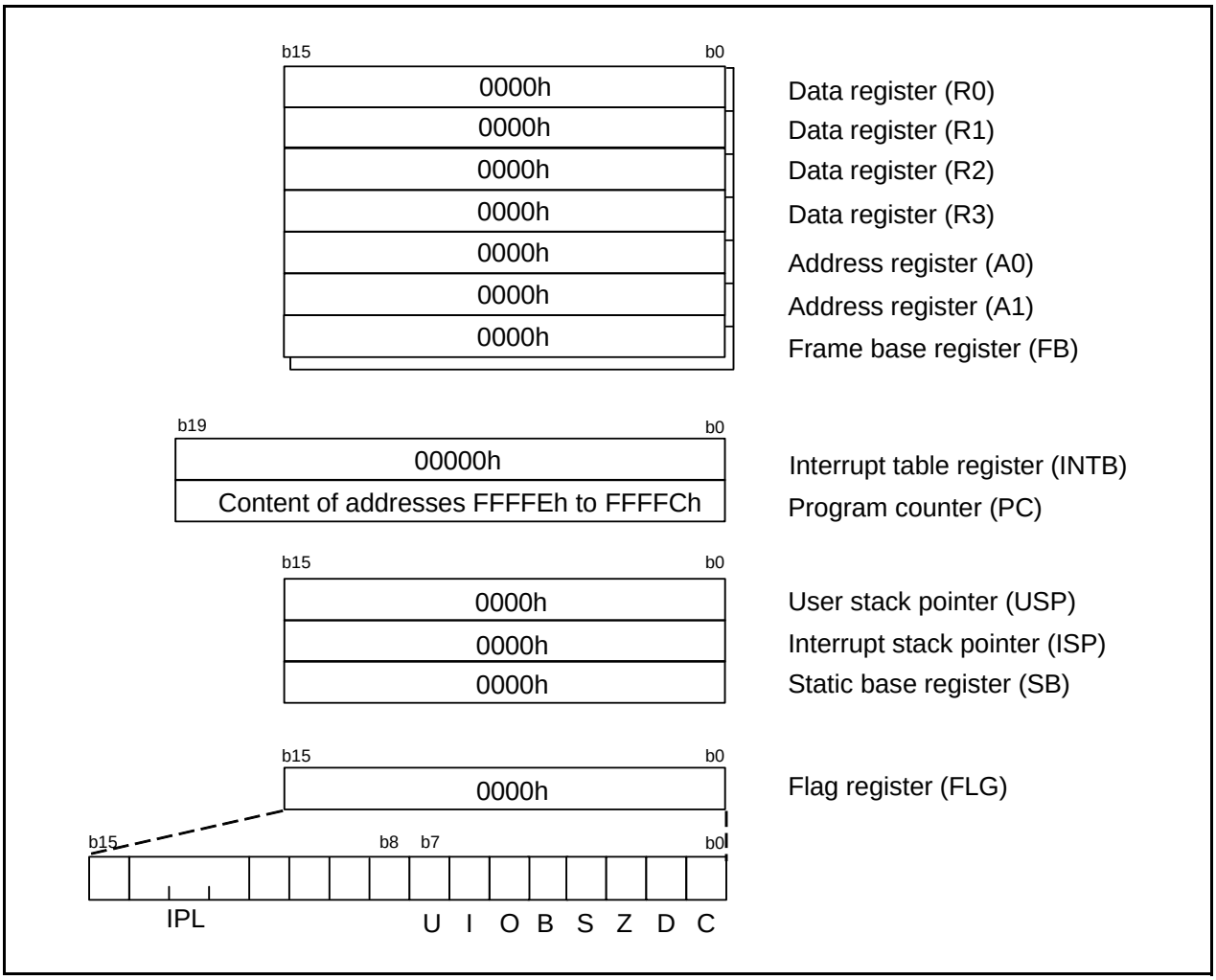


Figure 6.2 CPU Register Status after Reset

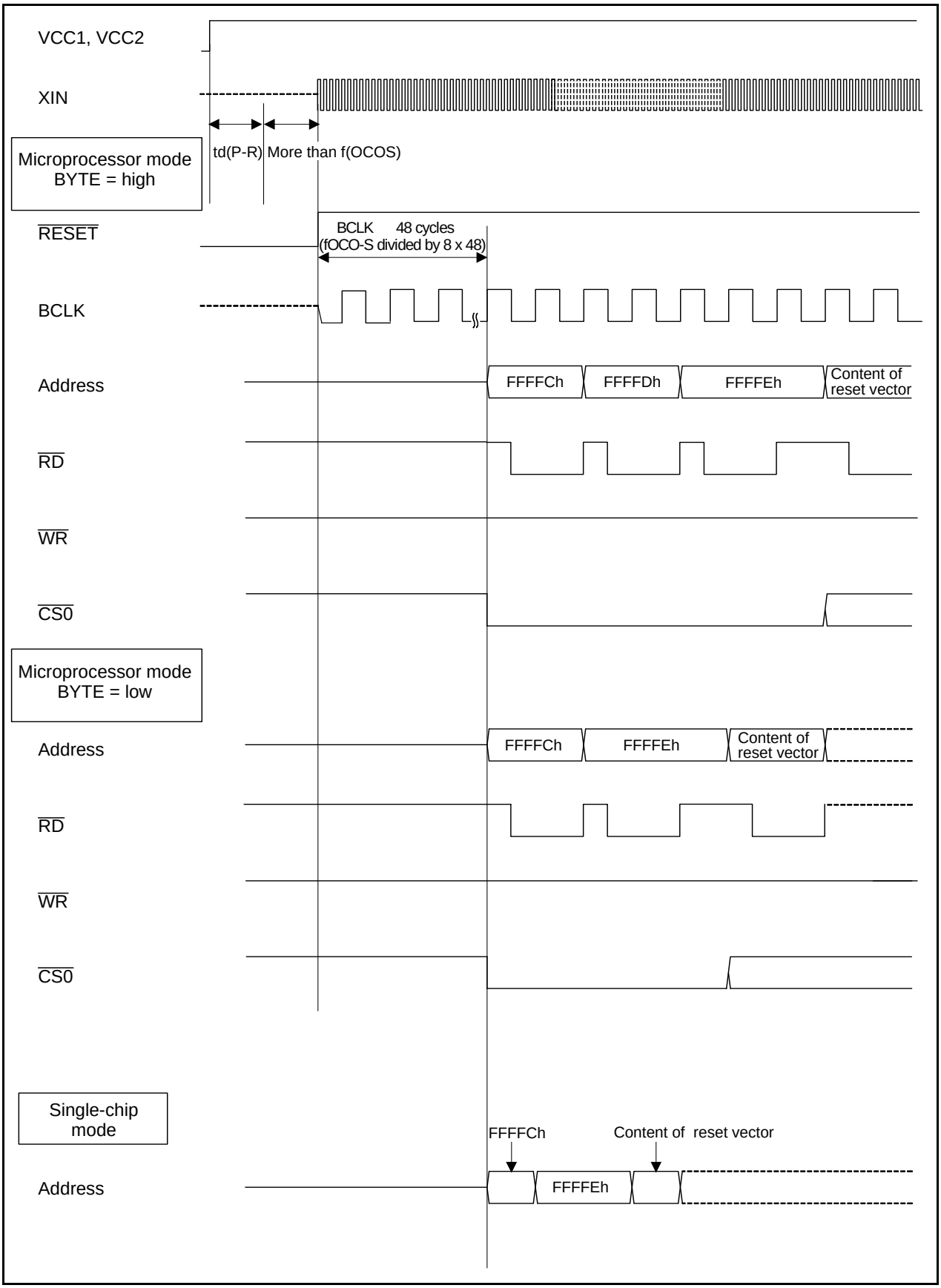


Figure 6.3 Reset Sequence

6.4.2 Hardware Reset

This reset is triggered by the $\overline{\text{RESET}}$ pin. If the power supply voltage meets the recommended operating conditions, the MCU resets the pins, CPU, and SFRs when a low-level signal is applied to the $\overline{\text{RESET}}$ pin.

When the signal applied to the $\overline{\text{RESET}}$ pin changes from low to high, the MCU executes the program at the address indicated by the reset vector. The fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The HWR bit in the RSTFR register becomes 1 (hardware reset detected) after hardware reset. Refer to 4. “Special Function Registers (SFRs)” for the rest of the SFR states after reset.

The internal RAM is not reset. When a low-level signal is applied to the $\overline{\text{RESET}}$ pin while writing data to the internal RAM, the internal RAM is in an undefined state.

The procedures for generating a hardware reset are as follows:

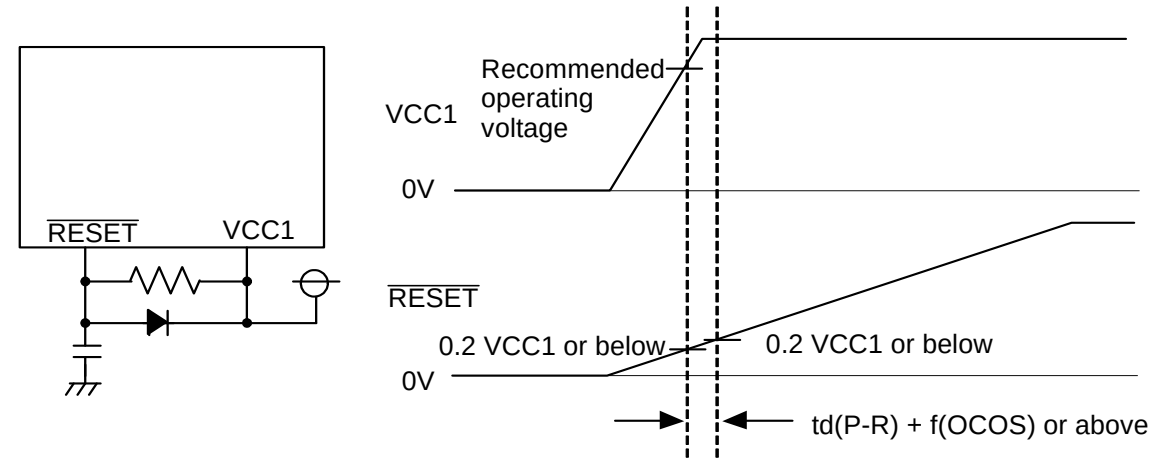
When Power Supply is Stable

(1) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(2) Wait for f(OCOS).
(3) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.

When Power is Turned on

(4) Apply a low-level signal to the $\overline{\text{RESET}}$ pin.
(5) Raise the power supply voltage to the recommended operating level.
(6) Wait for td(P-R) until the internal voltage stabilizes.
(7) Wait for f(OCOS).
(8) Apply a high-level signal to the $\overline{\text{RESET}}$ pin.

Figure 6.4 shows an Example Reset Circuit.



Note :
1. If VCC1 > VCC2, make sure that the VCC2 voltage is lower than that of VCC1 when the power is turned on or off.

Figure 6.4 Example Reset Circuit

6.4.3 Power-On Reset Function

When the $\overline{\text{RESET}}$ pin is connected to the VCC1 pin via a pull-up resistor, and the VCC1 pin voltage level rises while the rise gradient is trth or more, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFRs. Also, when a capacitor is connected to the $\overline{\text{RESET}}$ pin, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8 VCC or more.

When the input voltage to the VCC1 pin reaches the Vdet0 level or above, the fOCO-S starts counting. When the fOCO-S count reaches 32, the internal reset signal is held high and the MCU executes the program at the address indicated by the reset vector. The fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The CWR bit in the RSTFR register becomes 0 (cold start-up) after power-on reset. Refer to 4. “Special Function Registers (SFRs)” for the remaining SFR states after reset.

The internal RAM is not reset.

Use the voltage monitor 0 reset together with the power-on reset. Set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset) to use the power-on reset. In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1 and the VC25 bit in the VCR2 register is 1). Do not set these bits to 0 by a program.

Refer to 7. “Voltage Detector” for details of the voltage monitor 0 reset.

Figure 6.5 shows Example of Power-On Reset Circuit and Operation.

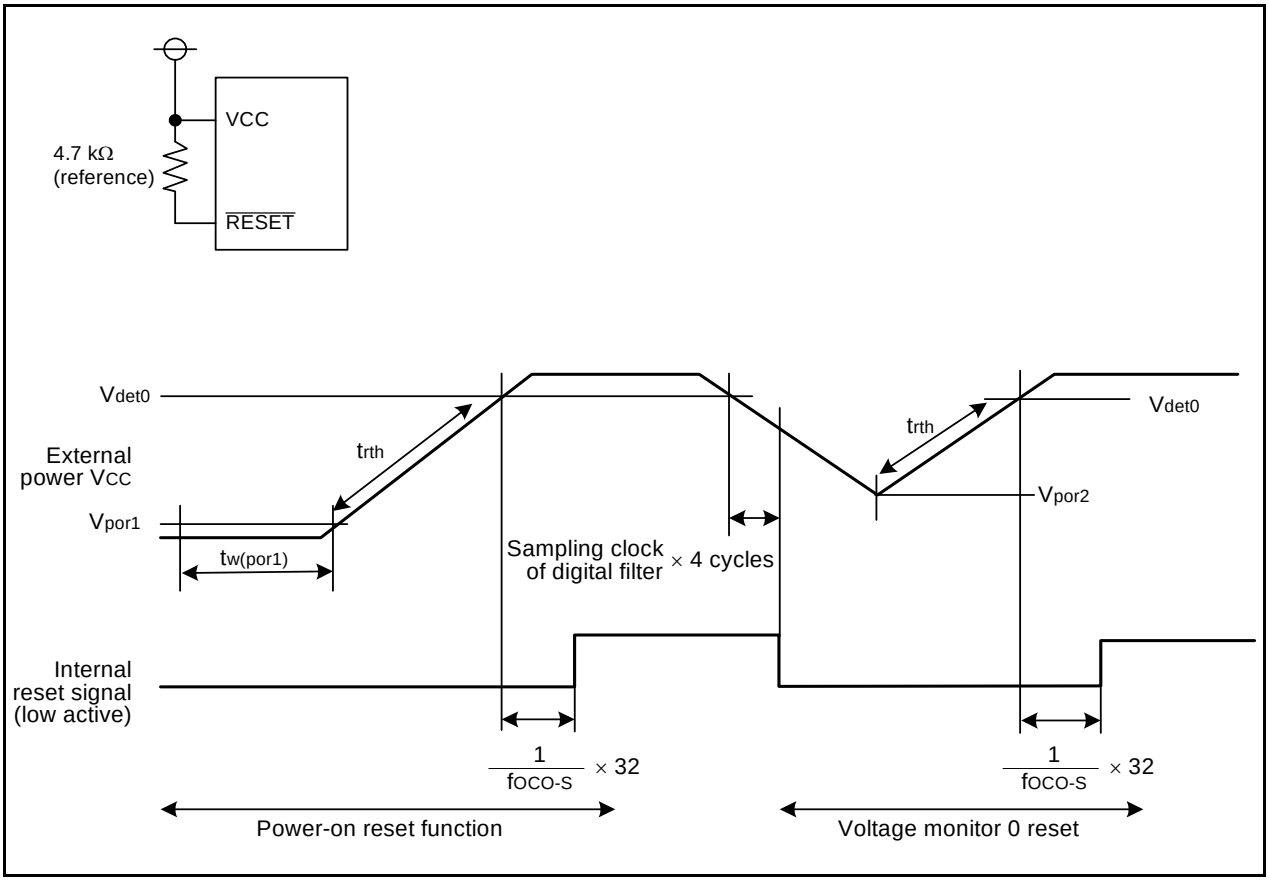


Figure 6.5 Example of Power-On Reset Circuit and Operation

6.4.4 Voltage Monitor 0 Reset

This reset is triggered by the MCU's on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the voltage applied to the VCC1 pin (Vdet0).

The MCU resets the pins, CPU, and SFRs when the voltage applied to the VCC1 pin drops to Vdet0 or below.

Then, the fOCO-S starts counting when the voltage applied to the VCC1 pin rises to Vdet0 or above. The internal reset signal becomes high after 32 cycles of the fOCO-S, and then the MCU executes the program at the address indicated by the reset vector. The fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The CWR bit in the RSTFR register becomes 0 (cold start-up) after voltage monitor 0 reset. Refer to 4. “Special Function Registers (SFRs)” for the remaining SFR states after reset.

The internal RAM is not reset. When the voltage applied to the VCC1 pin drops to Vdet0 or below while writing data to the internal RAM, the internal RAM is in an undefined state.

Refer to 7. “Voltage Detector” for details of the voltage monitor 0 reset.

6.4.5 Voltage Monitor 1 Reset

This reset is triggered by the MCU's on-chip voltage detection 1 circuit. The voltage detection 1 circuit monitors the voltage applied to the VCC1 pin (Vdet1).

When the VW1C6 bit in the VW1C register is 1 (voltage monitor 1 reset when Vdet1 passage is detected), the MCU resets the pins, CPU, and SFRs when the voltage applied to the VCC1 pin drops to Vdet1 or below. Then, after the set amount of time, the MCU executes the program at the address indicated by the reset vector. The fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The LVD1R bit in the RSTFR register becomes 1 (voltage monitor 1 reset detected) after voltage monitor 1 reset. Some SFRs are not reset at voltage monitor 1 reset. Refer to 4. “Special Function Registers (SFRs)” for details. The processor mode remains unchanged since bits PM01 to PM00 in the PM0 register are not reset.

The internal RAM is not reset.

Refer to 7. “Voltage Detector” for details of the voltage monitor 1 reset.

6.4.6 Voltage Monitor 2 Reset

This reset is triggered by the MCU's on-chip voltage detection 2 circuit. The voltage detection 2 circuit monitors the voltage applied to the VCC1 pin (Vdet2).

When the VW2C6 bit in the VW2C register is 1 (voltage monitor 2 reset when Vdet2 passage is detected), the MCU resets the pins, CPU, and SFRs when the voltage applied to the VCC1 pin drops to Vdet2 or below. Then, after the set amount of time, the MCU executes the program at the address indicated by the reset vector. The fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The LVD2R bit in the RSTFR register becomes 1 (voltage monitor 2 reset detected) after voltage monitor 2 reset. Some SFRs are not reset at voltage monitor 2 reset. Refer to 4. “Special Function Registers (SFRs)” for details. The processor mode remains unchanged since bits PM01 to PM00 in the PM0 register are not reset.

The internal RAM is not reset.

Refer to 7. “Voltage Detector” for details of the voltage monitor 2 reset.

6.4.7 Oscillation Stop Detection Reset

The MCU resets and stops the pins, CPU, and SFRs when the CM27 bit in the CM2 register is 0 (reset when oscillation stop detected), if it detects that the main clock oscillator has stopped.

The OSDR bit in the RSTFR register becomes 1 (oscillation stop detection reset detected).

Some SFRs are not reset at oscillation stop detection reset. Refer to 4. “Special Function Registers (SFRs)” for details. The processor mode remains unchanged since bits PM01 to PM00 in the PM0 register are not reset.

The internal RAM is not reset. When the main clock oscillation stop is detected while writing data to the internal RAM, the internal RAM is in an undefined state.

Oscillation stop detection reset is canceled by hardware reset or voltage monitor 0 reset.

Refer to 8.7 “Oscillation Stop/Re-Oscillation Detect Function” for details.

6.4.8 Watchdog Timer Reset

The MCU resets the pins, CPU, and SFRs when the PM12 bit in the PM1 register is 1 (reset when watchdog timer underflows) and the watchdog timer underflows. Then the MCU executes the program at the address determined by the reset vector. The fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The WDR bit in the RSTFR register becomes 1 (watchdog timer reset detected). Some SFRs are not reset at watchdog timer reset. Refer to 4. “Special Function Registers (SFRs)” for details. The processor mode remains unchanged since bits PM01 to PM00 in the PM0 register are not reset.

The internal RAM is not reset. When the watchdog timer underflows while writing data to the internal RAM, the internal RAM is in an undefined state.

Refer to 15. “Watchdog Timer” for details.

6.4.9 Software Reset

The MCU resets the pins, CPU, and SFRs when the PM03 bit in the PM0 register is 1 (MCU reset). Then the MCU executes the program at the address determined by the reset vector. The fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The SWR bit in the RSTFR register becomes 1 (software reset detected). Some SFRs are not reset at software reset. Refer to 4. “Special Function Registers (SFRs)” for details. The processor mode remains unchanged since bits PM01 to PM00 in the PM0 register are not reset.

The internal RAM is not reset.

6.4.10 Cold Start-Up/Warm Start-Up Discrimination

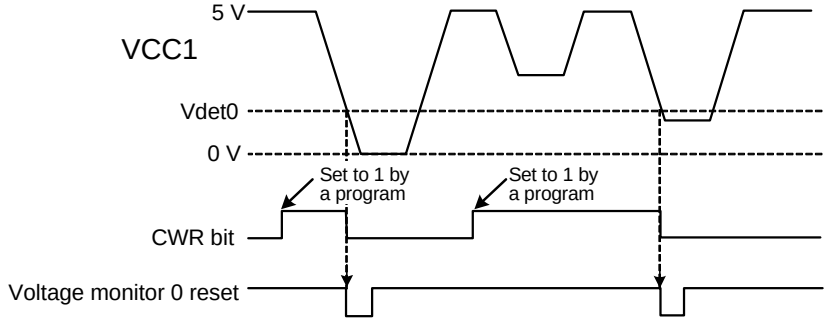
The cold start-up/warm start-up discrimination detects whether or not voltage applied to the VCC1 pin drops to the RAM hold voltage or below. The reference voltage is Vdet0. Therefore, the voltage monitor 0 reset is used for cold start-up/warm start-up discrimination. Follow Table 7.6 “Steps to Set Voltage Monitor 0 Reset Related Bits” to set the bits related to the voltage monitor 0 reset.

The CWR bit in the RSTFR register is 0 (cold start-up) when power is turned on. The CWR bit also becomes 0 after power-on reset or voltage monitor 0 reset. The CWR bit becomes 1 (warm start-up) by writing 1 by a program and remains unchanged at hardware reset, voltage monitor 1 reset, voltage monitor 2 reset, oscillation stop detection reset, watchdog timer reset, or software reset.

In the cold start-up/warm start-up discrimination, the Vdet0 level can be selected by setting the VDSEL1 bit in the OFS1 address.

- When power-on reset or voltage monitor 0 reset is used
  Set the VDSEL1 bit to 0 (Vdet0 = 2.85 V (Vdet0_2)).
- When neither power-on reset nor voltage monitor 0 reset is used as the user system
  Set the VDSEL1 bit to 1 (Vdet0 = 1.90 V (Vdet0_0)). In this case, voltage monitor 0 reset and its cancellation are based on Vdet0_0. Therefore, execute hardware reset after the cancellation of voltage monitor 0 reset.

Figure 6.6 shows the Cold Start-Up/Warm Start-Up Discrimination Example.



The above diagram shows an instance in which the digital filter is not used.

Figure 6.6 Cold Start-Up/Warm Start-Up Discrimination Example

6.5 Notes on Resets

6.5.1 Power Supply Rising Gradient

When supplying power to the MCU, make sure that the power supply voltage applied to the VCC1 pin meets the SVCC conditions.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
SVCC	Power supply rising gradient (VCC1) (Voltage range: 0 to 2)	0.05			V/ms

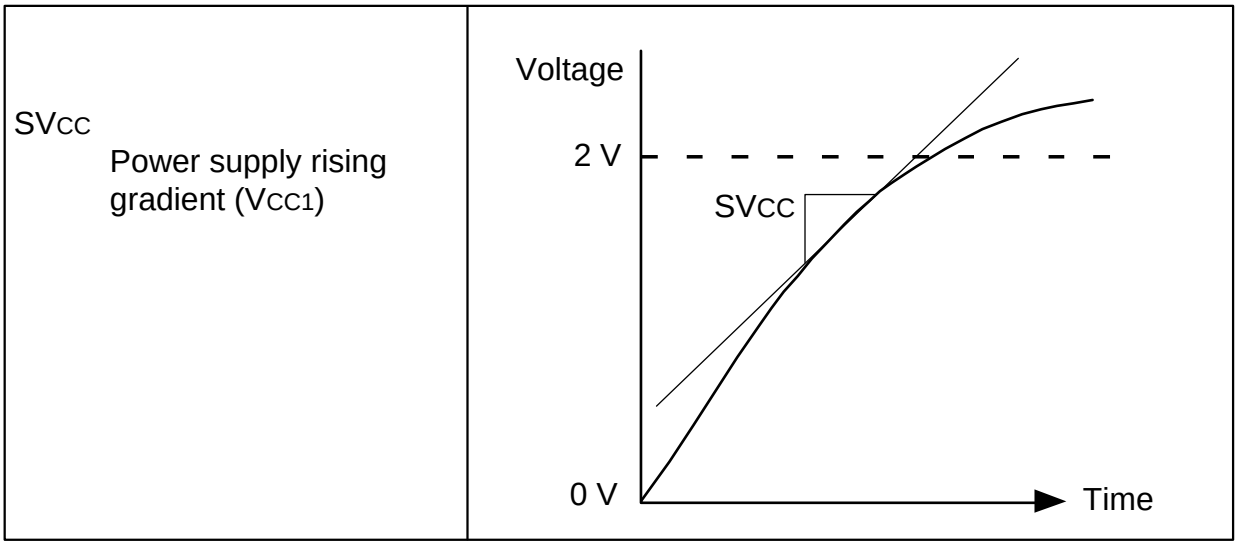


Figure 6.7 Timing of SVcc

6.5.2 Power-On Reset

Use the voltage monitor 0 reset together with the power-on reset. To use power-on reset, set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset). In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1, and the VC25 bit in the VCR2 register is 1) after power-on reset. Do not disable the bits by a program.

6.5.3 OSDR Bit (Oscillation Stop Detection Reset Detection Flag)

When the oscillation stop detection reset is generated, the MCU is reset and then stopped. This state is canceled by hardware reset or voltage monitor 0 reset.

Note that the OSDR bit remains unchanged at hardware reset, but is set to 0 (not detected) at voltage monitor 0 reset.

7. Voltage Detector

7.1 Introduction

The voltage detection circuit monitors the voltage applied to the VCC1 pin. This circuit can be programmed to monitor the VCC1 input voltage. Alternately, voltage monitor 0 reset, voltage monitor 1 interrupt, voltage monitor 1 reset, voltage monitor 2 interrupt, and voltage monitor 2 reset can also be used.

Table 7.1 lists the Voltage Detector Specifications and Figure 7.1 shows Voltage Detection Circuit.

Table 7.1 Voltage Detector Specifications

Item		Voltage Detection 0	Voltage Detection 1	Voltage Detection 2
VCC1 monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing Vdet0 by rising or falling	Whether passing Vdet1 by rising or falling	Whether passing Vdet2 by rising or falling
	Monitor	None	VW1C3 bit in VW1C register	VC13 bit in VCR1 register
			Whether VCC1 is higher or lower than Vdet1	Whether VCC1 is higher or lower than Vdet2
Process when voltage is detected	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset at Vdet0 > VCC1; restart CPU operation at VCC1 > Vdet0	Reset at Vdet1 > VCC1; restart CPU operation after a specified time	Reset at Vdet2 > VCC1; restart CPU operation after a specified time
	Interrupt	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Interrupt request at Vdet1 > VCC1 and VCC1 > Vdet1 when digital filter is enabled; interrupt request at Vdet1 > VCC1 or VCC1 > Vdet1 when digital filter is disabled	Interrupt request at Vdet2 > VCC1 and VCC1 > Vdet2 when digital filter is enabled; interrupt request at Vdet2 > VCC1 or VCC1 > Vdet2 when digital filter is disabled
Digital filter	Switch enabled/ disabled	Available	Available	Available
	Sampling time	(Divide-by-n of fOCO-S) × 3 n: 1, 2, 4, 8	(Divide-by-n of fOCO-S) × 3 n: 1, 2, 4, 8	(Divide-by-n of fOCO-S) × 3 n: 1, 2, 4, 8

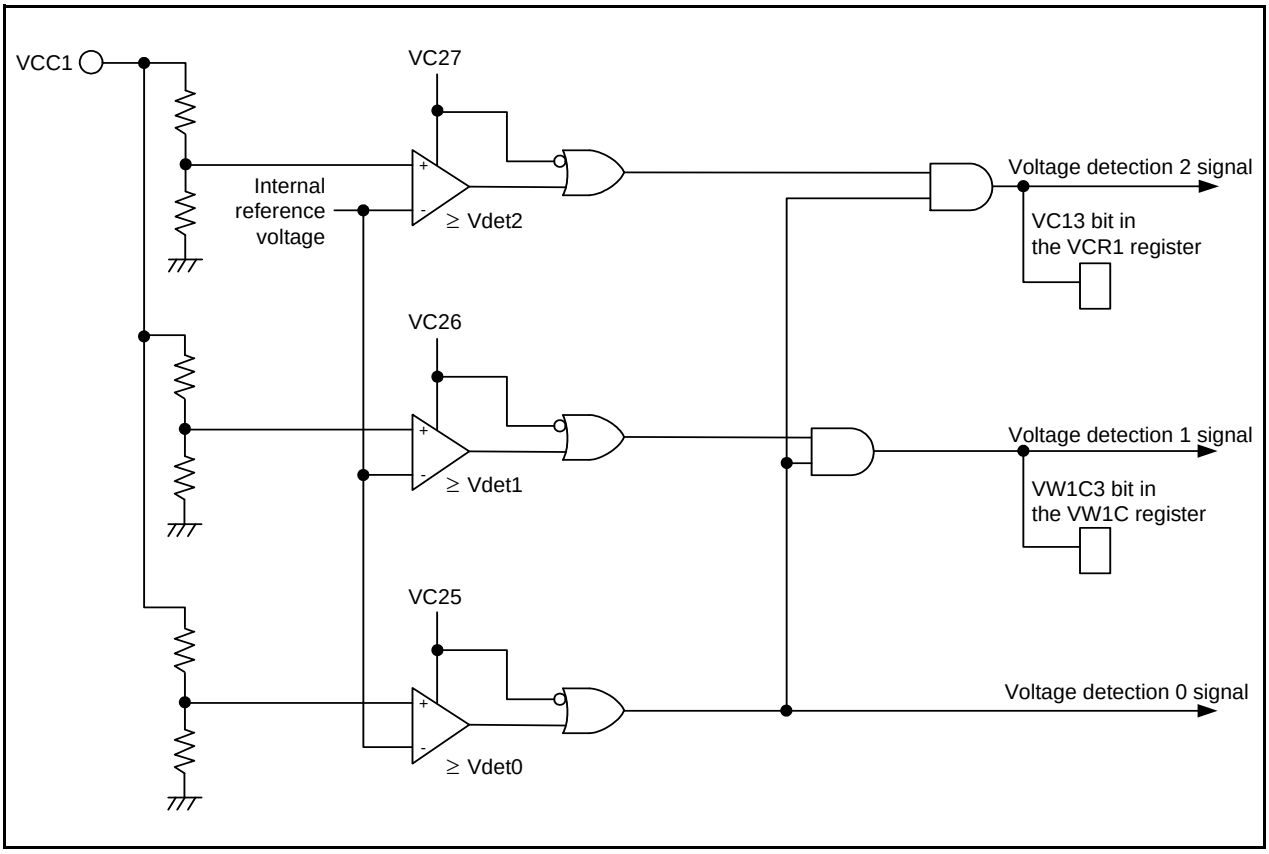


Figure 7.1 Voltage Detection Circuit

7.2 Registers

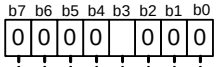
Table 7.2 Register Structure

Address	Register Name	Register Symbol	After Reset
0019h	Voltage Detection 2 Circuit Flag Register	VCR1	0000 X000b (1)
001Ah	Voltage Detection Circuit Operation Enable Register	VCR2	000X 0000b (2) 001X 0000b (3)
0026h	Voltage Monitor Function Select Register	VWCE	00h (4)
0028h	Voltage Detection 1 Level Select Register	VD1LS	0000 1010b (4)
002Ah	Voltage Monitor 0 Circuit Control Register	VW0C	1100 1X10b (2) 1100 1X11b (3)
002Bh	Voltage Monitor 1 Circuit Control Register	VW1C	1000 XX10b (1)
002Ch	Voltage Monitor 2 Circuit Control Register	VW2C	1000 0X10b (1)

Notes:
1. Hardware reset, power-on reset, or voltage monitor 0 reset
2. When the LVDAS bit of address OFS1 is 1 at hardware reset
3. This value shows the value after any of the following resets.
   - Voltage monitor 0 reset
   - When the LVDAS bit of address OFS1 is 0 at hardware reset
   - Power-on reset
4. Hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 1 reset or voltage monitor 2 reset

7.2.1 Voltage Detection 2 Circuit Flag Register (VCR1)

Voltage Detection 2 Circuit Flag Register



Symbol	Address	After Reset
VCR1	0019h	0000 X000b (hardware reset, power-on reset, voltage monitor 0 reset)

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0	RW
VC13	Low-voltage monitor flag	0 : VCC1 < Vdet2 1 : VCC1 ≥ Vdet2 or voltage detection circuit disabled	RO
— (b7-b4)	Reserved bits	Set to 0	RW

This register does not change at voltage monitor 1 reset, voltage monitor 2 reset, oscillation stop detection reset, watchdog timer reset, or software reset.

VC13 (Low-Voltage Monitor Flag) (b3)

The VC13 bit is enabled when the VW12E bit in the VWCE register is 1 (voltage detection 1 and 2 circuits enabled) and the VC27 bit in the VCR2 register is 1 (voltage detection 2 circuit enabled).

Condition to become 0:

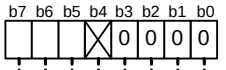
- VCC1 < Vdet 2 (when the VW12E bit is 1 and the VC27 bit is 1)

Condition to become 1:

- VCC1 ≥ Vdet 2 (when the VW12E bit is 1 and the VC27 bit is 1)
- The VC27 bit in the VCR2 register is 0 (voltage detector 2 disabled).

7.2.2 Voltage Detection Circuit Operation Enable Register (VCR2)

Voltage Detection Circuit Operation Enable Register



Symbol	Address	After Reset
VCR2	001Ah	000X 0000b (1) 001X 0000b (2)

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Reserved bits	Set to 0	RW
— (b4)	No register bit. If necessary, set to 0. Read as undefined value		—
VC25	Voltage detection 0 enable bit	0 : Disable voltage detection 0 circuit 1 : Enable voltage detection 0 circuit	RW
VC26	Voltage detection 1 enable bit	0 : Disable voltage detection 1 circuit 1 : Enable voltage detection 1 circuit	RW
VC27	Voltage detection 2 enable bit	0 : Disable voltage detection 2 circuit 1 : Enable voltage detection 2 circuit	RW

Notes :
1. When the LVDAS bit of address OFS1 is 1 at hardware reset
2. This value shows the value after any of the following resets:
   - Voltage monitor 0 reset
   - When the LVDAS bit of address OFS1 is 0 at hardware reset
   - Power-on reset

Write to the VCR2 register after setting the PRC3 bit in the PRCR register to 1 (write enabled).
This register does not change at voltage monitor 1 reset, voltage monitor 2 reset, oscillation stop detection reset, watchdog timer reset, or software reset.

VC25 (Voltage Detection 0 Enable Bit) (b5)

To use voltage monitor 0 reset, set the VC25 bit to 1 (voltage detection 0 circuit enabled). After changing the VC25 bit to 1, the detection circuit starts operating when the td(E-A) elapses.

VC26 (Voltage Detection 1 Enable Bit) (b6)

The voltage detection 1 circuit is enabled when the VW12E bit in the VWCE register is set to 1 (voltage detection 1 and 2 circuits enabled) and the VC26 bit is set to 1 (voltage detection 1 circuit enabled). Set bits VW12E and VC26 to 1 under the following conditions:

- When using voltage monitor 1 interrupt/reset
- When using bits VW1C2 and VW1C3 in the VW1C register

The detection circuit does not start operation until td(E-A) elapses after the VC26 bit is changed from 0 to 1.

VC27 (Voltage Detection 2 Enable Bit) (b7)

The voltage detection 2 circuit is enabled when the VW12E bit in the VWCE register is set to 1 (voltage detection 1 and 2 circuits enabled) and the VC27 bit is set to 1 (voltage detection 2 circuit enabled). Set bits VW12E and VC27 to 1 under the following conditions:

- When using voltage monitor 2 interrupt/reset
- When using the VC13 bit in the VCR1 register
- When using the VW2C2 bit in the VW2C register

The detection circuit does not start operation until td(E-A) elapses after the VC27 bit is changed from 0 to 1.

7.2.3 Voltage Monitor Function Select Register (VWCE)

Voltage Monitor Function Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	

Symbol	Address	After Reset
VWCE	0026h	00h (hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 1 reset, voltage monitor 2 reset)

Bit Symbol	Bit Name	Function	RW
VW12E	Voltage detection 1, 2 circuit enable bit	0 : Voltage detection 1 and 2 circuits disabled 1 : Voltage detection 1 and 2 circuits enabled	RW
— (b7-b1)	Reserved bits	Set to 0	RW

Set the PCR3 bit in the PRCR register to 1 (write enabled) before the VWCE register is rewritten.
This register does not change at watchdog timer reset, oscillation stop detection reset, or software reset.

VW12E Bit

Set the VW12E bit to 1 (enabled) when either or both of bits VC26 and VC27 in the VCR2 register are 1 (enabled).

7.2.4 Voltage Detection 1 Level Select Register (VD1LS)

Voltage Detection 1 Level Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

Symbol	Address	After Reset
VD1LS	0028h	0000 1010b (Hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 1 reset, voltage monitor 2 reset)

Bit Symbol	Bit Name	Function	RW
VD1LS0	Vdet1 Select Bit	b3 b2 b1 b0 0 1 1 0 : 3.09 V (Vdet1_6) 1 0 1 1 : 3.84 V (Vdet1_B) 1 1 1 1 : 4.44 V (Vdet1_F) Do not set values other than the above	RW
VD1LS1			RW
VD1LS2			RW
VD1LS3			RW
— (b7-b4)	Reserved bits	Set to 0.	—

Set the PCR3 bit in the PRCR register to 1 (write enabled) before the VD1LS register is rewritten.
This register does not change at watchdog timer reset, oscillation stop detection reset, or software reset.
The value of the VD1LS register is affected by the VW12E bit in the VWCE register. Table 7.3 lists Value of the VD1LS Register. When setting the VW12E bit to 0 and then 1 after setting a value to the VD1LS register, the setting value to the VD1LS register is returned.

Table 7.3 Value of the VD1LS Register

VW12E Bit	Value of the VD1LS Register
0	0000 1010b
1	Value set in the VD1LS register (0000 0111b when no value is set in the VD1LS register)

VD1LS3-VD1LS0 (Vdet1 Select Bit) (b3-b0)

To use the voltage detection 1 circuit, set the values shown in the above figure.
When the voltage detection 1 circuit is not used, the values after reset can remain as is.

7.2.5 Voltage Monitor 0 Circuit Control Register (VW0C)

Voltage Monitor 0 Circuit Control Register

b7	b6	b5	b4	b3	b2	b1	b0
1	1				0		

Symbol	Address	After Reset
VW0C	002Ah	1100 1X10b (1) 1100 1X11b (2)

Bit Symbol	Bit Name	Function	RW
VW0C0	Voltage monitor 0 reset enable bit	0 : Disabled 1 : Enabled	RW
VW0C1	Voltage monitor 0 digital filter disable mode select bit	0 : Enable digital filter 1 : Disable digital filter	RW
— (b2)	Reserved bit	Set to 0. Read as undefined value	RW
— (b3)	Reserved bit	Read as undefined value	RO
VW0F0	Sampling clock select bit	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW0F1			
— (b7-b6)	Reserved bits	Set to 1	RW

Notes :
1. When the LVDAS bit of address OFS1 is 1 at hardware reset
2. This value shows the value after any of the following resets:
   - Voltage monitor 0 reset
   - When the LVDAS bit of address OFS1 is 0 at hardware reset
   - Power-on reset

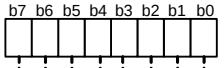
Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing to the VW0C register.
This register does not change at voltage monitor 1 reset, voltage monitor 2 reset, oscillation stop detection reset, watchdog timer reset, or software reset.

VW0C0 (Voltage Monitor 0 Reset Enable Bit) (b0)

The VW0C0 bit is enabled when the VC25 bit in the VCR2 register is 1 (voltage detection 0 circuit enabled). Set the VW0C0 bit to 0 (disabled) when the VC25 bit is 0 (voltage detection 0 circuit disabled).

7.2.6 Voltage Monitor 1 Circuit Control Register (VW1C)

Voltage Monitor 1 Circuit Control Register



Symbol: VW1C
Address: 002Bh
After Reset: 1000 XX10b (hardware reset, power-on reset, voltage monitor 0 reset)

Bit Symbol	Bit Name	Function	RW
VW1C0	Voltage monitor 1 interrupt/ reset enable bit	0 : Disabled 1 : Enabled	RW
VW1C1	Voltage monitor 1 digital filter disable mode select bit	0 : Enable digital filter 1 : Disable digital filter	RW
VW1C2	Voltage change detection flag	0 : Not detected 1 : Vdet1 passage detected	RW
VW1C3	Voltage detection 1 signal monitor flag	0 : VCC1 < Vdet1 1 : VCC1 ≥ Vdet1 or voltage detection 1 circuit disabled	RO
VW1F0 VW1F1	Sampling clock select bit	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW1C6	Voltage monitor 1 circuit mode select bit	0 : Voltage monitor 1 interrupt at Vdet1 passage 1 : Voltage monitor 1 reset at Vdet1 passage	RW
VW1C7	Voltage monitor 1 interrupt/ reset generation condition select bit	0 : When VCC1 reaches Vdet1 or above 1 : When VCC1 reaches Vdet1 or below	RW

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing to the VW1C register.
The VW1C2 bit may become 1 when the VW1C register is rewritten. Therefore, set the VW1C2 bit to 0 after rewriting the VW1C register.

VW1C0 (Voltage Monitor 1 Interrupt/Reset Enable Bit) (b0)

The VW1C0 bit is enabled when the VW12E bit in the VWCE register is 1 (voltage detection 1 and 2 circuits enabled) and the VC26 bit in the VCR2 register is 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VC26 bit is 0 (voltage detection 1 circuit disabled).

VW1C1 (Voltage Monitor 1 Digital Filter Disable Mode Select Bit) (b1)

After using the voltage monitor 1 interrupt to exit stop mode, to use it again to exit stop mode, set the VW1C1 bit to 0 first, and then to 1.

VW1C2 (Voltage Change Detection Flag) (b2)

The VW1C2 bit is enabled when the VC26 bit in the VCR2 register is 1 (voltage detection 1 circuit enabled). The VW1C2 remains unchanged even if 1 is written by a program.

Condition to become 0:

- Writing 0 by a program

Condition to become 1:

Table 7.4 Conditions Under which the VW1C2 Bit Becomes 1

Bit Setting			Conditions under Which the VW1C2 Bit Becomes 1
WV1C1	VW1C6	VW1C7	
0	0	0 or 1	The VW1C3 bit changes (from 0 to 1 and from 1 to 0).
	1	1	The VW1C3 bit changes from 1 to 0.
1	0	0	The VW1C3 bit changes from 0 to 1.
		1	The VW1C3 bit changes from 1 to 0.
	1	1	The VW1C3 bit changes from 1 to 0.

Note:

1. Do not set values not listed above.

VW1C3 (Voltage Detection 1 Signal Monitor Flag) (b3)

The VW1C3 bit is enabled when the VW12E bit in the VWCE register is 1 (voltage detection 1 and 2 circuits enabled) and the VC26 bit in the VCR2 register is 1 (voltage detection 1 circuit enabled).

Condition to become 0:

- VCC1 < Vdet1 (when the VW12E bit is 1 and the VC26 bit is 1)

Condition to become 1:

- VCC1 ≥ Vdet1 (when the VW12E bit is 1 and the VC26 bit is 1)
- The VC26 bit in the VCR2 register is 0 (voltage detection 1 circuit disabled).

VW1C6 (Voltage Monitor 1 Circuit Mode Select Bit) (b6)

The VW1C6 bit is enabled when the VW1C0 bit is 1 (voltage monitor 1 interrupt/reset enabled).

VW1C7 (Voltage Monitor 1 Interrupt/Reset Generation Condition Select Bit) (b7)

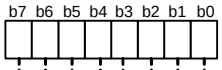
The voltage monitor 1 interrupt/reset generation condition can be selected by the VW1C7 bit when the VW1C6 bit is 0 (voltage monitor 1 interrupt at Vdet1 passage) and the VW1C1 bit is 1 (digital filter disabled).

When the VW1C6 bit is 1 (voltage monitor 1 reset at Vdet1 passage), set the VW1C7 bit to 1 (when VCC1 reaches Vdet1 or below). (Do not set the VW1C7 bit to 0.)

When the VW1C1 bit is 0 (digital filter enabled), regardless of the VW1C7 bit setting, the voltage monitor 1 interrupt is generated when VCC1 reaches Vdet1 or above and also when VCC1 reaches Vdet1 or below.

7.2.7 Voltage Monitor 2 Circuit Control Register (VW2C)

Voltage Monitor 2 Circuit Control Register



Symbol	Address	After Reset
VW2C	002Ch	1000 0X10b (hardware reset, power-on reset, voltage monitor 0 reset)

Bit Symbol	Bit Name	Function	RW
VW2C0	Voltage monitor 2 interrupt/ reset enable bit	0 : Disabled 1 : Enabled	RW
VW2C1	Voltage monitor 2 digital filter disable mode select bit	0 : Enable digital filter 1 : Disable digital filter	RW
VW2C2	Voltage change detection flag	0 : Not detected 1 : Vdet2 passage detected	RW
VW2C3	WDT detection flag	0 : Not detected 1 : Watchdog timer underflow detected	RW
VW2F0 VW2F1	Sampling clock select bit	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW2C6	Voltage monitor 2 circuit mode select bit	0 : Voltage monitor 2 interrupt at Vdet2 passage 1 : Voltage monitor 2 reset at Vdet2 passage	RW
VW2C7	Voltage monitor 2 interrupt/ reset generation condition select bit	0 : When VCC1 reaches Vdet2 or above 1 : When VCC1 reaches Vdet2 or below	RW

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
When rewriting the VW2C register, the VW2C2 bit may become 1. Set the VW2C2 bit to 0 after rewriting the VW2C register.
The VW2C3 bit does not change at voltage monitor 1 reset, voltage monitor 2 reset, oscillation stop detection reset, watchdog timer reset, or software reset.

VW2C0 (Voltage Monitor 2 Interrupt/Reset Enable Bit) (b0)

The VW2C0 bit is enabled when the VW12E bit in the VWCE register is 1 (voltage detection 1 and 2 circuits enabled) and the VC27 bit in the VCR2 register is 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disabled) when the VC27 bit is 0 (voltage detection 2 circuit disabled).

VW2C1 (Voltage Monitor 2 Digital Filter Disable Mode Select Bit) (b1)

After using the voltage monitor 2 interrupt to exit stop mode, to use it again to exit stop mode, set the VW2C1 bit to 0 first and then to 1.

VW2C2 (Voltage Change Detection Flag) (b2)

The VW2C2 bit is enabled when the VC27 bit in the VCR2 register is 1 (voltage detection 2 circuit enabled). The VW2C2 remains unchanged even if 1 is written by a program.

Condition to become 0:

- Writing 0 by a program

Condition to become 1:

Table 7.5 Conditions Under which the VW2C2 Bit Becomes 1

Bit Setting			Conditions under Which the VW2C2 Bit Becomes 1
WV2C1	VW2C6	VW2C7	
0	0	0 or 1	The VW1C3 bit changes (from 0 to 1 and from 1 to 0).
	1	1	The VW1C3 bit changes from 1 to 0.
1	0	0	The VW1C3 bit changes from 0 to 1.
		1	The VW1C3 bit changes from 1 to 0.
	1	1	The VW1C3 bit changes from 1 to 0.

Note:

1. Do not set values not listed above.

VW2C6 (Voltage Monitor 2 Circuit Mode Select Bit) (b6)

The VW2C6 bit is enabled when the VW2C0 bit is 1 (voltage monitor 2 interrupt/reset enabled).

VW2C7 (Voltage Monitor 2 Interrupt/Reset Generation Condition Select Bit) (b7)

The voltage monitor 2 interrupt/reset generation condition can be selected by the VW2C7 bit when the VW2C6 bit is 0 (voltage monitor 2 interrupt at Vdet2 passage) and the VW2C1 bit is 1 (digital filter disabled).

When the VW2C6 bit is 1 (voltage monitor 2 reset at Vdet2 passage), set the VW2C7 bit to 1 (when VCC1 reaches Vdet2 or below). (Do not set the VW2C7 bit to 0.)

When the VW2C1 bit is 0 (digital filter enabled), regardless of the VW2C7 bit setting, the voltage monitor 2 interrupt is generated when VCC1 reaches Vdet2 or above, and also when VCC2 reaches Vdet1 or below.

7.3 Optional Function Select Area

In the optional function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.
The optional function select area is not an SFR, and therefore cannot be rewritten by a program. Set a proper value when writing a program in flash memory. The entire optional function select area is set to FFh when the block including the optional function select area is erased.

7.3.1 Optional Function Select Address (OFS1)

Optional Function Select Address 1

b7	b6	b5	b4	b3	b2	b1	b0
			1			1	

Symbol	Address	Factory Setting
OFS1	FFFFFh	FFh

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Watchdog timer starts automatically after reset. 1 : Watchdog timer is in a stopped state after reset.	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect cancel bit	0 : ROM code protection cancelled. 1 : ROMCP1 bit enabled.	RW
ROMCP1	ROM code protect bit	0 : ROM code protection enabled. 1 : ROM code protection disabled.	RW
— (b4)	Reserved bit	Set to 1.	RW
VDSEL1	Vdet0 select bit 1	0 : 2.85 V (Vdet0_2) 1 : 1.90 V (Vdet0_0)	RW
LVDAS	Voltage detection 0 circuit start bit	0 : Voltage monitor 0 reset enabled after hardware reset. 1 : Voltage monitor 0 reset disabled after hardware reset.	RW
CSPROINI	After-reset count source protection mode select bit	0 : Count source protection mode enabled after reset. 1 : Count source protection mode disabled after reset.	RW

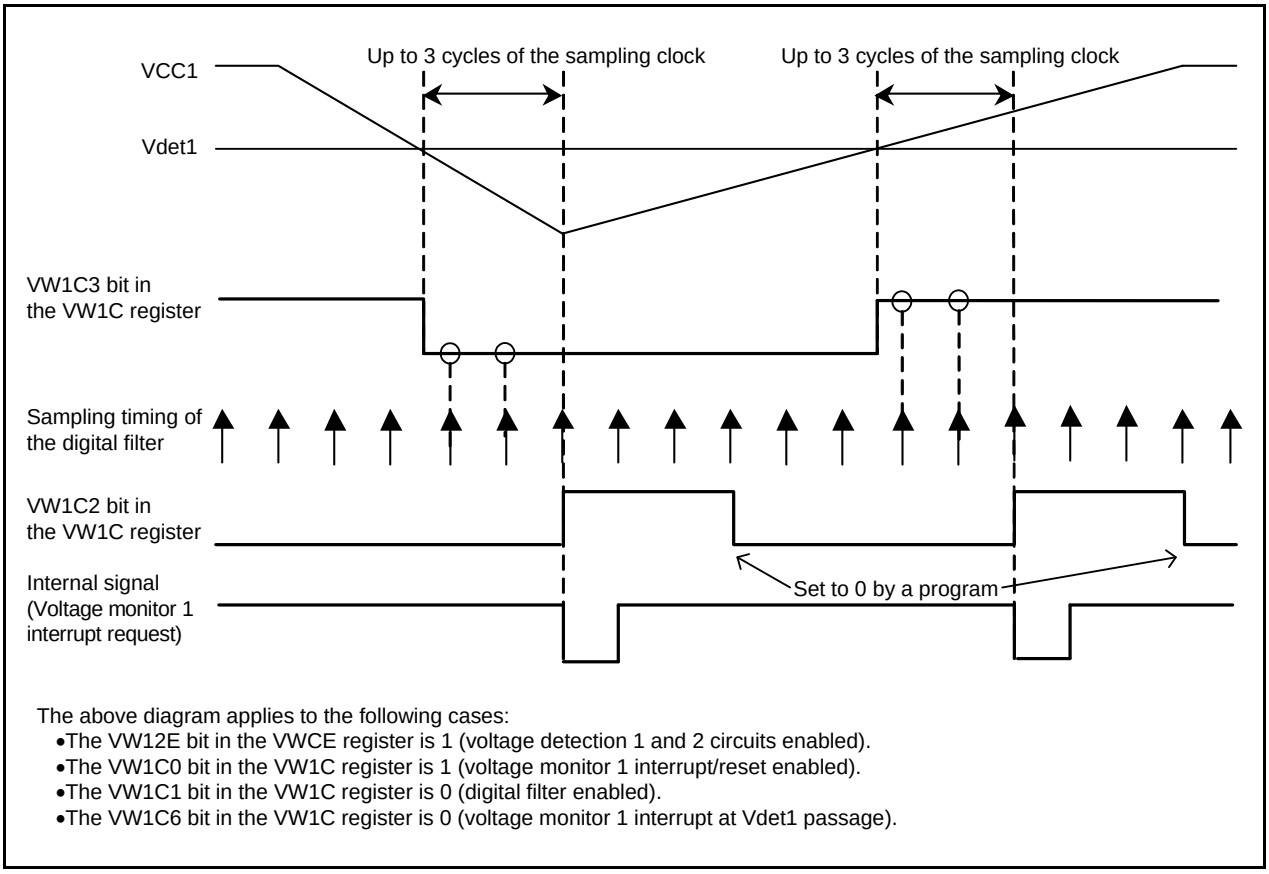
VDSEL1 (Vdet0 Select Bit 1) (b5)

The Vdet0 level used in the voltage detection 0 circuit is selectable. The voltage detection 0 circuit operates based on Vdet0.
Set the VDSEL1 bit to 0 (Vdet0 is 2.85 V) when using power-on reset or voltage monitor 0 reset. Refer to 6.4.10 “Cold Start-Up/Warm Start-Up Discrimination”.

7.4 Operations

7.4.1 Digital Filter

A digital filter can be used to monitor VCC1 input voltage. For the voltage detection i circuit (i = 0 to 2), the digital filter is enabled when the VWiC1 bit in the VWiC register is set to 0 (digital filter enabled).
The fOCO-S divided by 1, 2, 4, or 8 is selected as a sampling clock. When using the digital filter, set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on).
The VCC1 input level is sampled by the digital filter for every sampling clock. When the same sampled level is detected two times in a row, at the next sampling timing, the internal reset signal goes low or a voltage monitor i interrupt request is generated. Therefore, when the digital filter is used, the time from when the VCC1 input voltage level passes Vdeti until when a reset or an interrupt is generated is up to three cycles of the sampling clock.
Since the fOCO-S stops in stop mode, the digital filter does not function. When using the voltage detection i circuit to exit stop mode, set the VWiC1 bit in the VWiC register to 1 (digital filter disabled).
Figure 7.2 shows Digital Filter Operation Example.



The above diagram applies to the following cases:
- The VW12E bit in the VWCE register is 1 (voltage detection 1 and 2 circuits enabled).
- The VW1C0 bit in the VW1C register is 1 (voltage monitor 1 interrupt/reset enabled).
- The VW1C1 bit in the VW1C register is 0 (digital filter enabled).
- The VW1C6 bit in the VW1C register is 0 (voltage monitor 1 interrupt at Vdet1 passage).

Figure 7.2 Digital Filter Operation Example

7.4.2 Voltage Detection 0 Circuit

When the VC25 bit in the VCR2 register is 1 (voltage detection 0 circuit enabled), the voltage detection 0 circuit monitors the voltage applied to the VCC1 pin and detects whether the voltage passes Vdet0 by rising or falling. The level of Vdet0 can be selected by the VDSEL1 bit in the OFS1 address.

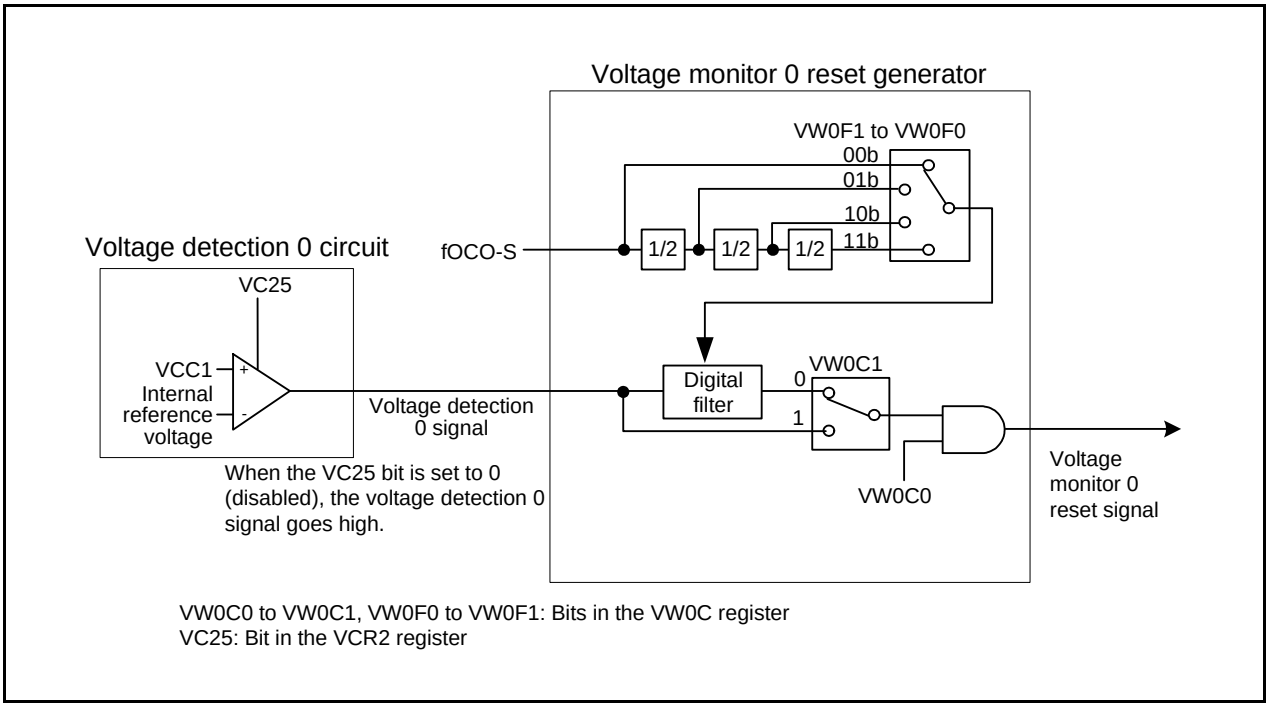


Figure 7.3 Voltage Monitor 0 Reset Generator

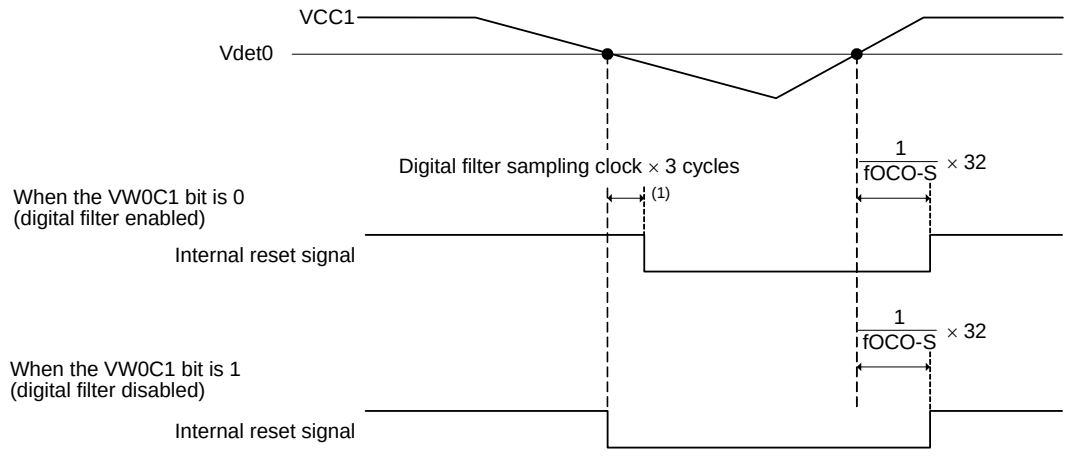
7.4.2.1 Voltage Monitor 0 Reset

When using voltage monitor 0 reset, set the VDSEL1 bit in the OFS1 address to 0 (Vdet0 is 2.85 V (Vdet0_2)).
Table 7.6 lists Steps to Set Voltage Monitor 0 Reset Related Bits.

Table 7.6 Steps to Set Voltage Monitor 0 Reset Related Bits

Step	When Using the Digital Filter	When Not Using the Digital Filter
1	Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator enabled).	-
2	Wait for digital filter sampling clock x 3 cycles.	- (no wait time)
3	Set the VC25 bit in the VCR2 register to 1 (voltage detection 0 circuit enabled).	
4	Wait for td(E (E-A).	
5	Use bits VW0F0 to VW0F1 in the VW0C register to select the digital filter sampling clock. Set the VW0C1 bit to 0 (digital filter enabled), and bits 6 and 7 to 1.	Set the VW0C1 bit in the VW0C register to 1 (digital filter disabled), and bits 6 and 7 to 1.
6	Set bit 2 in the VW0C register to 0. Set bit 2 to 0 once again after procedure 4.	
7	Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled).	

When using voltage monitor 0 reset to exit stop mode, set the VW0C1 bit in the VW0C register to 1 (digital filter disabled).
When voltage monitor 0 reset is generated, the CWR bit in the RSTFR register is automatically set to 0 (cold start-up). Refer to 6.4.4 “Voltage Monitor 0 Reset” for status after reset.
Figure 7.4 shows Voltage Monitor 0 Reset Operation Example.



VW0C1: Bit in the VW0C register

The above diagram applies under the following conditions.
- The VC25 bit in the VCR2 register is 1 (voltage detection 0 circuit enabled).
- The VW0C0 bit in the VW0C register is 1 (voltage monitor 0 reset enabled).

The pins, CPU, and SFRs are initialized when the internal reset signal goes low.
The MCU executes the program at the address indicated by the reset vector when the internal reset signal changes from low to high.
Refer to 4. “SFRs” for the SFR status after reset.

Note:
1. Make sure that VCC1 does not drop to 2.7 V or below during sampling time.

Figure 7.4 Voltage Monitor 0 Reset Operation Example

7.4.3 Voltage Detection 1 Circuit

When the VW12E bit in the VWCE register is 1 (voltage detection 1 and 2 circuits enabled) and the VC26 bit in the VCR2 register is 1 (voltage detection 1 circuit enabled), the voltage detection 1 circuit monitors the voltage applied to the VCC1 pin and detects whether the voltage passes Vdet1 by rising or falling.

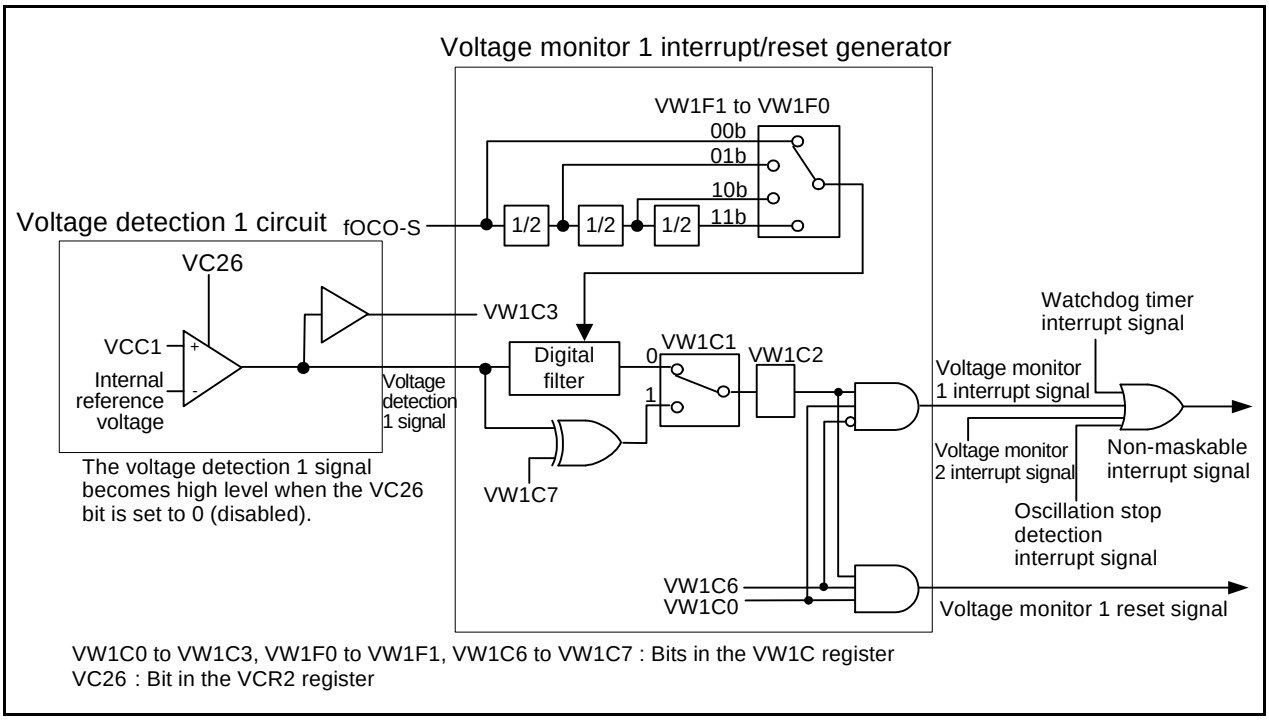


Figure 7.5 Voltage Monitor 1 Interrupt/Reset Generator

7.4.3.1 Monitoring Vdet1

Set the VW12E bit in the VWCE register to 1 (voltage detection 1 and 2 circuits enabled) and the VC26 bit in the VCR2 register to 1 (voltage detection 1 circuit enabled). Vdet1 can be monitored by using the VW1C3 bit in the VW1C register after td(E-A) elapses.

7.4.3.2 Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset

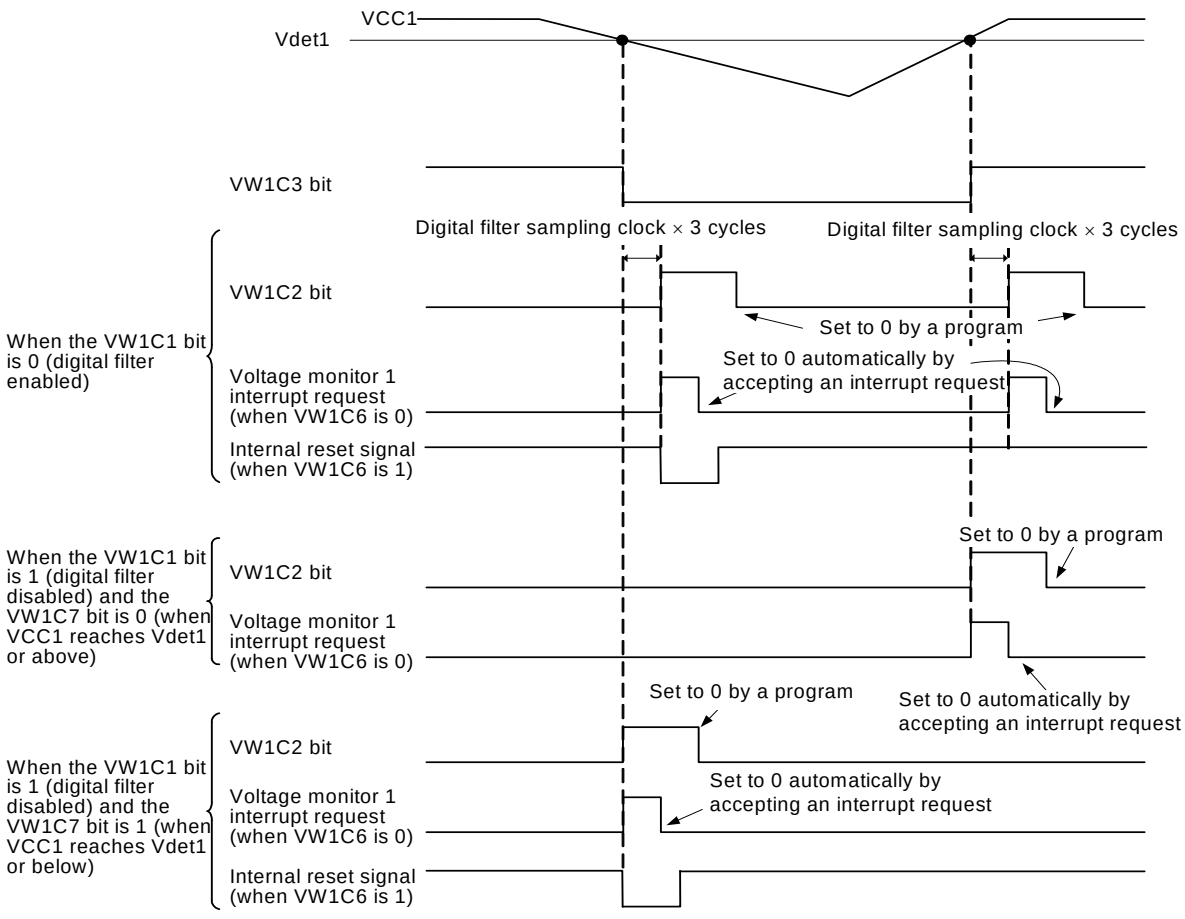
Table 7.7 lists Steps to Set Voltage Monitor 1 Interrupt/Reset Related Bits.

Table 7.7 Steps to Set Voltage Monitor 1 Interrupt/Reset Related Bits

Step	When Using the Digital Filter		When Not Using the Digital Filter	
	Voltage Monitor 1 Interrupt	Voltage Monitor 1 Reset	Voltage Monitor 1 Interrupt	Voltage Monitor 1 Reset
1	Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on)		-	
2	Wait for digital filter sampling clock x 3 cycles.		- (no wait time)	
3	Set the VW12E bit in the VWCE register to 1 (voltage detection 1 and 2 circuits enabled).			
4	Set bits VD1LS3 to VD1LS0 in the VD1LS register to select Vdet1.			
5	Set the VC26 bit in the VCR2 register to 1 (voltage detection 1 circuit enabled).			
6	Wait for td(E (E-A).			
7	Use bits VW1F0 to VW1F1 in the VW1C register to select the digital filter sampling clock.		Use the VW1C7 bit in the VW1C register to select the timing of the interrupt and reset request. (1)	
8 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).		Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).	
9 (2)	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt mode).	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset mode).	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt mode).	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset mode).
10	Set the VW1C2 bit in the VW1C register to 0 (Vdet1 passage not detected).			
11	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt/reset enabled).			

Notes:
1. Set the VW1C7 bit to 1 (when VCC reaches Vdet1 or below) for the voltage monitor 1 reset.
2. When the VW1C0 bit is 0, procedures 7, 8, and 9 can be executed simultaneously (with one instruction).

When using voltage monitor 1 interrupt or voltage monitor 1 reset to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
When voltage monitor 1 reset is generated, the LVD1R bit in the RSTFR register is automatically set to 1 (voltage monitor 1 reset detected). Refer to 6.4.5 “Voltage Monitor 1 Reset” for status after reset.
Figure 7.6 shows Voltage Monitor 1 Interrupt/Reset Operation Example.



VW1C1, VW1C2, VW1C3, VW1C6, VW1C7 : Bits in the VW1C register

The above diagram applies under the following conditions:
- The VC26 bit in the VCR2 register is 1 (voltage detection 1 circuit enabled).
- The VW1C0 bit in the VW1C register is 1 (voltage monitor 1 interrupt/reset enabled).

Note:
1. When not using the voltage monitor 0 reset, operate at 2.7 V or above (VCC1).

Figure 7.6 Voltage Monitor 1 Interrupt/Reset Operation Example

7.4.4 Voltage Detection 2 Circuit

When the VW12E bit in the VWCE register is 1 (voltage detection 1 and 2 circuits enabled) and the VC27 bit in the VCR2 register is 1 (voltage detection 2 circuit enabled), the voltage detection 2 circuit monitors the voltage applied to the VCC1 pin and detects whether the voltage passes Vdet2 by rising or falling.

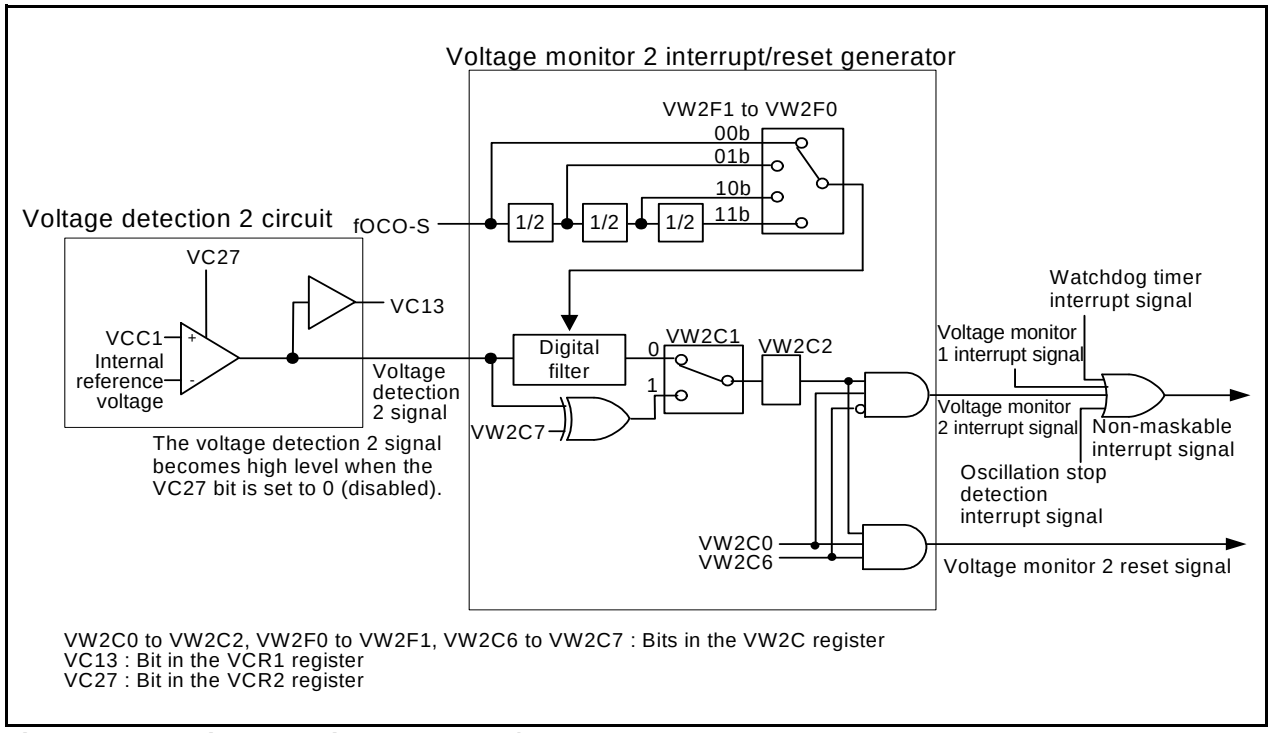


Figure 7.7 Voltage Monitor 2 Interrupt/Reset Generator

7.4.4.1 Monitoring Vdet2

Set the VW12E bit in the VWCE register to 1 (voltage detection 1 and 2 circuits enabled) and the VC27 bit in the VCR2 register to 1 (voltage detection 2 circuit enabled). Vdet2 can be monitored by using the VCA13 bit in the VCA1 register after td(E-A) elapses.

7.4.4.2 Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset

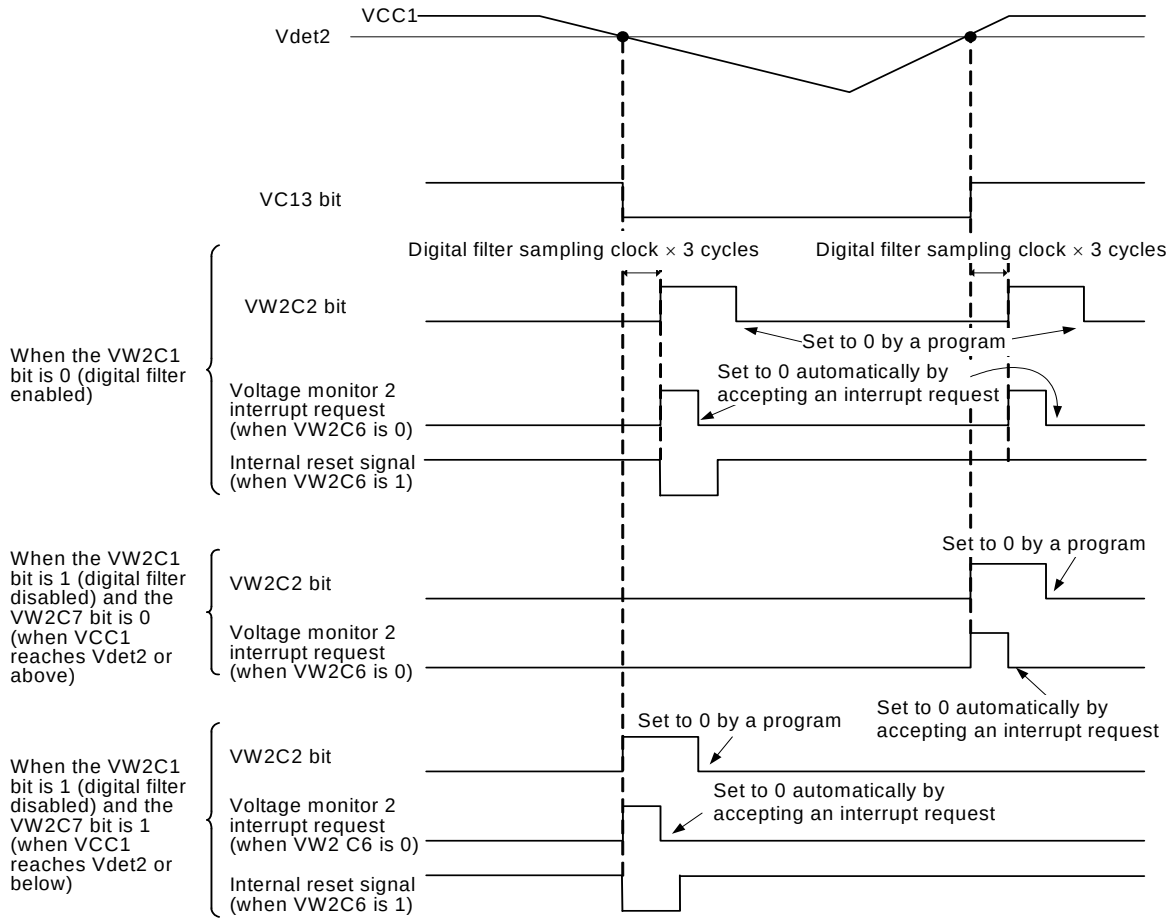
Table 7.8 lists Steps to Set Voltage Monitor 2 Interrupt/Reset Related Bits.

Table 7.8 Steps to Set Voltage Monitor 2 Interrupt/Reset Related Bits

Step	When Using the Digital Filter		When Not Using the Digital Filter	
	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset
1	Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on)		-	
2	Wait for digital filter sampling clock x 3 cycles.		- (no wait time)	
3	Set the VW12E bit in the VWCE register to 1 (voltage detection circuit enabled).			
4	Set the VC27 bit in the VCR2 register to 1 (voltage detection 2 circuit enabled).			
5	Wait for td(E (E-A).			
6	Use bits VW2F0 to VW2F1 in the VW2C register to select the digital filter sampling clock.		Use the VW2C7 bit in the VW2C register to select the timing of the interrupt and reset request. (1)	
7 (2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).		Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).	
8 (2)	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode).	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode).	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode).
9	Set the VW2C2 bit in the VW2C register to 0 (Vdet2 passage not detected).			
10	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt/reset enabled).			

Notes:
1. Set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below) for the voltage monitor 2 reset.
2. When the VW2C0 bit is 0, procedures 6, 7, and 8 can be executed simultaneously (with one instruction).

When using voltage monitor 2 interrupt or voltage monitor 2 reset to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
When voltage monitor 2 reset is generated, the LVD2R bit in the RSTFR register is automatically set to 1 (voltage monitor 2 reset detected). Refer to 6.4.6 “Voltage Monitor 2 Reset” for status after reset.
Figure 7.8 shows Voltage Monitor 2 Interrupt/Reset Operation Example.



VC13 : Bit in the VCR1 register
VW2C1, VW2C2, VW2C6, VW2C7 : Bits in the VW2C register

The above diagram applies under the following conditions:
- The VC27 bit in the VCR2 register is 1 (voltage detection 2 circuit enabled).
- The VW2C0 bit in the VW2C register is 1 (voltage monitor 2 interrupt/reset enabled).

Note:
1. When not using the voltage monitor 0 reset, operate at 2.7 V or above (VCC1).

Figure 7.8 Voltage Monitor 2 Interrupt/Reset Operation Example

7.5 Interrupts

The voltage monitor 1 interrupt and voltage monitor 2 interrupt are non-maskable interrupts.

The watchdog timer interrupt, oscillation stop and re-oscillation detection interrupt, voltage monitor 1 interrupt, and voltage monitor 2 interrupt share the same interrupt vector. When using some functions together, read the detect flags of the events in an interrupt processing program, and determine the interrupt source of the interrupt request.

The detect flag for voltage monitor 1 is the VW1C2 bit in the VW1C register, and the detect flag for voltage monitor 2 is the VW2C2 bit in the VW2C register. After the interrupt source is determined, set bits VW1C2 and VW2C2 to 0 (not detected).

8. Clock Generator

8.1 Introduction

The clock generator generates operating clocks for the CPU and peripheral circuits. Five circuits are incorporated to generate the system clock signals.

- Main clock oscillation circuit
- PLL frequency synthesizer
- 40 MHz on-chip oscillator
- 125 kHz on-chip oscillator
- Sub clock oscillation circuit

Table 8.1 lists Clock Generator Specifications, and Figure 8.1 shows System Clock Generator Circuitry.

Table 8.1 Clock Generator Specifications

Item	Main Clock Oscillation Circuit	PLL Frequency Synthesizer	On-Chip Oscillator		Sub clock Oscillation Circuit
			40 MHz On-Chip Oscillator	125 kHz On-Chip Oscillator	
Application	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when the main clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock sources when the main clock stops oscillating • Watchdog timer count source when CPU clock is stopped	• CPU clock source • Peripheral function clock source
Clock frequency	0 to 20 MHz	10 to 32 MHz	Approx. 40 MHz	Approx. 125 kHZ	32.768 kHz
Connectable oscillators	• Ceramic oscillator • Crystal oscillator	- (1)	-	-	Crystal oscillator
Pins connecting to oscillator	XIN, XOUT	- (1)	-	-	XCIN, XCOUT
Oscillation start, stop function	Yes	Yes	Yes	Yes	Yes
Oscillator status after reset	Oscillating	Stopped	Stopped	Oscillating	Stopped
Other	An externally generated clock can be input.	- (1)	-	-	An externally generated clock can be input.

Note:
1. The PLL frequency synthesizer uses the main clock oscillation circuit as a reference clock source. The items above are based on the main clock oscillation circuit.

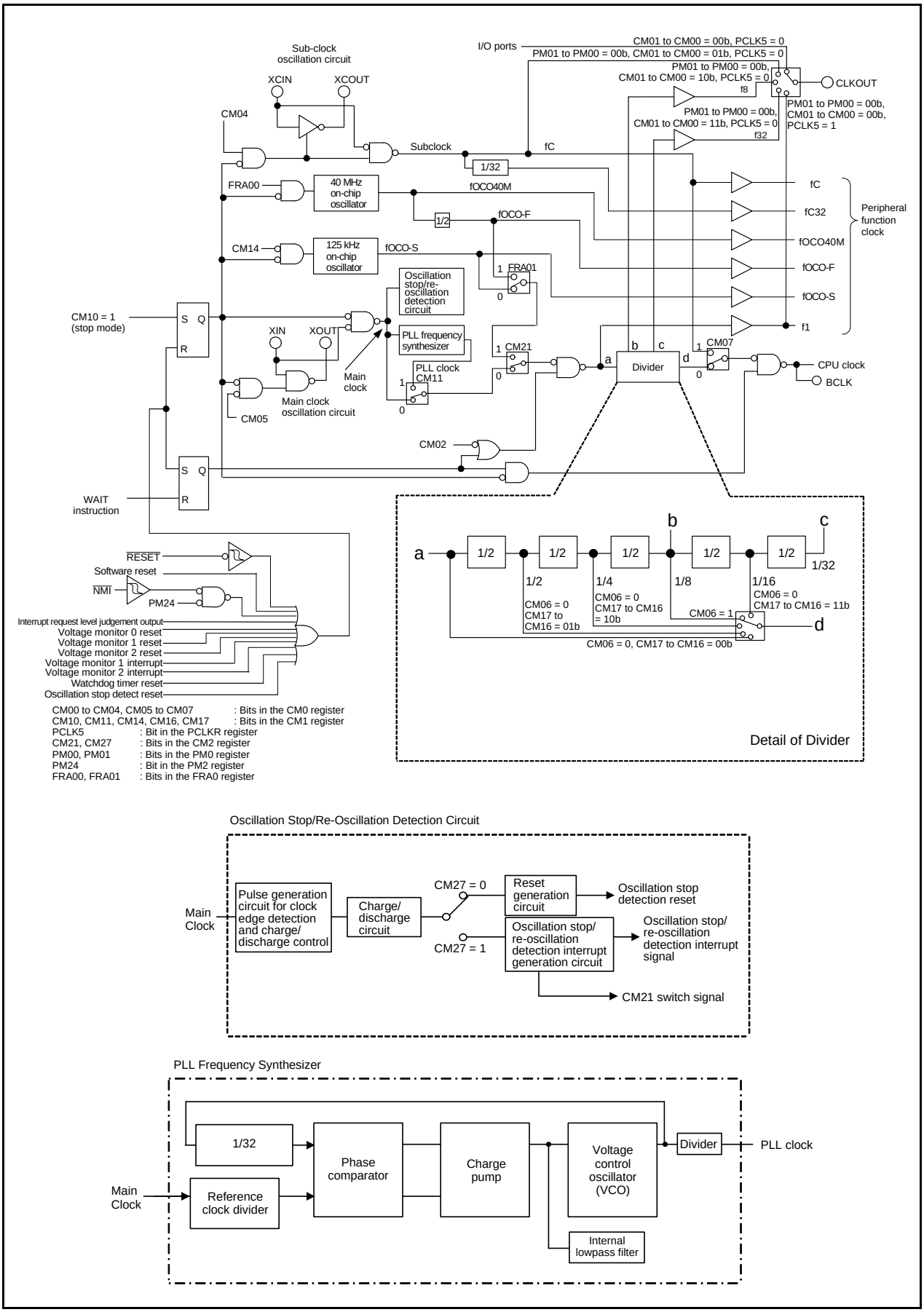


Figure 8.1 System Clock Generator Circuitry

Table 8.2 I/O Pins

Pin Name	I/O Type	Function
XIN	Input	I/O pins for the main clock oscillation circuit
XOUT	Output	
XCIN	Input (1)	I/O pins for a sub clock oscillation circuit
XCOUT	Output (1)	
CLKOUT	Output	Clock output (in single-chip mode)
BCLK	Output	BCLK output (in memory expansion mode, microprocessor mode)

Note:
1. Set the port direction bits which share pins to 0 (input mode).

8.2 Registers

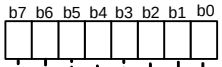
Table 8.3 Register Structure

Address	Register Name	Register Symbol	After Reset
0004h	Processor Mode Register 0	PM0	0000 0000b (CNVSS pin is low) 0000 0011b (CNVSS pin is high)
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b (1)
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
001Ch	PLL Control Register 0	PLC0	0X01 X010b
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
0022h	40 MHz On-Chip Oscillator Control Register 0	FRA0	XXXX XX00b

Note:
1. Bits CM20, CM21, and CM27 remain unchanged at oscillation stop detection reset.

8.2.1 Processor Mode Register 0 (PM0)

Processor Mode Register 0



Symbol	Address	After Reset
PM0	0004h	0000 0000b (CNVSS pin is held low) 0000 0011b (CNVSS pin is held high)

Bit Symbol	Bit Name	Function	RW
PM00	Processor mode bit	b1 b0 0 0 : Single-chip mode 0 1 : Memory expansion mode 1 0 : Do not set 1 1 : Microprocessor mode	RW
PM01			RW
PM02	R/W mode select bit	0 : $\overline{RD}$, $\overline{BHE}$, $\overline{WR}$ 1 : $\overline{RD}$, $\overline{WRH}$, $\overline{WRL}$	RW
PM03	Software reset bit	Setting this bit to 1 resets the MCU. Read as 0.	RW
PM04	Multiplexed bus space select bit	b5 b4 0 0 : Multiplexed bus is unused (separate bus in the entire $\overline{CS}$ space) 0 1 : Allocated to $\overline{CS2}$ space 1 0 : Allocated to $\overline{CS1}$ space 1 1 : Allocated to the entire $\overline{CS}$ space	RW
PM05			RW
PM06	Port P4_0 to P4_3 function select bit	0 : Address output 1 : Port function (address is not output)	RW
PM07	BCLK output disable bit	0 : BCLK is output 1 : BCLK is not output (pin is left in high-impedance)	RW

Write to the PM0 register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
Bits PM01 to PM00 do not change at software reset, watchdog timer reset, oscillation stop detection reset, voltage monitor 1 reset, or voltage monitor 2 reset.

PM07 (BCLK Output Disable Bit) (b7)

This bit is enabled in memory expansion mode and microprocessor mode. A clock with the same frequency as that of the CPU clock is output as the BCLK signal from the BCLK pin.

8.2.2 System Clock Control Register 0 (CM0)

System Clock Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
CM0	0006h	0100 1000b

Bit Symbol	Bit Name	Function	RW
CM00	Clock output function select bit (valid in single-chip mode only)	b1 b0 0 0 : I/O port P5_7 0 1 : Output fC 1 0 : Output f8 1 1 : Output f32	RW
CM01			
CM02	Wait mode peripheral function clock stop bit	0 : Peripheral function clock f1 does not stop in wait mode 1 : Peripheral function clock f1 stops in wait mode	RW
CM03	XCIN-XCOUT drive capacity select bit	0 : Low 1 : High	RW
CM04	Port XC select bit	0 : I/O ports 1 : XCIN-XCOUT oscillation function	RW
CM05	Main clock stop bit	0 : On 1 : Off	RW
CM06	Main clock division select bit 0	0 : CM16 and CM17 enabled 1 : Divide-by-8 mode	RW
CM07	System clock select bit	0 : Main clock, PLL clock or on-chip oscillator clock 1 : Sub-clock	RW

Rewrite the CM0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).
Refer to Table 9.3 “Clock Related Bit Setting and Modes” to select a clock and a mode.

CM01-CM00 (Clock Output Function Select Bit) (b1-b0)

The CLKOUT pin outputs can be selected. These bits are enabled when the PCLK5 bit in the PCLKR register is set to 0 (bits CM01 to CM00 enabled) in single-chip mode. When the PCLK5 bit is 1, set bits CM01 to CM00 to 00b. Table 8.4 shows CLKOUT Pin Functions for Single-Chip Mode.

Table 8.4 CLKOUT Pin Functions for Single-Chip Mode

PCLKR Register	CM0 Register		CLKOUT Pin Output
PCLK5 bit	CM01 bit	CM00 bit	
0	0	0	I/O port
0	0	1	Output fC
0	1	0	Output f8
0	1	1	Output f32
1	0	0	Output f1

Only set the combinations listed above.

CM02 (Wait Mode Peripheral Function Clock Stop Bit) (b2)

The CM02 bit is used to stop the peripheral function clock f1 in wait mode. The peripheral functions fC, fC32, fOCO-S, fOCO-F, and fOCO40M are not affected by the CM02 bit.
When the PM21 bit in the PM2 register is set to 1 (clock change disabled), the CM02 bit remains unchanged even when written to.

CM03 (XCIN-XCOUT Drive Capacity Select Bit) (b3)

Setting the driving capacity to low while sub-clock oscillation is stable reduces power consumption.
The CM03 bit is set to 1 (high) while the CM04 bit is 0 (P8_6 and P8_7 are I/O ports), or when entering stop mode.

CM04 (Port XC Select Bit) (b4)

The CM03 bit is set to 1 (high) while the CM04 bit is 0 (P8_6 and P8_7 are I/O ports).

CM05 (Main Clock Stop Bit) (b5)

The CM05 bit is provided to stop the main clock when selecting the low power mode or 125 kHz on-chip oscillator low power mode, or when stopping the main clock at 40 MHz on-chip oscillator mode. The CM05 bit cannot be used to detect whether the main clock is stopped or not. Refer to 8.7 “Oscillation Stop/Re-Oscillation Detect Function” for the main clock stop detection.
When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM05 bit remains unchanged even when written to.

CM06 (Main Clock Division Select Bit) (b6)

The CM06 bit becomes 1 (divide-by-8 mode) under the following conditions:

- When entering stop mode
- When the CM07 bit is 1 (sub clock used as CPU clock) and the CM05 bit is 1 (main clock off)

CM07 (System Clock Select Bit) (b7)

The CPU clock source and the peripheral function clock f1 depend on combinations of the bit status of the CM07 bit, the CM11 bit in the CM1 register, and the CM21 bit in the CM2 register. When the CM07 bit is 0 (main clock, PLL clock or on-chip oscillator clock used as CPU clock), the CPU clock source and the peripheral function clock f1 can be selected by combinations of the bit status of the CM11 bit and the CM21 bit. When the CM07 bit is 1 (sub clock used as CPU clock), the CPU clock source is fC, and the peripheral function clock f1 can be selected by combinations of the bit status of bits CM11 and CM21.
When setting the PM21 bit in the PM2 register to 1 (clock change disabled), set the CM07 bit to 0 (main clock) before setting the PM21 bit to 1. When the PM21 bit is set to 1, this bit remains unchanged even when written to.

8.2.3 System Clock Control Register 1 (CM1)

System Clock Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
					0		

Symbol	Address	After Reset
CM1	0007h	0010 0000b

Bit Symbol	Bit Name	Function	RW
CM10	All clock stop control bit	0 : Clock on 1 : All clocks off (stop mode)	RW
CM11	System clock select bit 1	0 : Main clock 1 : PLL clock	RW
— (b2)	Reserved bit	Set to 0	RW
CM13	XIN-XOUT feedback resistor select bit	0 : Internal feedback resistor connected 1 : Internal feedback resistor not connected	RW
CM14	125 kHz on-chip oscillator stop bit	0 : 125 kHz on-chip oscillator on 1 : 125 kHz on-chip oscillator off	RW
CM15	XIN-XOUT drive capacity select bit	0 : Low 1 : High	RW
CM16	Main clock division select bit 1	b7 b6 0 0 : No division mode 0 1 : Divide-by-2 mode 1 0 : Divide-by-4 mode 1 1 : Divide-by-16 mode	RW
CM17			

Rewrite the CM1 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).
Refer to Table 9.3 “Clock Related Bit Setting and Modes” to select a clock and a mode.

CM10 (All Clock Stop Control Bit) (b0)

When the CM11 bit is 1 (PLL clock), or the CM20 bit in the CM2 register is 1 (oscillation stop detection function enabled), do not set the CM10 bit to 1.
When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM10 bit remains unchanged even when written to (stop mode is not entered). When the CSPRO bit in the CSPR register is 1 (watchdog timer count source protection mode), the CM10 bit remains unchanged even when written to (stop mode is not entered).

CM11 (System Clock Select Bit) (b1)

The CM11 bit is valid when the CM21 bit in the CM2 register is set to 0 (main clock or PLL clock).
The CPU clock source and the peripheral function clock f1 can be selected by the CM11 bit when the CM07 bit is 0 (main clock, PLL clock, or on-chip oscillator clock used as CPU clock). The peripheral function clock f1 can be selected by the CM11 bit when the CM07 bit is 1 (sub clock used as CPU clock).
When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM11 bit remains unchanged even when written to.

CM13 (XIN-XOUT Feedback Resistor Select Bit) (b3)

The CM13 bit can be used when the main clock is not used at all, or when the externally generated clock is supplied to the XIN pin. When connecting a resonator between pins XIN and XOUT, set the CM13 bit to 0 (internal feedback resistor connected). Do not set this bit to 1.
When the CM10 bit is 1 (stop mode), the feedback resistor is not connected regardless of the CM13 bit status.

CM14 (125 kHz On-Chip Oscillator Stop Bit) (b4)

The CM14 bit can be set to 1 (125 kHz on-chip oscillator off) when the CM21 bit is 0 (main clock or PLL clock). When the CM21 bit is set to 1 (on-chip oscillator clock), the CM14 bit is automatically set to 0 (125 kHz on-chip oscillator on) and remains unchanged even when 1 is written to this bit. Note that the 125 kHz on-chip oscillator does not stop.
When the CSPRO bit in the CSPR register is 1 (watchdog timer count source protection mode), the CM14 bit is automatically set to 0 (125 kHz on-chip oscillator on) and remains unchanged even when 1 is written to this bit. Note that the 125 kHz on-chip oscillator does not stop.

CM15 (XIN-XOUT Drive Capacity Select Bit) (b5)

When entering stop mode or the CM05 bit is set to 1 (main clock stopped) in low speed mode, the CM15 bit is automatically set to 1 (drive capacity high).

CM17-CM16 (Main Clock Division Select Bit 1) (b7-b6)

Bits CM17 to CM16 are valid when the CM06 bit is set to 0 (bits CM16 and CM17 enabled).

8.2.4 Oscillation Stop Detection Register (CM2)

Oscillation Stop Detection Register

b7	b6	b5	b4	b3	b2	b1	b0
	X	0	0				

Symbol	Address	After Reset
CM2	000Ch	0X00 0010b

Bit Symbol	Bit Name	Function	RW
CM20	Oscillation stop and re-oscillation detection enable bit	0: Oscillation stop and re-oscillation detection function disabled 1: Oscillation stop and re-oscillation detection function enabled	RW
CM21	System clock select bit 2	0: Main clock or PLL clock 1: On-chip oscillator clock	RW
CM22	Oscillation stop and re-oscillation detection flag	0: Main clock stopped and re-oscillation not detected 1: Main clock stopped and re-oscillation detected	RW
CM23	XIN monitor flag	0: Main clock oscillating 1: Main clock stopped	RO
— (b5-b4)	Reserved bits	Set to 0	RW
— (b6)	No register bit. If necessary, set to 0. Read as undefined value		—
CM27	Operation select bit (when an oscillation stop or re-oscillation is detected)	0: Oscillation stop detection reset 1: Oscillation stop/re-oscillation detection interrupt	RW

Rewrite the CM2 register after setting the PRC0 bit in the PRCR register to 1 (write enabled). Bits CM20, CM21, and CM27 do not change at oscillation stop detection reset.
Refer to Table 9.3 “Clock Related Bit Setting and Modes” to select a clock and a mode.

CM20 (Oscillation Stop and Re-Oscillation Detection Enable Bit) (b0)

Set the CM20 bit to 0 (oscillation stop and re-oscillation detection function disabled) to enter stop mode. Set the CM20 bit back to 1 (enabled) after stop mode is exited.
When the PM21 bit in the PM2 register is 1 (clock change disabled), the CM20 bit remains unchanged even when being written.

CM21 (System Clock Select Bit 2) (b1)

When the CM07 bit is 0 (main clock, PLL clock, or on-chip oscillator clock used as CPU clock source), the CPU clock source and the peripheral function clock f1 can be selected by the CM21 bit. When the CM07 bit is 1 (sub clock used as CPU clock source), the peripheral function clock f1 can be selected by the CM21 bit.
To set the CM21 bit to 1 (on-chip oscillator clock), set the FRA01 bit in the FRA0 register to select either the 125 kHz on-chip oscillator, or the 40 MHz on-chip oscillator.
When the CM20 bit is 1 (oscillation stop and re-oscillation detection function enabled) and the CM23 bit is 1 (main clock stopped), do not set the CM21 bit to 0 (main clock or PLL clock).
When the CM20 bit is 1 (oscillation stop and re-oscillation detection function enabled), the CM27 bit is 1 (oscillation stop and re-oscillation detection interrupt), and the main clock is used as a CPU clock source, the CM21 bit is automatically set to 1 (on-chip oscillator clock) if main clock stop is detected. See 8.7 “Oscillation Stop/Re-Oscillation Detect Function” for details.

CM22 (Oscillation Stop and Re-Oscillation Detection Flag) (b2)

Condition to become 0:

- Set it to 0.

Condition to become 1:

- Main clock stop is detected.
- Main clock re-oscillation is detected.

(The CM22 bit remains unchanged even if 1 is written.)

When the CM22 bit changes state from 0 to 1, an oscillation stop/re-oscillation detection interrupt is generated. Use this bit in an interrupt routine to determine the factors of interrupts between the oscillation stop and re-oscillation detection interrupt and the watchdog timer interrupt.

When the CM22 bit is 1 and oscillation stop or re-oscillation is detected, an oscillation stop/re-oscillation detection interrupt is not generated. The bit is not set to 0 even if an oscillation stop/re-oscillation detection interrupt request is accepted.

CM23 (XIN Monitor Flag) (b3)

Determine the main clock status by reading the CM23 bit several times in the oscillation stop and re-oscillation detection interrupt routine.

8.2.5 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
0	0		0	0	0			PCLKR	0012h	0000 0011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A and B clock select bit (clock source for timers A and B, the dead time timer, and muliti-master I^2C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART2, UART5 to UART7, SI/O3, and SI/O4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0	RW
PCLK5	Clock output function extension bit (valid in single-chip mode)	0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1	RW
— (b7-b6)	Reserved bits	Set to 0	RW

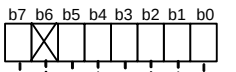
Write to the PCLKR register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

PCLK5 (Clock Output Function Extension Bit) (b5)

The PCLK5 bit is valid in single-chip mode. Output from the CLKOUT pin is selectable. When the PCLK5 bit is 1, set bits CM01 to CM00 to 00b. Refer to Table 8.4 “CLKOUT Pin Functions for Single-Chip Mode”.

8.2.6 PLL Control Register 0 (PLC0)

PLL Control Register 0



Symbol: PLC0 | Address: 001Ch | After Reset: 0X01 X010b

Bit Symbol	Bit Name	Function	RW
PLC00	PLL multiplying factor select bit	b2 b1 b0 0 0 0 : Do not set 0 0 1 : Multiply-by-2 0 1 0 : Multiply-by-4 0 1 1 : Multiply-by-6 1 0 0 : Multiply-by-8 1 0 1 : 1 1 0 : Do not set these values 1 1 1 :	RW
PLC01			RW
PLC02			RW
— (b3)	Reserved bit	Read as undefined value	RO
PLC04	Reference frequency counter set bit	b5 b4 0 0 : No division 0 1 : Divide-by-2 1 0 : Divide-by-4 1 1 : Do not set	RW
PLC05			RW
— (b6)	No register bit. If necessary, set to 0. Read as undefined value		—
PLC07	Operation enable bit	0 : PLL off 1 : PLL on	RW

Rewrite the PLC0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

PLC02-PLC00 (PLL Multiplying Factor Select Bit) (b2-b0)

Write to bits PLC00 to PLC02 when the PLC07 bit is 0 (PLL off).
When the PM21 bit in the PM2 register is 1 (clock change disabled), writing to bits PLC02 to PLC00 has no effect.

PLC05-PLC04 (Reference Frequency Counter Set Bit) (b5-b4)

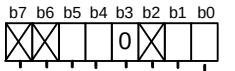
Write to bits PLC05 to PLC04 when the PLC07 bit is 0 (PLL off).
When the PM21 bit in the PM2 register is 1 (clock change disabled), writing to bits PLC05 to PLC04 has no effect.

PLC07 (Operation Enable Bit) (b7)

When the PM21 bit in the PM2 register is 1 (clock change disabled), writing to the PLC07 bit has no effect.

8.2.7 Processor Mode Register 2 (PM2)

Processor Mode Register 2



Symbol	Address	After Reset
PM2	001Eh	XX00 0X01b

Bit Symbol	Bit Name	Function	RW
PM20	Specifying wait when accessing SFR at PLL operation	0 : 2 waits 1 : 1 wait	RW
PM21	System clock protection bit	0 : Clock is protected by PRCR register 1 : Clock change disabled	RW
— (b2)	No register bit. If necessary, set to 0. Read as 0		—
— (b3)	Reserved bit	Set to 0	RW
PM24	$\overline{\text{NMI}}$ interrupt enable bit	0 : $\overline{\text{NMI}}$ interrupt disabled 1 : $\overline{\text{NMI}}$ interrupt enabled	RW
PM25	Peripheral clock fC provide bit	0 : Provided 1 : Not provide	RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as undefined value		—

Rewrite the PM2 register after setting the PRC1 bit in the PRCR register to 1 (write enabled).

PM20 (Specifying Wait When Accessing SFR at PLL Operation) (b0)

Change the PM20 bit when the PLC07 bit is 0 (PLL off). The PM20 bit becomes enabled when the PLC07 bit in the PLC0 register is set to 1 (PLL on).

PM21 (System Clock Protection Bit) (b1)

The PM21 bit is used to protect the CPU clock. (See 8.6 “System Clock Protection Function”.)
If the PM21 bit is set to 1, writing to the following bits has no effect.

- Bits CM02, CM05, and CM07 in the CM0 register
- Bits CM10 and CM11 in the CM1 register
- The CM20 bit in the CM20 register
- All bits in the PLC0 register

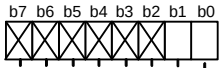
Do not execute the WAIT instruction when the PM21 bit is 1.

PM25 (Peripheral Clock fC Provide Bit) (b5)

The PM25 bit provides fC to the real-time clock, CEC function, and remote control signal receiver. (See Figure 8.5 “Peripheral Function Clocks”.)

8.2.8 40 MHz On-Chip Oscillator Control Register 0 (FRA0)

40 MHz On-Chip Oscillator Control Register 0



Symbol	Address	After Reset
FRA0	0022h	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
FRA00	40 MHz on-chip oscillator start bit	0 : 40 MHz on-chip oscillator off 1 : 40 MHz on-chip oscillator on	RW
FRA01	On-chip oscillator select bit	0 : 125 kHz on-chip oscillator 1 : 40 MHz on-chip oscillator	RW
— (b7-b2)	No register bits. If necessary, set to 0. Read as undefined value		—

Rewrite the FRA0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).
Refer to Table 9.3 “Clock Related Bit Setting and Modes”Table 9.3 “Clock Related Bit Setting and Modes” to select a clock and a mode.

FRA00 (40 MHz On-Chip Oscillator Start Bit) (b0)

When using an oscillation stop/re-oscillation detection interrupt, do not set the FRA00 bit to 0 (40 MHz on-chip oscillator off), and the FRA01 bit to 1 (40 MHz on-chip oscillator).

FRA01 (40 MHz On-Chip Oscillator Select Bit) (b1)

Change the FRA01 bit if the both conditions below are met.

- When the FRA00 bit is 1 (40 MHz on-chip oscillator on) and oscillation is stable
- When the CM14 bit in the CM1 register is 0 (125 kHz on-chip oscillator on) and oscillation is stable

When setting the FRA01 bit to 0 (125 kHz on-chip oscillator), do not set the FRA00 bit to 0 (40 MHz on-chip oscillator off) at the same time. Set the FRA00 bit to 0 after setting the FRA01 bit to 0.

8.3 Clocks Generated by Clock Generators

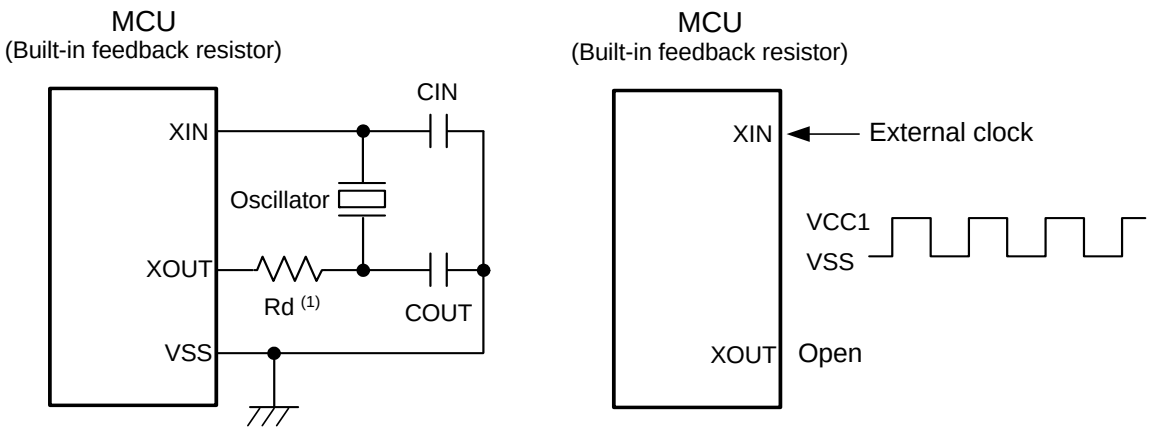
The clocks generated by the clock generators are described below.

8.3.1 Main Clock

This clock is supplied by the main clock oscillator circuit and used as a clock source for the CPU and peripheral function clocks. After reset, the main clock is running, but is not used as a clock source for the CPU.

The main clock oscillator circuit is configured by connecting a resonator between pins XIN and XOUT. The main clock oscillator circuit contains a feedback resistor, which is separated from the oscillator circuit in stop mode in order to reduce the amount of power consumed by the chip. The main clock oscillator circuit may also be configured by feeding an externally generated clock to the XIN pin.

Figure 8.2 shows Main Clock Connection Examples.



Note :
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the oscillator manufacturer. When the oscillation drive capacity is set to low, check if oscillation is stable in low status. Also, place a feedback resistor between XIN and XOUT if the oscillator manufacturer recommends placing the resistor externally.

Figure 8.2 Main Clock Connection Examples

The XOUT becomes high by setting the CM05 bit in the CM0 register to 1 (main clock oscillator circuit turned off) after switching the clock source for the CPU clock to the sub clock (fC) or on-chip oscillator clock (fOCO-F, fOCO-S). In this case, the XIN is pulled high to the XOUT via the feedback resistor because the internal feedback resistor remains connected.
When the main clock oscillator circuit is not used, setting the CM13 bit in the CM1 register to 1 enables to select the internal feedback resistor not connected.
Perform the following steps to start or stop the main clock. Refer to 8.2 “Registers” for access to register and bit.

Main clock oscillation start

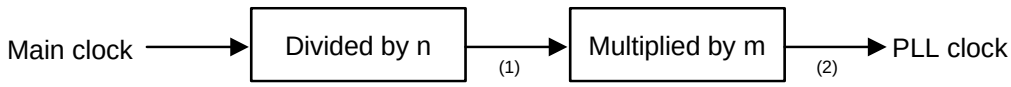
(1) Set the CM15 bit to 1 (drive capacity high) when a resonator is connected between pins XIN and XOUT.
(2) Set the CM05 bit to 0 (main clock oscillating).
(3) Wait until main clock oscillation stabilizes. (Enter the external clock when entering it from the XIN pin.)

Main clock oscillation stop

(1) Set the CM20 bit in the CM2 register to 0 (oscillation stop/re-oscillation detection function disabled).
(2) Set the CM05 bit to 1 (stop).
(3) Stop the external clock (when entering the external clock from the XIN pin).

8.3.2 PLL Clock

The PLL clock is generated by the PLL frequency synthesizer. This clock is used as the clock source for the CPU and peripheral function clocks.
After reset, the PLL frequency synthesizer is stopped.
The PLL clock is the main clock divided by the selected values of bits PLC05 to PLC04 in the PLC0 register, and then multiplied by the selected values of bits PLC02 to PLC00. Set bits PLC05 to PLC04 to fit divided frequency between 2 MHz and 5 MHz. Figure 8.3 shows Relation between Main Clock and PLL Clock.



n : 1, 2, 4 (selected by bits PLC05 to PLC04 in the PLC0 register)
m : 2, 4, 6, 8 (selected by bits PLC02 to PLC00 in the PLC0 register)

Notes :
1. Set the frequency divided by n to between 2 MHz and 5 MHz.
2. Set 10 MHz ≤ PLL clock frequency ≤ 32 MHz

Figure 8.3 Relation between Main Clock and PLL Clock

Bits PLC05 to PLC04 and bits PLC02 to PLC00 can be set only once after reset. Table 8.5 lists Example Settings for PLL Clock Frequencies.

Table 8.5 Example Settings for PLL Clock Frequencies

Main Clock	Setting Value		PLL Clock
	Bits PLC05 to PLC04	Bits PLC02 to PLC00	
10 MHz	01b (divide-by-2)	010b (multiply-by-4)	20 MHz
5 MHz	00b (not divided)	010b (multiply-by-4)	
12 MHz	10b (divide-by-4)	100b (multiply-by-8)	24 MHz
6 MHz	01b (divide-by-2)	100b (multiply-by-8)	
16 MHz	10b (divide-by-4)	100b (multiply-by-8)	32 MHz
8 MHz	01b (divide-by-2)	100b (multiply-by-8)	

8.3.3 fOCO40M

The fOCO40M is a 40 MHz clock (approx.), which is supplied by the 40 MHz on-chip oscillator. It is used as the clock source for ϕAD of AD converter.

Follow the steps below to start or stop the 40 MHz on-chip oscillator clock. Refer to 8.2 “Registers” for access to register and bit.

40 MHz on-chip oscillator clock oscillation start

(1) Set the FRA00 bit in the FRA0 register to 1 (40 MHz on-chip oscillator on).
(2) Wait for td (OCOF).

40 MHz on-chip oscillator clock oscillation stop

(1) Set the FRA01 bit in the FRA0 register to 0 (125 MHz on-chip oscillator) (when the CM27 bit is 1 (oscillation stop/re-oscillation detection interrupt)).
(2) Set the FRA00 bit in the FRA0 register to 0 (40 MHz on-chip oscillator off).

8.3.4 fOCO-F

The fOCO-F is a 40 MHz clock (approx.), which is supplied by the 40 MHz on-chip oscillator, divided by 2. It is used as the clock source for the CPU and peripheral function clocks.

After reset, the 40 MHz on-chip oscillator is stopped.

If the main clock stops oscillating and the FRA01 bit is 1 when the CM20 bit in the CM2 register is 1 (oscillation stop/re-oscillation detection function enabled), and the CM27 bit is 1 (oscillation stop/re-oscillation detection interrupt), the fOCO-F is used as the clock source for the CPU.

Follow the steps below to start or stop the 40 MHz on-chip oscillator clock. Refer to 8.2 “Registers” for access to registers and bits.

40 MHz on-chip oscillator clock oscillation start

(1) Set the FRA00 bit in the FRA0 register to 1 (40 MHz on-chip oscillator on).
(2) Wait for td (OCOF).

40 MHz on-chip oscillator clock oscillation stop

(1) Set the FRA01 bit in the FRA0 register to 0 (125 MHz on-chip oscillator) (when the CM27 bit is 1 (oscillation stop/re-oscillation detection interrupt)).
(2) Set the FRA00 bit in the FRA0 register to 0 (40 MHz on-chip oscillator off).

8.3.5 125 kHz On-Chip Oscillator Clock (fOCO-S)

This clock is approximately 125 kHz, and is supplied by the 125 kHz on-chip oscillator. It is used as the clock source for the CPU and peripheral function clocks. In addition, when the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), this clock is used as the count source for the watchdog timer (refer to 15.4.2 “Count Source Protection Mode Enabled”).

After reset, the fOCO-S divided by 8 is used as the CPU clock.

If the main clock stops oscillating and the FRA01 bit is 0, when the CM20 bit in the CM2 register is 1 (oscillation stop/re-oscillation detection function enabled) and the CM27 bit is 1 (oscillation stop/re-oscillation detection interrupt), the 125 kHz on-chip oscillator automatically starts operating and supplying the necessary clock for the MCU.

Follow the steps below to start or stop the fOCO-S. Refer to 8.2 “Registers” for access to register and bit.

fOCO-S start

(1) Set the CM14 bit in the CM1 register to 0 (125 kHz on-chip oscillator on).

(2) Wait for td (OCOS).

fOCO-S stop

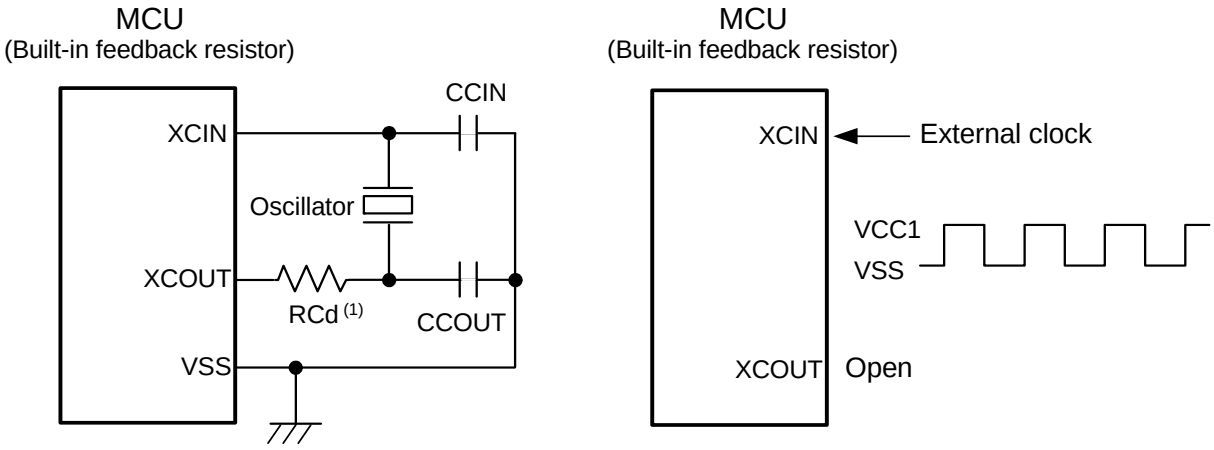
(1) Set the CM14 bit in the CM1 register to 1 (125 kHz on-chip oscillator off).

When the CM21 bit is 1 (on-chip oscillator used as the clock source for the CPU), the CM14 bit becomes 0 (125 kHz on-chip oscillator on).

8.3.6 Sub Clock (fC)

The sub clock is supplied by the sub clock oscillator circuit. This clock is used as the clock source for count sources of the CPU clock, timer A, timer B, real-time clock, CEC function, and remote control signal receiver.

The sub clock oscillator circuit is configured by connecting a crystal resonator between pins XCIN and XCOUT. The sub clock oscillator circuit contains a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The sub clock oscillator circuit may also be configured by feeding an externally generated clock to the XCIN pin. Figure 8.4 shows Sub Clock Connection Examples.



Note :
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the oscillator manufacturer. When the oscillation drive capacity is set to low, check if oscillation is stable in low status. Also, place a feedback resistor between XCIN and XCOUT if the oscillator manufacturer recommends placing the resistor externally.

Figure 8.4 Sub Clock Connection Examples

After reset, the sub clock is stopped. At this time, the feedback resistor is disconnected from the oscillator circuit.

Follow the steps below to start the sub clock. Refer to 8.2 “Registers” for access to registers and bits.

(1)Set the PU21 bit in the PUR2 register to 0 (P8_4 to P8_7 not pulled high).
(2)Set bits PD8_6 and PD8_7 in the PD8 register to 0 (P8_6, P8_7 function as input ports).
(3)Set the CM04 bit to 1 (XCIN-XCOUT oscillation function). Set the CM03 bit to 1 (XCIN-XCOUT drive capacity high).
(4)Wait until sub clock oscillation stabilizes (enter the external clock when entering it from the XCIN pin).

8.4 CPU Clock and Peripheral Function Clocks

The CPU is run by the CPU clock, and the peripheral functions are run by the peripheral function clocks.

8.4.1 CPU Clock and BCLK

The CPU clock is an operating clock for the CPU and watchdog timer. Also it is used as a sampling clock of the $\overline{NMI}/\overline{SD}$ digital filter.

The main clock, PLL clock, fOCO-F, fOCO-S, or fC can be selected as the clock source for the CPU clock. (See Table 9.2 “Clocks in Normal Operating Mode”.)

When the main clock, PLL clock, fOCO-F, or fOCO-S is selected as the clock source for the CPU clock, the selected clock source can be divided by 1 (no division), 2, 4, 8 or 16 to produce the CPU clock. Use the CM06 bit in the CM0 register, and bits CM17 to CM16 in the CM1 register to select a frequency-divided value.

When fC is selected as the clock source for the CPU clock, it is not divided and is used directly as the CPU clock.

After reset, the fOCO-S divided by 8 is used as the CPU clock. Note that when entering stop mode or when the CM05 bit in the CM0 register is set to 1 (stop) in low-speed mode, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).

BCLK is a bus reference clock.

In memory expansion or microprocessor mode, a BCLK signal with the same frequency as the CPU clock can be output from the BCLK pin by setting the PM07 bit in the PM0 register to 0 (output enabled).

8.4.2 Peripheral Function Clocks (f1, fOCO40M, fOCO-F, fOCO-S, fC32, fC)

f1, fOCO40M, fOCO-F, fOCO-S, and fC32 are operating clocks for the peripheral functions.

f1 is produced from one of the following:

- Main clock divided by 1 (no division)
- PLL clock divided by 1 (no division)
- fOCO-S divided by 1 (no division)
- fOCO-F divided by 1 (no division)

f1 is used for timers A and B, PWM, real-time clock, remote control signal receiver, UART0 to UART2, UART5 to UART7, SI/O3, SI/O4, multi-master I^2C-bus interface, and the A/D converter.

When the WAIT instruction is executed after setting the CM02 bit in the CM0 register to 1 (peripheral function clock f1 turned off during wait mode), the f1 clock is stopped.

fOCO40M can be used for A/D converter. fOCO40M can be used when the FRA00 bit in the FRA0 register is 1 (40 MHz on-chip oscillator on).

fOCO-F can be used for timers A and B, UART0 to UART2, UART5 to UART7, SI/O3, and SI/O4. fOCO-F can be used when the FRA00 bit in the FRA0 register is 1 (40 MHz on-chip oscillator on).

fOCO-S is used for timers A and B. It is also used for reset, voltage detector and watchdog timer. fOCO-S is also used when the CM14 bit in the CM1 register is set to 0 (125 kHz on-chip oscillator on).

fC is divided by 32 to produce fC32. fC32 is used for timers A and B, and is enabled when the sub clock is on.

fC is used for the watchdog timer. fC is also used as the clock source for the real-time clock, remote control signal receiver, and CEC function, when the PM25 bit in the PM2 register is 1 (peripheral clock fC provided). fC can be used when the sub clock is on.

Figure 8.5 shows Peripheral Function Clocks.

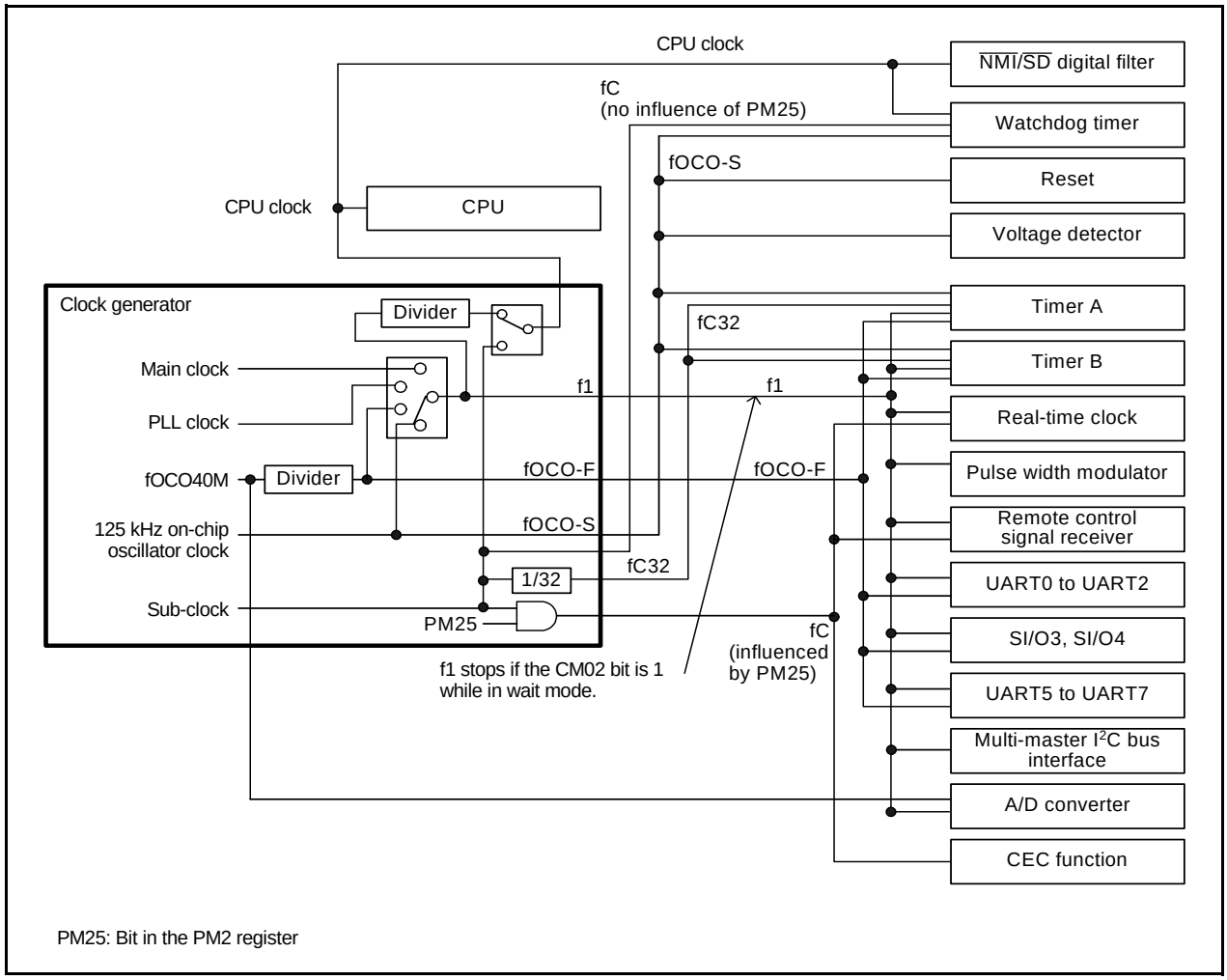


Figure 8.5 Peripheral Function Clocks

8.5 Clock Output Function

In single-chip mode, the f1, f8, f32 or fC clock can be output from the CLKOUT pin. Use bits CM01 to CM00 in the CM0 register, and the PCLK5 bit in the PCLKR register to select the clock. f8 has the same frequency as f1 divided by 8, and f32 has the same frequency as f1 divided by 32.
Set the frequency of a clock output from the CLKOUT pin to 25 MHz or below.

8.6 System Clock Protection Function

The system clock protection function prohibits the CPU clock from changing clock sources when the main clock is selected as the CPU clock source. This is to prevent the CPU clock from stopping due to an unexpected program operation.
When the PM21 bit in the PM2 register is set to 1 (clock change disabled), the following bits remain unchanged even if they are written to.

- The CM02 bit in the CM0 register (peripheral function clock f1 in wait mode)
- The CM05 bit in the CM0 register (to prevent the main clock from being stopped)
- The CM07 bit in the CM0 register (clock source of the CPU clock)
- The CM10 bit in the CM1 register (stop mode is not entered)
- The CM11 bit in the CM1 register (clock source of the CPU clock)
- The CM20 bit in the CM2 register (oscillation stop/re-oscillation detect function set)
- All bits in the PLC0 register (PLL frequency synthesizer set)

To use the system clock protect function, set the CM05 bit in the CM0 register to 0 (main clock oscillation) and CM07 bit to 0 (main clock as CPU clock source), and then follow the procedures below.

(1) Set the PRC1 bit in the PRCR register to 1 (write to PM2 register enabled).
(2) Set the PM21 bit in the PM2 register to 1 (clock change disabled).
(3) Set the PRC1 bit in the PRCR register to 0 (write to PM2 register disabled).

When the PM21 bit is 1, do not execute the WAIT instruction.

8.7 Oscillation Stop/Re-Oscillation Detect Function

This function is to detect the stop and re-oscillation of the main clock oscillation circuit. The oscillation stop and re-oscillation detect function can be enabled and disabled with the CM20 bit in the CM2 register. A reset or oscillation stop/re-oscillation detection interrupt is generated when an oscillation stop or re-oscillation is detected. Set the CM27 bit in the CM2 register to select the reset or interrupt.
Table 8.6 lists Specification Overview of Oscillation Stop and Re-Oscillation Detect Function.

Table 8.6 Specification Overview of Oscillation Stop and Re-Oscillation Detect Function

Item	Specification
Oscillation stop detectable clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Enabling condition for oscillation stop/ re-oscillation detect function	Set CM20 bit to 1 (enabled)
Operation at oscillation stop/ re-oscillation detection	When CM27 bit is 0: Oscillation stop detection reset generated When CM27 bit is 1: Oscillation stop/re-oscillation detection interrupt generated

8.7.1 Operation When CM27 Bit is 0 (Oscillation Stop Detection Reset)

When main clock stop is detected while the CM20 bit is 1 (oscillation stop/re-oscillation detection function enabled), the MCU is initialized, and then stops (oscillation stop reset). (Refer to 4. “Special Function Registers (SFRs)” and 6. “Resets”.)
The status is cancelled at hardware reset or voltage monitor 0 reset. The MCU can also be initialized and stopped when re-oscillation is detected, but do not use the MCU in this manner (during main clock stop, do not set the CM20 bit to 1 and the CM27 bit to 0).

8.7.2 Operation When CM27 Bit is 1 (Oscillation Stop, Re-Oscillation Detect Interrupt)

When the CM20 bit is 1 (oscillation stop/re-oscillation detect function enabled), the system is placed in the state shown in Table 8.7 if the main clock detects oscillation stop or re-oscillation.
The CM21 bit is automatically set to 1 in high-speed, medium-speed, or low-speed mode. The FRA01 bit does not change. Thus, high-speed and medium-speed mode become 125 kHz on-chip oscillator mode or 40 MHz on-chip oscillator mode. Because the CM07 bit does not change, low-speed mode remains in low-speed mode, but clock sources for the peripheral functions become fOCO-S or fOCO-F.

When the CM21 bit is set to 1, the CM14 bit is set to 0 (125 kHz on-chip oscillator on), but the FRA00 bit remains unchanged (40 MHz on-chip oscillator does not oscillate automatically). Thus, when the FRA01 bit is set to 1 (40 MHz on-chip oscillator selected), set the FRA00 bit to 1 (40 MHz on-chip oscillator on). Do not set the FRA00 bit to 0 while the FRA01 bit is 1, and vice versa.
Since the CM21 bit remains unchanged in PLL operating mode, select 125 kHz on-chip oscillator mode or 40 MHz on-chip oscillator mode inside the interrupt routine.

Table 8.7 State after Oscillation Stop and Re-Oscillation Detect When CM27 Bit is 1

Condition		After Detection
Main clock oscillation stop detected	High-speed mode Medium-speed mode	• Oscillation stop, re-oscillation detection interrupt is generated • CM14 bit is 0 (125 kHz on-chip oscillator on) • CM21 bit is 1 (fOCO-S or fOCO-F is used as the clock source for the CPU and peripheral function clocks) (1), (2) • CM22 bit is 1 (main clock stop detected) • CM23 bit is 1 (main clock stopped)
	Low-speed mode	
	40 MHz on-chip oscillator mode	
	125 kHz on-chip oscillator mode	
	PLL operating mode	• Oscillation stop, re-oscillation detection interrupt is generated • CM14 bit is 0 (125 kHz on-chip oscillator on) • CM21 bit remains unchanged • CM22 bit is 1 (main clock stop detected) • CM23 bit is 1 (main clock stopped)
Main clock re-oscillation detected	-	• Oscillation stop, re-oscillation detection interrupt is generated • CM14 bit is 0 (125 kHz on-chip oscillator on) • CM21 bit remains unchanged • CM22 bit is 1 (main clock stop detected) • CM23 bit is 0 (main clock oscillating)

Notes:
1. fOCO-S or fOCO-F is selected depending on the FRA01 bit status.
2. fC is used as the CPU clock in low-speed mode.

8.7.3 Using the Oscillation Stop, Re-Oscillation Detect Function

- The oscillation stop/re-oscillation detect interrupt shares a vector with the watchdog timer interrupt, voltage monitor 1 interrupt, and voltage monitor 2 interrupt. If the oscillation stop/re-oscillation detection interrupt is used with a watchdog timer interrupt, voltage monitor 1 interrupt, or voltage monitor 2 interrupt, read the CM22 bit (oscillation stop/re-oscillation detection), VW1C2 bit (Vdet1 passage detection), VW2C2 bit (Vdet2 passage detection) and VW2C3 bit (watchdog timer underflow detection) in an interrupt routine to determine which interrupt source is requesting the interrupt.
- After oscillation stop is detected, if the main clock re-oscillates, set the main clock back to the clock source for the CPU clock and peripheral functions by a program. Figure 8.6 shows the Procedure to Switch Clock Source from On-Chip Oscillator to Main Clock.

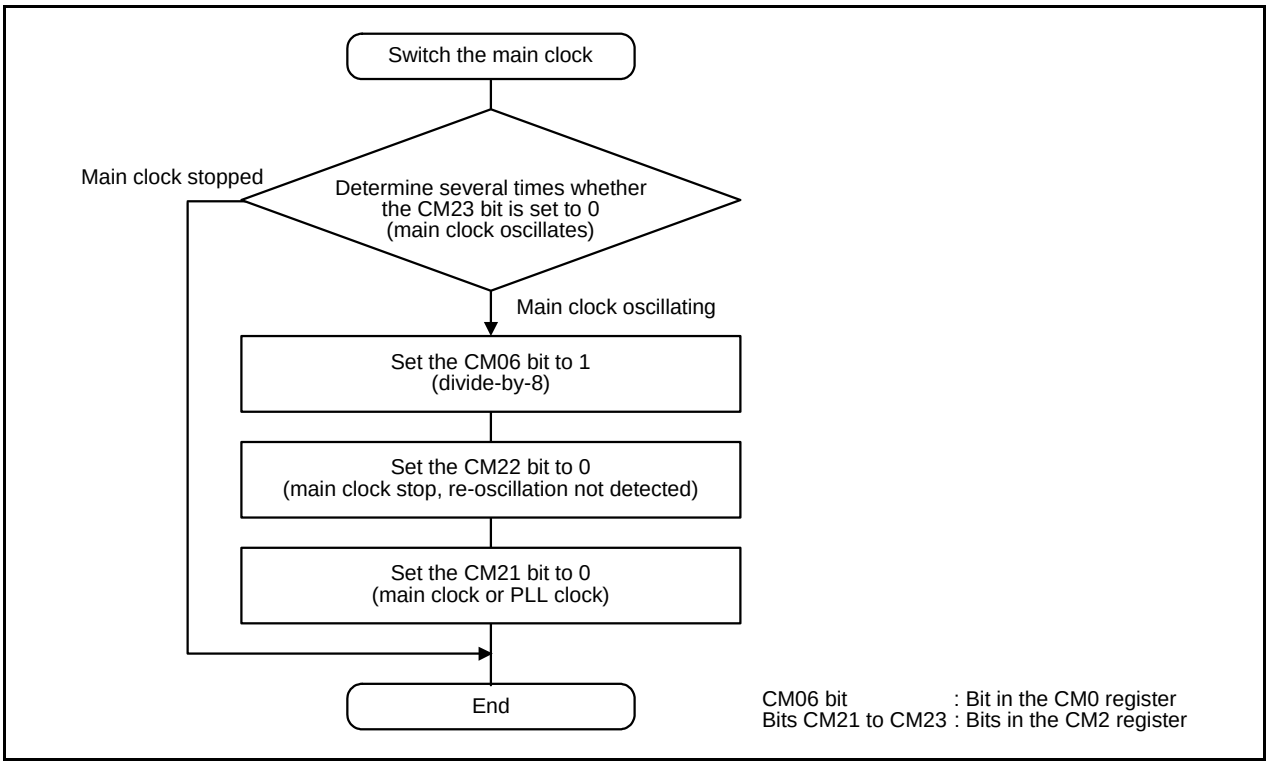


Figure 8.6 Procedure to Switch Clock Source from On-Chip Oscillator to Main Clock

- The CM22 bit becomes 1 at the same time an oscillation stop/re-oscillation detection interrupt is generated. When the CM22 bit is 1, the oscillation stop/re-oscillation detection interrupt is disabled. When setting the CM22 bit to 0 by a program, the oscillation stop/re-oscillation detection interrupt is enabled.

8.8 Notes on Clock Generator

8.8.1 Oscillation Circuit Using an Oscillator

To connect an oscillator, follow these instructions:

- The oscillation characteristics are tied closely to the user's board design. Perform a careful evaluation of the board before connecting an oscillator.
- Oscillation circuit structure depends on the oscillator. The M16C/65 Group contains a feedback resistor, but an external feedback resistor may be required. Contact the oscillator manufacturer regarding circuit constants, as they are dependent on the oscillator or stray capacitance of the mounted circuit.
- Check output from the CLKOUT pin to confirm that the clock generated by the oscillation circuit is properly transmitted to the MCU. Procedures for outputting a clock from the CLKOUT pin are listed below. Set the clock output from the CLKOUT pin to 25 MHz or below.

Outputting the main clock

(1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
(2) Set the CM11 bit in the CM1 register to 0, the CM07 bit in the CM0 register to 0, and the CM21 bit in the CM2 register to 0 (main clock selected).
(3) Select the clock output from the CLKOUT pin (refer to the following table).
(4) Set the PRC0 bit in the PRCR register to 0 (write disabled)

Table 8.8 Output from CLKOUT Pin When Selecting Main Clock

Bit Setting		Output from CLKOUT Pin
PCLKR Register	CM0 Register	
PCLK5 Bit	Bits CM01 to CM00	
1	00b	Clock with the same frequency as the main clock
0	10b	Main clock divided by 8
0	11b	Main clock divided by 32

Outputting the sub clock

(1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
(2) Set the CM07 bit in the CM0 register to 1 (sub clock selected).
(3) Set the PCLK5 bit in the PCLKR register to 0, and bits CM01 to CM00 in the CM0 register to 01b (fC output from CLKOUT pin).
(4) Set the PRC0 bit in the PRCR register to 0 (write disabled)

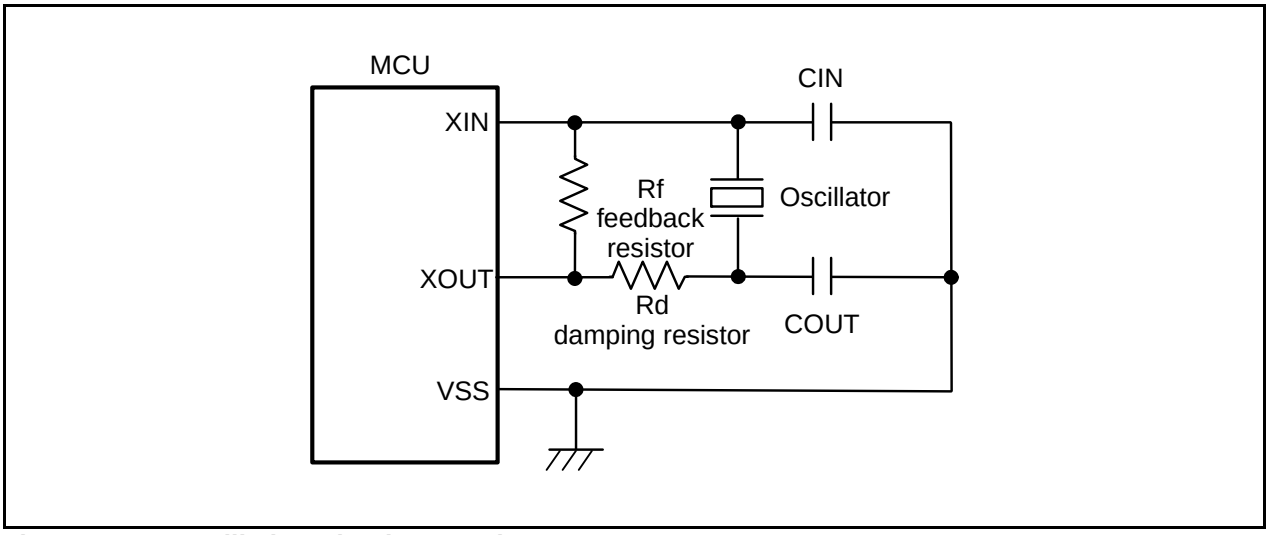


Figure 8.7 Oscillation Circuit Example

8.8.2 Noise Countermeasure

8.8.2.1 Clock I/O Pin Wiring

- Connect the shortest possible wiring to the clock I/O pin.
- Connect (a) the capacitor's ground lead connected to the oscillator, and (b) the MCU's VSS pin, with the shortest possible wiring (maximum 20 mm).

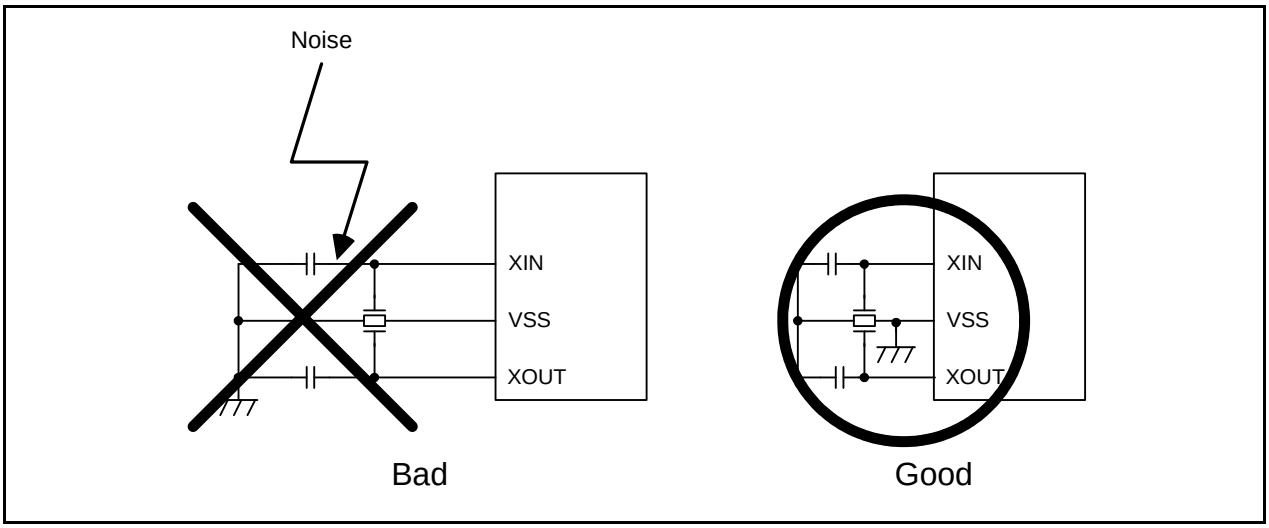


Figure 8.8 Clock I/O Pin Wiring

Reason

If noise enters the clock I/O pin, the clock waveform becomes unstable, which causes an error in operation or a program runaway. Also, if a potential difference attributed to the noise occurs between the VSS level of the MCU and the VSS level of the oscillator, an accurate clock is not input to the MCU.

8.8.2.2 Large Current Signal Line

For large currents that go above the MCU's current range, wire the signal lines as far away from the MCU as possible (especially the oscillator).

Reason

In the system using the MCU, there are signal lines for controlling motors, LEDs, and thermal heads. When a large current flows through these signal lines, noise is generated due to mutual inductance.

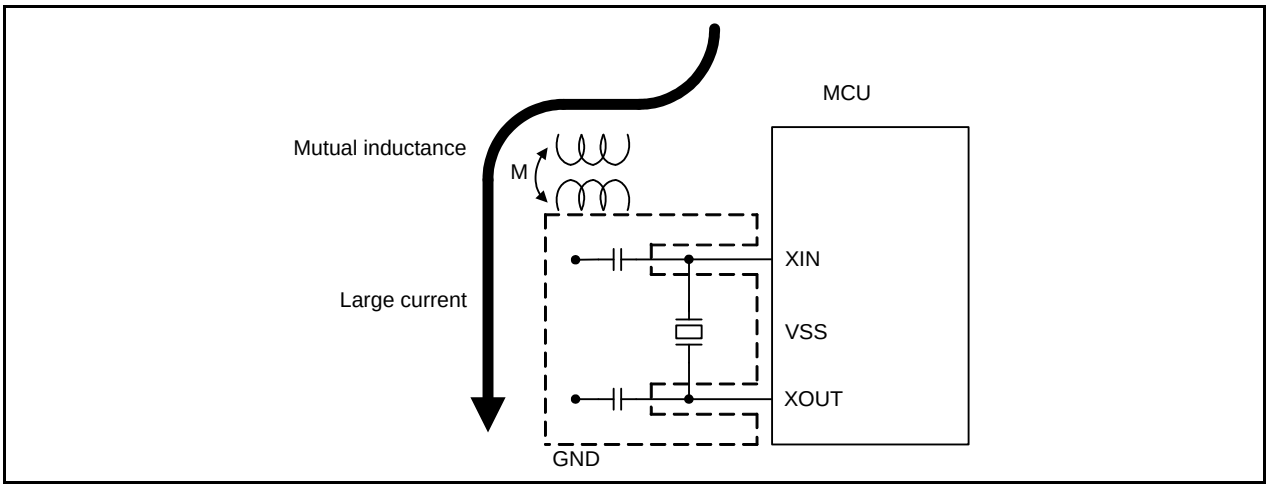


Figure 8.9 Large Current Signal Line Wiring

8.8.2.3 Signal Line Whose Level Changes at a High-Speed

For a signal line whose level changes at a high-speed, wire it as far away from the oscillator and the oscillator wiring pattern as possible. Do not wire it across or extend it parallel to a clock-related signal line or other signal lines which are sensitive to noise.

Reason
A signal whose level changes at a high-speed (such as the signal from the TAOUT pin) affects other signal lines due to the level change at rising or falling edges. Specially when the signal line crosses the clock-related signal line, the clock waveform becomes unstable, which causes an error in operation or a program runaway.

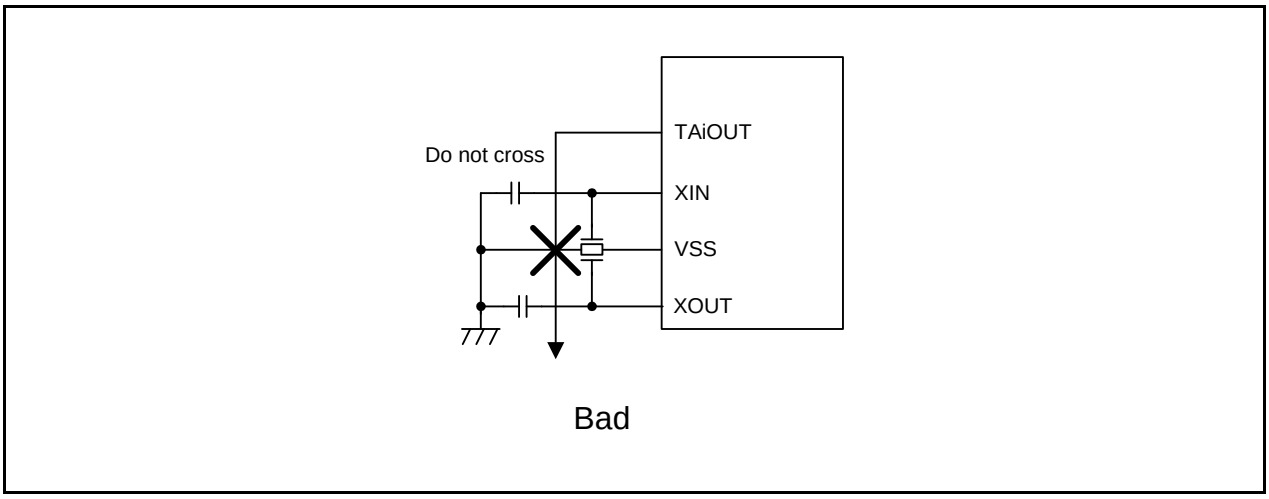


Figure 8.10 Wiring of Signal Line Whose Level Changes at High-Speed

8.8.3 CPU ClockW

- When the external clock is entered from the XIN pin and the main clock is used as the CPU clock, do not stop the external clock.

8.8.4 Oscillation Stop, Re-Oscillation Detect Function

- In the following cases, set the CM20 bit to 0 (oscillation stop/re-oscillation detect function disabled), and then change the status of each bit.
  When the CM05 bit is set to 1 (main clock stopped)
  When the CM10 bit is set to 1 (stop mode)
- To enter wait mode while using the oscillation stop/re-oscillation detection function, set the CM02 bit to 0 (peripheral function clock f1 not turned off during wait mode).
- This function cannot be used if the main clock frequency is 2 MHz or below. In that case, set the CM20 bit to 0 (oscillation stop/re-oscillation detect function disabled).
- While the CM27 bit is 1 (oscillation stop/re-oscillation detect interrupt), when the FRA01 bit is 1 (40 MHz on-chip oscillator selected), set the FRA00 bit to 1 (40 MHz on-chip oscillator on). (Do not set the FRA00 bit to 0 while FRA01 bit is 1, and vice versa.)

8.8.5 PLL Frequency Synthesizer

To use the PLL frequency synthesizer, stabilize the supply voltage to meet the power supply ripple standard.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f (ripple)	Power supply ripple allowable frequency (V_{CC1})				10	kHz
V_{P-P} (ripple)	Power supply ripple allowable amplitude voltage	(V_{CC1} = 5 V)			0.5	V
		(V_{CC1} = 3 V)			0.3	V
V_{CC} ($\lvert\Delta V / \Delta T\rvert$)	Power supply ripple rising/falling gradient	(V_{CC1} = 5 V)			0.3	V/ms
		(V_{CC1} = 3 V)			0.3	V/ms

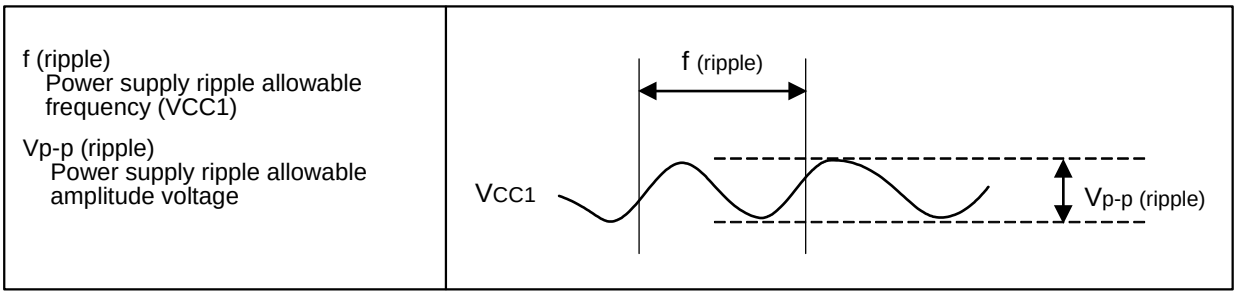


Figure 8.11 Voltage Fluctuation Timing

9. Power Control

9.1 Introduction

The following describes how to reduce the amount of current consumption.

9.2 Registers

Refer to 8. “Clock Generator” for the clock-related registers.

Table 9.1 Register Structure

Address	Register Name	Symbol	After Reset
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b

9.2.1 Flash Memory Control Register 0 (FMR0)

Flash Memory Control Register 0

Symbol	Address	After Reset
FMR0	0220h	0000 0001b (other than user boot mode) 0010 0001b (user boot mode)

b7 b6 b5 b4 b3 b2 b1 b0
0 0

Bit Symbol	Bit Name	Function	RW
FMR00	RY/$\overline{BY}$ status flag	0 : Busy (being written or erased) 1 : Ready	RO
FMR01	CPU rewrite mode select bit	0 : CPU rewrite mode disabled 1 : CPU rewrite mode enabled	RW
FMR02	Lock bit disable select bit	0 : Lock bit enabled 1 : Lock bit disabled	RW
FMSTP	Flash memory stop bit	0 : Flash memory operation enabled 1 : Flash memory operation stopped (placed in low power mode, flash memory initialized)	RW
— (b4)	Reserved bit	Set to 0	RW
— (b5)	Reserved bit	Set to 0 in other than user boot mode. Set to 1 in user boot mode.	RW
FMR06	Program status flag	0 : Terminated normally 1 : Terminated in error	RO
FMR07	Erase Status Flag	0 : Terminated normally 1 : Terminated in error	RO

FMR01 (CPU Rewrite Mode Select Bit) (b1)

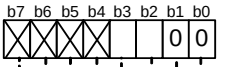
To set the FMR01 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers occur before writing 1 after writing 0.
In EW0 mode, write to this bit by a program in any area other than the flash memory.
Enter read array mode first to set this bit to 0.

FMSTP (Flash Memory Stop Bit) (b3)

Write to the FMSTP bit by a program in any area other than the flash memory.
The FMSTP bit is enabled when the FMR01 bit is 1 (CPU rewrite mode). When the FMR01 bit is 0, although the FMSTP bit can be set to 1, the flash memory is neither placed in low power mode nor initialized.
When the FMR23 bit is 1 (low current consumption read mode enabled), do not set the FMSTP bit to 1 (flash memory stopped). Also, when the FMSTP bit is 1, do not set the FMR23 bit to 1.

9.2.2 Flash Memory Control Register 2 (FMR2)

Flash Memory Control Register 2



Symbol: FMR2 | Address: 0222h | After Reset: XXXX 0000b

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
FMR22	Slow read mode enable bit	0 : Disabled 1 : Enabled	RW
FMR23	Low current consumption read mode enable bit	0 : Disabled 1 : Enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value		—

FMR22 (Slow Read Mode Enable Bit) (b2)

This bit enables mode which reduces the amount of current consumption when reading the flash memory. When rewriting the flash memory (CPU rewrite mode), set the FMR22 bit to 0 (slow read mode disabled).
Slow read mode can be used when f(BCLK) is 5 MHz or below. When f(BCLK) is above 5 MHz, set the FMR22 bit to 0 (slow read mode disabled).
To set the FMR22 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers occur before writing 1 and after writing 0.
Set the FMR23 bit to 1 (low current consumption read mode enabled) after the FMR22 bit is set to 1 (slow read mode enabled). Also, set the FMR22 bit to 0 (slow read mode disabled) after the FMR23 bit is set to 0 (slow read mode disabled). Do not change the FMR22 bit and FMR23 bit at the same time.

FMR23 (Low Current Consumption Read Mode Enable Bit) (b3)

When this bit is enabled, the slow read mode reduces the amount of current consumption when reading the flash memory. When rewriting the flash memory (CPU rewrite mode), set the FMR23 bit to 0 (slow read mode disabled).
Low current consumption read mode can be used when the CM07 bit in the CM0 register is 1 (sub clock used as CPU clock). When the CM07 bit is 0, set the FMR23 bit to 0 (slow read mode disabled).
To set the FMR23 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers occur before writing 1 and after writing 0.
Set the FMR23 bit to 1 (low current consumption read mode enabled) after the FMR22 bit is set to 1 (slow read mode enabled). Also, set the FMR22 bit to 0 (slow read mode disabled) after the FMR23 bit is set to 0 (slow read mode disabled). Do not change bits FMR22 and FMR23 at the same time.
When the FMR23 bit is 1, do not set the FMSTP bit in the FMR0 register to 1 (flash memory stopped). Also, when the FMSTP bit is 1, do not set the FMR23 bit to 1.
When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not enter wait mode or stop mode. To enter wait mode or stop mode, set the FMR23 bit to 0 (low current consumption read mode disabled) before entering.

9.3 Clock

The amount of current consumption correlates with the number of operating clocks and frequency. If there are fewer operating clocks and a lower frequency, current consumption will be low.
Normal operating mode, wait mode, and stop mode are provided to control power consumption. All mode states, except wait mode and stop mode, are called normal operating mode in this document.

9.3.1 Normal Operating Mode

In normal operating mode, because both the CPU clock and the peripheral function clocks are supplied, the CPU and the peripheral functions are operating. Power control is exercised by controlling the CPU clock frequency. The higher the CPU clock frequency, the greater the processing capability. The lower the CPU clock frequency, the smaller the power consumption in the chip. If unnecessary oscillator circuits are turned off, power consumption is further reduced.

9.3.1.1 High-Speed Mode and Medium-Speed Mode

In high-speed mode, the main clock divided by 1 (no division) is used as the CPU clock.
In medium-speed mode, the main clock divided by 2, 4, 8 or 16 is used as the CPU clock.
f1 with the same frequency of the main clock divided by 1 is used as the peripheral function clocks in both high-speed and medium-speed modes. When fC is supplied, fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

9.3.1.2 PLL Operating Mode

The PLL clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the PLL clock divided by 1 (no division) is used as the peripheral function clocks.
When fC is supplied, fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.
PLL operating mode can be entered and exited from high-speed mode or medium-speed mode. To enter other modes including wait mode and stop mode, enter high-speed mode or medium-speed mode first, and then enter the intended mode (refer to Figure 9.1 “Clock Mode Transition”).

9.3.1.3 40 MHz On-Chip Oscillator Mode

The fOCO-F clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the fOCO-F clock divided by 1 is used as the peripheral function clocks.
When fC is supplied, fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. fOCO40M and fOCO-F can be used as the peripheral function clocks.

9.3.1.4 125 kHz On-Chip Oscillator Mode

The fOCO-S clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the fOCO-S clock divided by 1 is used as the peripheral function clocks.

When fC is supplied, fC and fC32 can be used as the peripheral function clocks. fOCO-S can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

9.3.1.5 125 kHz On-Chip Oscillator Low Power Mode

The main clock and fOCO-F are turned off after the MCU enters 125 kHz on-chip oscillator mode. The fOCO-S clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. f1 with the same frequency of the fOCO-S clock divided by 1 is used as the peripheral function clocks.

When fC is supplied, fC and fC32 can be used as the peripheral function clocks. fOCO-S can be used as the peripheral function clocks.

9.3.1.6 Low-Speed Mode

fC is used as the CPU clock.

When the CM21 bit is 0 and the CM11 bit is 0 (main clock), f1 with the same frequency of the main clock divided by 1 is used as the peripheral function clocks. When the CM21 bit is 0 and the CM11 bit is 1 (PLL clock), f1 with the same frequency of the PLL clock divided by 1 is used as the peripheral function clocks. When the CM21 bit is 1 (on-chip oscillator clock) and the FRA01 bit is 0 (125 kHz on-chip oscillator clock), f1 with the same frequency of the fOCO-S clock divided by 1 is used as the peripheral function clocks. When the CM21 bit is 1 (on-chip oscillator clock) and the FRA01 bit is 1 (40 MHz on-chip oscillator clock), f1 with the same frequency of the fOCO-F clock divided by 1 is used as the peripheral function clocks.

fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks. When fOCO40M and fOCO-F are supplied, they can be used as the peripheral function clocks.

9.3.1.7 Low Power Mode

The main clock and fOCO-F are turned off after the MCU enters low speed mode. fC is used as the CPU clock. When the CM21 bit is 1 (on-chip oscillator clock) and the FRA01 bit is 0 (125 kHz on-chip oscillator clock), f1 with the same frequency of the fOCO-S clock divided by 1 is used as the peripheral function clocks.

fC and fC32 can be used as the peripheral function clocks. When fOCO-S is supplied, it can be used as the peripheral function clocks.

When this mode is selected, the CM06 bit in the CM0 register simultaneously becomes 1 (divide- by-8 mode). In low power mode, do not change the CM06 bit. Consequently, select the divide-by-8 mode when any clock (except the sub clock) is used for the next operation.

Table 9.2 Clocks in Normal Operating Mode

Mode	CPU Clock	Peripheral Clocks			
		f1	fC, fC32	fOCO-S	fOCO-F fOCO40M
High-speed mode	Main clock divided by 1 (1)	Main clock divided by 1	Enabled (2)	Enabled (3)	Enabled (4)
Medium-speed mode	Main clock divided by n (1)				
PLL operating mode	PLL clock divided by n (1)	PLL clock divided by 1			
40 MHz on-chip oscillator mode	fOCO-F divided by n (1)	fOCO-F divided by 1	Enabled (2)	Enabled (3)	Enabled
125 kHz on-chip oscillator mode	fOCO-S divided by n (1)	fOCO-S divided by 1	Enabled (2)	Enabled	Enabled (4)
125 kHz on-chip oscillator low power mode	fOCO-S divided by n (1)	fOCO-S divided by 1	Enabled (2)	Enabled	Disabled
Low-speed mode	fC	Any of the following: Main clock divided by 1 (when the CM21 is 0 and the CM11 is 0) (5) PLL clock divided by 1 (when the CM21 is 0 and the CM11 is 1) (6) fOCO-F divided by 1 (when the CM21 is 1 and the FRA01 is 1) (4) fOCO-S divided by 1 (when the CM21 is 0 and the FRA01 is 0) (3)	Enabled	Enabled (3)	Enabled (4)
Low power mode	fC	fOCO-S divided by 1 (when the CM21 is 1 and the FRA01 is 0) (3)	Enabled	Enabled (3)	Disabled

CM11 : Bit in the CM1 register
CM21 : Bit in the CM2 register
FRA01 : Bit in the FRA0 register
Notes:
1. Select by using the CM06 bit in the CM0 register and bits CM17 to CM16 in the CM1 register.
2. When the fC is supplied.
3. When the fOCO-S is supplied.
4. When the fOCO40M and fOCO-F are supplied.
5. When the main clock is supplied.
6. When the PLL clock is supplied.

Table 9.3 Clock Related Bit Setting and Modes

Mode	CM2 Register	CM1 Register		CM0 Register			FRA0 Register	
	CM21	CM14	CM11	CM07	CM05	CM04	FRA01	FRA00
High-speed mode, medium-speed mode	0	-	0	0	0	-	-	-
PLL operating mode	0	-	1	0	0	-	-	-
40 MHz on-chip oscillator mode	1	-	0	0	-	-	1	1
125 kHz on-chip oscillator mode	1	0	0	0	0 (1)	-	0	1 (1)
125 kHz on-chip oscillator low power mode	1	0	0	0	1	-	0	0
Low-speed mode	-	-	0	1	0 (1)	1	-	1 (1)
Low power mode	-	-	0	1	1	1	-	0

Note:
1. Both or either the main clock and fOCO-F are oscillated

Table 9.4 Selecting Clock Division Related Bits (1)

Division	CM1 Register	CM0 Register
	Bits CM17 to CM16	CM16 bit
Divide-by-1 (no division) (2)	00b	0
Divide-by-2	01b	0
Divide-by-4	10b	0
Divide-by-8	-	1
Divide-by-16	11b	0

Notes:
1. While in high-speed mode, medium-speed mode, PLL operating mode, 125 kHz on-chip oscillator mode, or 125 kHz on-chip oscillator low power mode.
2. Select divide-by-1 (no division) in high-speed mode.

Table 9.5 Example Settings for 40 MHz On-Chip Oscillator Mode Division Related Bits

Division	CPU Clock Frequency	CM1 Register	CM0 Register
		Bits CM17 to CM16	CM06 bit
Divide-by-2	Approx. 20 MHz	00b (divide-by-1 (no division))	0
Divide-by-4	Approx. 10 MHz	01b (divide-by-2)	0
Divide-by-8	Approx. 5 MHz	10b (divide-by-4)	0
Divide-by-16	Approx. 2.5 MHz	-	1 (divide-by-8)
Divide-by-32	Approx. 1.25 MHz	11b (divide-by-16)	0

9.3.2 Mode Transitions

Figure 9.1 shows Clock Mode Transition. Arrows indicate that mode transitions are enabled between modes.

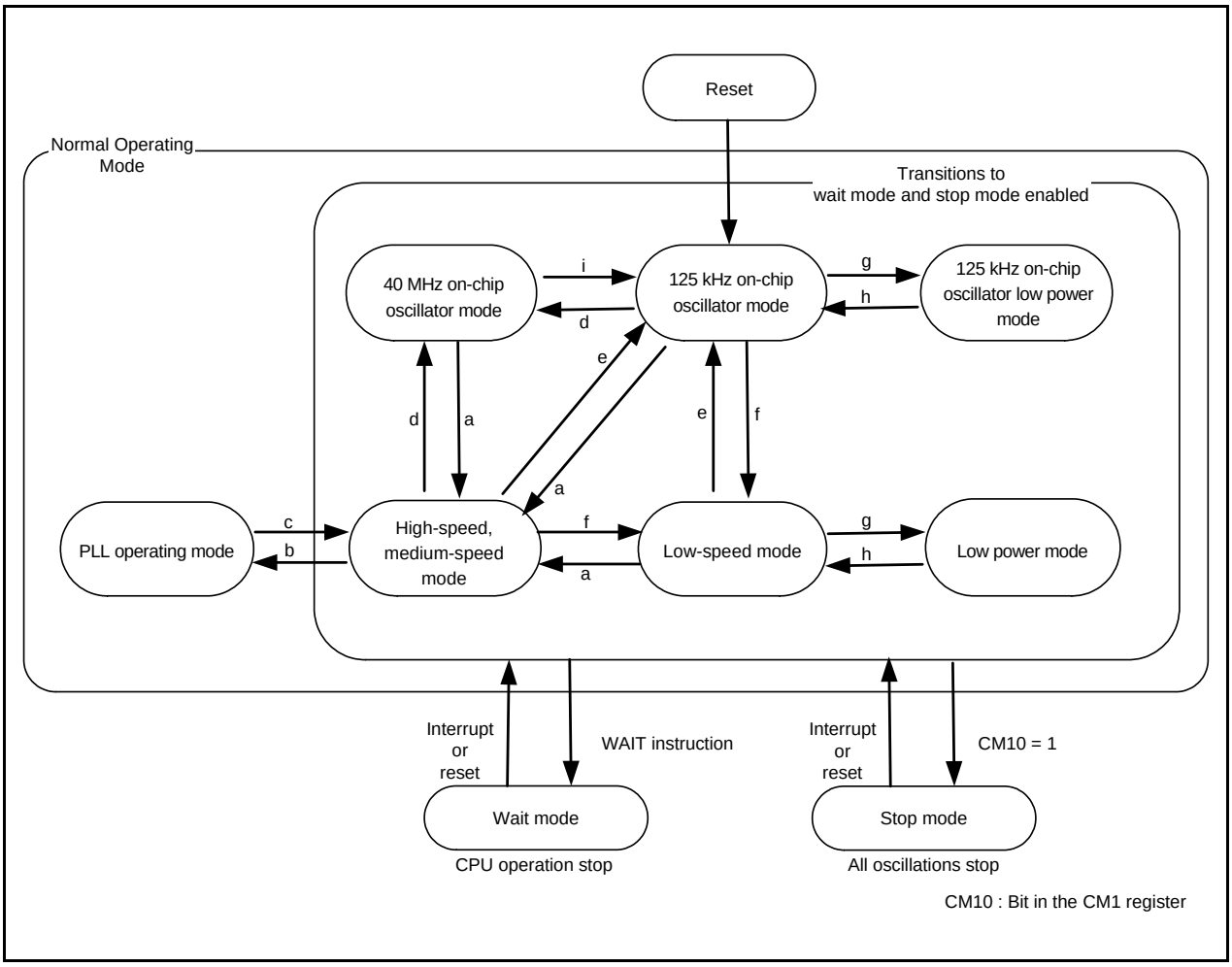


Figure 9.1 Clock Mode Transition

To start or stop clock oscillations, or to change modes in normal operating mode, follow the instructions below.

- Enter a mode after the clock for the mode entered stabilizes completely.
- To stop a clock, stop the clock for the mode exited after mode transition is completed. Do not stop the clock at the same time as mode transition.
- Execute mode transition according to the following procedures. To access registers and bits, see 9.2 “Registers”. Letters a to h correspond to those in Figure 9.1 “Clock Mode Transition”.
- For oscillation start and stop, see 8.3.1 “Main Clock” to 8.3.6 “Sub Clock (fC)”.

a.Entering high-speed mode or medium-speed mode from 40 MHz on-chip oscillator mode, 125 kHz on-chip oscillator mode, or low-speed mode

(1)Oscillate the main clock and wait until the oscillation stabilizes. See 8.3.1 “Main Clock”.
(2)Set the CM06 bit to 1 (divide-by-8 mode).
(3)Set the CM11 bit to 0, the CM21 bit to 0, and the CM07 bit to 0 (main clock selected as CPU clock source).

b.Entering PLL operating mode from high-speed mode or medium-speed mode

(1)Set a multiplying factor and reference frequency counter by using bits PLC05 to PLC04 and bits PLC02 to PLC00 in the PLC0 register.
(2)Specify wait for SFR accessing by the PM20 bit.
(3)Set the PLC07 bit to 1 (PLL on).
(4)Wait for tsu(PLL) until the PLL clock stabilizes.
(5)Set the CM11 bit to 1, the CM21 bit to 0, and the CM07 bit to 0 (PLL clock selected as CPU clock source).

c.Entering high-speed mode or medium-speed mode from PLL operating mode

(1)Select a divide ratio by setting the CM06 bit and bits CM17 to CM16.
(2)Set the CM11 bit to 0, the CM21 bit to 0, and the CM07 bit to 0 (main clock selected as CPU clock source).
(3)Set the PLC07 bit to 0 (PLL off).

d.Entering 40 MHz on-chip oscillator mode from high-speed mode, medium-speed mode, or 125 kHz on-chip oscillator mode

(1)Oscillate the 40 MHz on-chip oscillator and wait until the oscillation stabilizes. See 8.3.4 “fOCO-F”.
(2)Set the CM06 bit to 1 (divide-by-8 mode).
(3)Set the FRA01 bit to 1 (40 MHz on-chip oscillator).
(4)Set the CM21 bit to 1 (on-chip oscillator clock selected as CPU clock source).
(5)Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock selected as CPU clock source).

e.Entering 125 kHz on-chip oscillator mode from high-speed mode, medium-speed mode, or low-speed mode

(1)Oscillate the 125 kHz on-chip oscillator and wait until the oscillation stabilizes. See 8.3.5 “125 kHz On-Chip Oscillator Clock (fOCO-S)”.
(2)Set the FRA01 bit to 0 (125 kHz on-chip oscillator).
(3)Set the CM21 bit to 1 (on-chip oscillator clock selected as CPU clock source).
(4)Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock selected as CPU clock source).

f.Entering low-speed mode from high-speed mode, medium-speed mode, or 125 kHz on-chip oscillator mode

(1)Oscillate the sub clock and wait until the oscillation stabilizes. See 8.3.6 “Sub Clock (fC)”.
(2)Set the CM07 bit to 1 (sub clock selected as CPU clock source).

g.Entering 125 kHz on-chip oscillator low power mode from 125kHz on-chip oscillator mode
Entering low power mode from low-speed mode
Follow both or either of the procedures below (in no particular order).

(1)Stop oscillating the main clock. See 8.3.1 “Main Clock”
(2)Stop oscillating the 40 MHz on-chip oscillator. See 8.3.4 “fOCO-F”.

h.Entering 125 kHz on-chip oscillator mode from 125 kHz on-chip oscillator low power mode
Entering low-speed mode from low power mode
Follow both or either of the procedures below (in no particular order).
(1)Oscillate the main clock and wait until the oscillation stabilizes. See 8.3.1 “Main Clock”.
(2)Oscillate the 40 MHz on-chip oscillator and wait until the oscillation stabilizes. See 8.3.4 “fOCO-F”.

i.Entering 125 kHz on-chip oscillator mode from 40 MHz on-chip oscillator mode
(1)Oscillate the 125 kHz on-chip oscillator and wait until the oscillation stabilizes. See 8.3.5 “125 kHz On-Chip Oscillator Clock (fOCO-S)”.
(2)Set the CM06 bit to 1 (divide-by-8 mode).
(3)Set the FRA01 bit to 0 (125 kHz on-chip oscillator).
(4)Set the CM21 bit to 1 (on-chip oscillator clock selected as CPU clock source).
(5)Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock selected as CPU clock source).

9.3.3 Wait Mode

In wait mode, the CPU clock, CPU, watchdog timer, and $\overline{NMI}$/$\overline{SD}$ digital filter are turned off as they are operated by the CPU clock. However, if the CSPRO bit in the CSPR register is 1 (count source protection enabled), the watchdog timer remains active. Because the main clock, fOCO-F, fOCO-S, and fC do not stop, the peripheral functions using these clocks keep operating.

9.3.3.1 Peripheral Function Clock Stop Function

When the CM02 bit is 1 (peripheral function clock f1 turned off during wait mode), the f1 clock is turned off while in wait mode, and power consumption is reduced. However, all the peripheral clocks except f1 (i.e. fOCO-F, fOCO-S, fC, and fC32) do not stop.

9.3.3.2 Entering Wait Mode

The MCU enters wait mode by executing a WAIT instruction.
When the CM11 bit is 1 (PLL clock selected as CPU clock source), set the CM11 bit to 0 (main clock selected as CPU clock source) before entering wait mode. Chip power consumption can be reduced by setting the PLC07 bit to 0 (PLL off).

9.3.3.3 Pin Status in Wait Mode

Table 9.6 lists Pin Status in Wait Mode.

Table 9.6 Pin Status in Wait Mode

Pin		Memory Expansion Mode Microprocessor Mode	Single-Chip Mode
A0 to A19, D0 to D15, $\overline{CS0}$ to $\overline{CS3}$, $\overline{BHE}$		Retains the status just prior to entering wait mode	Cannot be used as a bus control pin
$\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{WRH}$		High	
$\overline{HLDA}$, BCLK		High	
ALE		Low	
I/O ports		Retains the status just prior to entering wait mode	Retains the status just prior to entering wait mode
CLKOUT	fC selected	Cannot be used as a CLKOUT pin	Does not stop
	f1, f8, f32 selected		Does not stop when the CM02 bit is 0. When the CM02 bit is 1, the status immediately prior to entering wait mode is maintained

9.3.3.4 Exiting Wait Mode

The MCU exits wait mode by a reset or interrupt. Table 9.7 lists Resets and Interrupts to Exit Wait Mode and Conditions for Use.

The peripheral function interrupts are affected by the CM02 bit. When the CM02 bit is 0 (peripheral function clock f1 not turned off in wait mode), peripheral function interrupts can be used to exit wait mode. When the CM02 bit is 1 (peripheral function clock f1 turned off in wait mode), the peripheral functions using the peripheral function clock f1 stop operating, so that the peripheral functions activated by external signals and the peripheral function clocks except f1 (fOCO40M, fOCO-F, fOCO-S, fC, fC32) can be used to exit wait mode.

The fOCO-S is also used for the digital filter in the voltage detection circuit, so wait mode is exited when the digital filter is disabled or when the fOCO-S is supplied.

Table 9.7 Resets and Interrupts to Exit Wait Mode and Conditions for Use

Interrupt, Reset			Conditions for Use	
			CM02 = 0	CM02 = 1
Interrupt	Peripheral function interrupt	$\overline{\text{INT}}$	Usable	Usable
		Key input	Usable	Usable
		timer A, timer B	Usable in all modes	Usable when fOCO-F, fOCO-S or fC32 is supplied and is used as count source. Usable when counting external signals in event counter mode
		Remote control signal receiver	Usable	Usable when fC is supplied and is used as count source. Usable when fOCO-F, fOCO-S, or fC32 is supplied and is used as count source for timer B1 or B2, and timer B1 or B2 underflow is used as count source for remote control signal receiver.
		Serial interface	Usable in internal clock or external clock	Usable in external clock Usable when fOCO-F is supplied and is used as internal clock
		Multi-master I^2C-bus interface	Both I^2C-bus interface and SCL/SDA are usable	SCL/SDA is usable
		CEC function	Usable	Usable when fC is supplied and is used as count source.
		A/D converter	Usable in one-shot mode or single sweep mode	Usable when fOCO40M is supplied and is used as fAD in one-shot mode or single sweep mode
		Real-time clock	Usable when fC is supplied and is used as count source	
	Voltage detection 1, Voltage detection 2		Usable when the digital filter is disabled or fOCO-S is supplied	
	$\overline{\text{NMI}}$		Usable when the digital filter is disabled (bits NMIDF2 to NMIDF0 in the NMIDF register are 000b)	
Reset	Hardware reset		Usable	
	Voltage detection 0 reset, Voltage detection 1 reset, Voltage detection 2 reset		Usable when the digital filter is disabled or fOCO-S is supplied	
	Watchdog timer		Usable when count source protection mode is enabled (CSPRO = 1)	

When the MCU exits wait mode by hardware reset, voltage monitor 0 reset, voltage monitor 1 reset, voltage monitor 2 reset, watchdog timer reset, $\overline{\text{NMI}}$ interrupt, voltage monitor 1 interrupt, or voltage monitor 2 interrupt, set bits ILVL2 to ILVL0 in peripheral function interrupt to 000b (interrupt disabled) before executing the WAIT instruction.

When the MCU exits wait mode by peripheral function interrupts, make the following settings before executing a WAIT instruction:

(1) Set the interrupt priority level of bits ILVL2 to ILVL0 in the interrupt control register for peripheral function interrupts which are used to exit wait mode.
Set bits ILVL2 to ILVL0 in all other interrupt control registers, for peripheral function interrupts not used to exit wait mode, to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Start operating the peripheral functions used to exit wait mode.

When exiting wait mode by means of an interrupt, an interrupt routine is performed after an interrupt request is generated, and then the CPU clock is supplied again.
When the MCU exits wait mode by an interrupt, the CPU clock is the same CPU clock used while executing the WAIT instruction.

9.3.4 Stop Mode

In stop mode, all oscillator circuits, the CPU clock, and peripheral function clocks are turned off. Therefore, the CPU and the peripheral functions using these clocks stop operating. The least amount of power is consumed in this mode. If the voltage applied to pins VCC1 and VCC2 is VRAM or greater, the contents of internal RAM are retained. When applying 2.7 V or less to pins VCC1 and VCC2, make sure VCC1 ≥ VCC2 ≥ VRAM.

However, the peripheral functions activated by external signals keep operating.

9.3.4.1 Entering Stop Mode

The MCU enters stop mode by setting the CM10 bit in the CM1 register to 1 (all clocks turned off). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode), and the CM15 bit in the CM1 register is set to 1 (main clock oscillator circuit drive capability high).

Before entering stop mode, set the CM20 bit to 0 (oscillation stop/re-oscillation detection function disabled).

Also, when the CM11 bit is 1 (PLL clock used as the CPU clock source), set the CM11 bit to 0 (main clock used as the CPU clock source), and then the PLC07 bit to 0 (PLL turned off) before entering stop mode.

9.3.4.2 Pin Status in Stop Mode

Table 9.8 lists Pin Status in Stop Mode.

Table 9.8 Pin Status in Stop Mode

Pin		Memory Expansion Mode Microprocessor Mode	Single-Chip Mode
A0 to A19, D0 to D15, $\overline{CS0}$ to $\overline{CS3}$, $\overline{BHE}$		Retains status just prior to stop mode	Cannot be used as bus control pin
$\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{WRH}$		High	
$\overline{HLDA}$, BCLK		High	
ALE		Undefined	
I/O ports		Retains status just prior to stop mode	Retains status just prior to stop mode
CLKOUT	fC selected	Cannot be used as CLKOUT pin	High
	f1, f8, f32 selected		Retains status just prior to stop mode
XOUT		High	
XCIN, XCOUT		High-impedance	

9.3.4.3 Exiting Stop Mode

Use a reset or an interrupt to exit stop mode. Table 9.9 lists Resets and Interrupts to Exit Stop Mode and Conditions for Use.

Table 9.9 Resets and Interrupts to Exit Stop Mode and Conditions for Use

Interrupt, Reset			Conditions for Use
Interrupt	Peripheral function interrupt	$\overline{\text{INT}}$	Usable
		Key input	Usable
		timer A, timer B	Usable when counting external signals in event counter mode
		Serial interface	Usable when an external clock is selected
		Multi-master I^2C-bus interface	SCL/SDA is usable
	Voltage detection 1 interrupt,		Usable when the digital filter is disabled (VW1C1 bit in the VW1C register is 1)
	Voltage detection 2 interrupt		Usable when the digital filter is disabled (VW2C1 bit in the VW2C register is 1)
	$\overline{\text{NMI}}$		Usable when the digital filter is disabled (bits NMIDF2 to NMIDF0 in the NMIDF register are 000b)
Reset	Hardware reset		Usable
	Voltage detection 0 reset		Usable when the digital filter is disabled (VW0C1 bit in the VW0C register is 1)

To exit stop mode by using hardware reset, voltage monitor 0 reset, $\overline{\text{NMI}}$ interrupt, voltage monitor 1 interrupt, or voltage monitor 2 interrupt, set bits ILVL2 to ILVL0 in the interrupt control registers for the peripheral function interrupt to 000b (interrupt disabled) before setting the CM10 bit to 1.

To use a peripheral function interrupt to exit stop mode, set the CM10 bit to 1 after the following settings are completed.

(1) Set the interrupt priority level of bits ILVL2 to ILVL0 in the interrupt control register for peripheral function interrupts which are used to exit stop mode.
Set bits ILVL2 to ILVL0 in all other interrupt control registers, for peripheral function interrupts not used to exit stop mode, to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Start operating the peripheral functions used to exit stop mode.

When exiting stop mode by means of a peripheral function interrupt, an interrupt routine is performed after an interrupt request is generated and then the CPU clock is supplied again.
When stop mode is exited by means of an interrupt, the CPU clock source varies depending on the CPU clock source setting before the MCU had entered stop mode. Table 9.10 lists CPU Clock After Exiting Stop Mode.

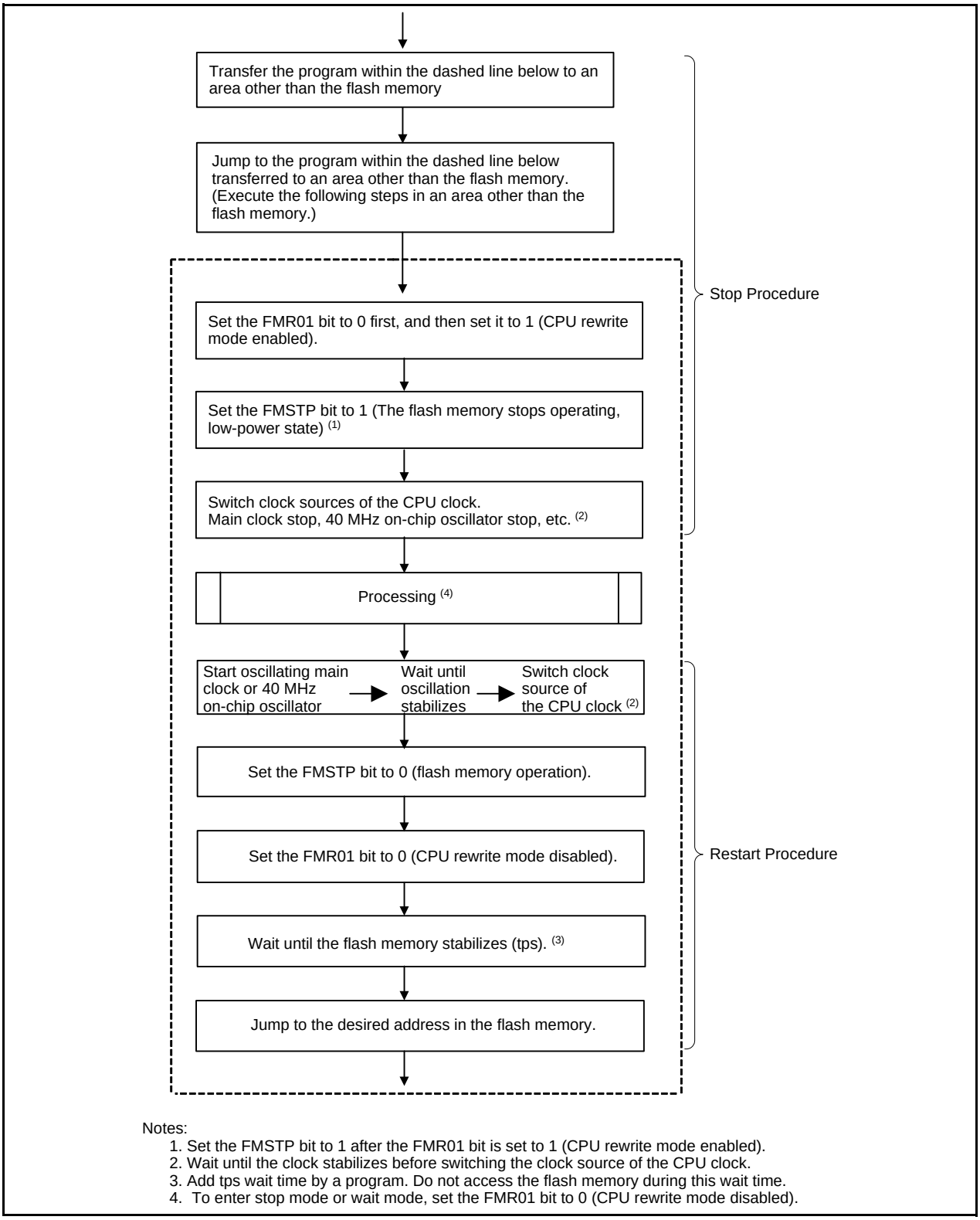
Table 9.10 CPU Clock After Exiting Stop Mode

CPU Clock Before Entering Stop Mode	CPU Clock After Exiting Stop Mode
Main clock divided by 1 (no division), 2, 4, 8 or 16	Main clock divided by 8
fOCO-S divided by 1 (no division), 2, 4, 8 or 16	fOCO-S divided by 8
fOCO-F divided by 1 (no division), 2, 4, 8 or 16	fOCO-F divided by 8
fC	fC

9.4 Power Control in Flash Memory

9.4.1 Stopping Flash Memory

When the flash memory is stopped, consumption current is reduced. Execute a program in any area other than the flash memory. Figure 9.2 shows Stop and Restart of the Flash Memory. Follow the flowchart of Figure 9.2.



Notes:
1. Set the FMSTP bit to 1 after the FMR01 bit is set to 1 (CPU rewrite mode enabled).
2. Wait until the clock stabilizes before switching the clock source of the CPU clock.
3. Add tps wait time by a program. Do not access the flash memory during this wait time.
4. To enter stop mode or wait mode, set the FMR01 bit to 0 (CPU rewrite mode disabled).

Figure 9.2 Stop and Restart of the Flash Memory

9.4.2 Reading Flash Memory

Consumption current while reading the flash memory can be reduced by using bits FMR22 and FMR23.

9.4.2.1 Slow Read Mode

Slow read mode can be used when f(BCLK) is 5 MHz or below. Figure 9.3 shows Setting and Canceling of Slow Read Mode.

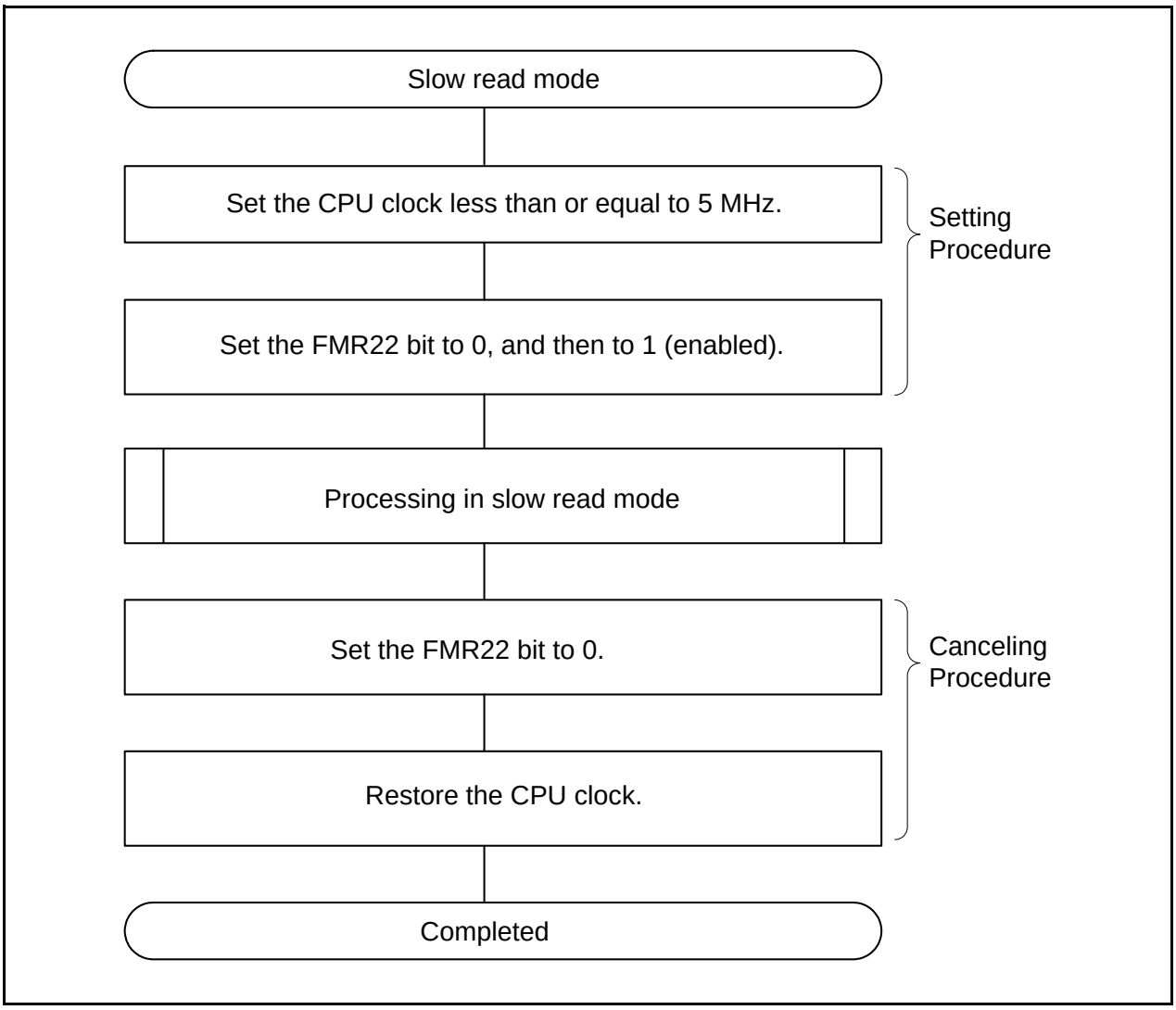
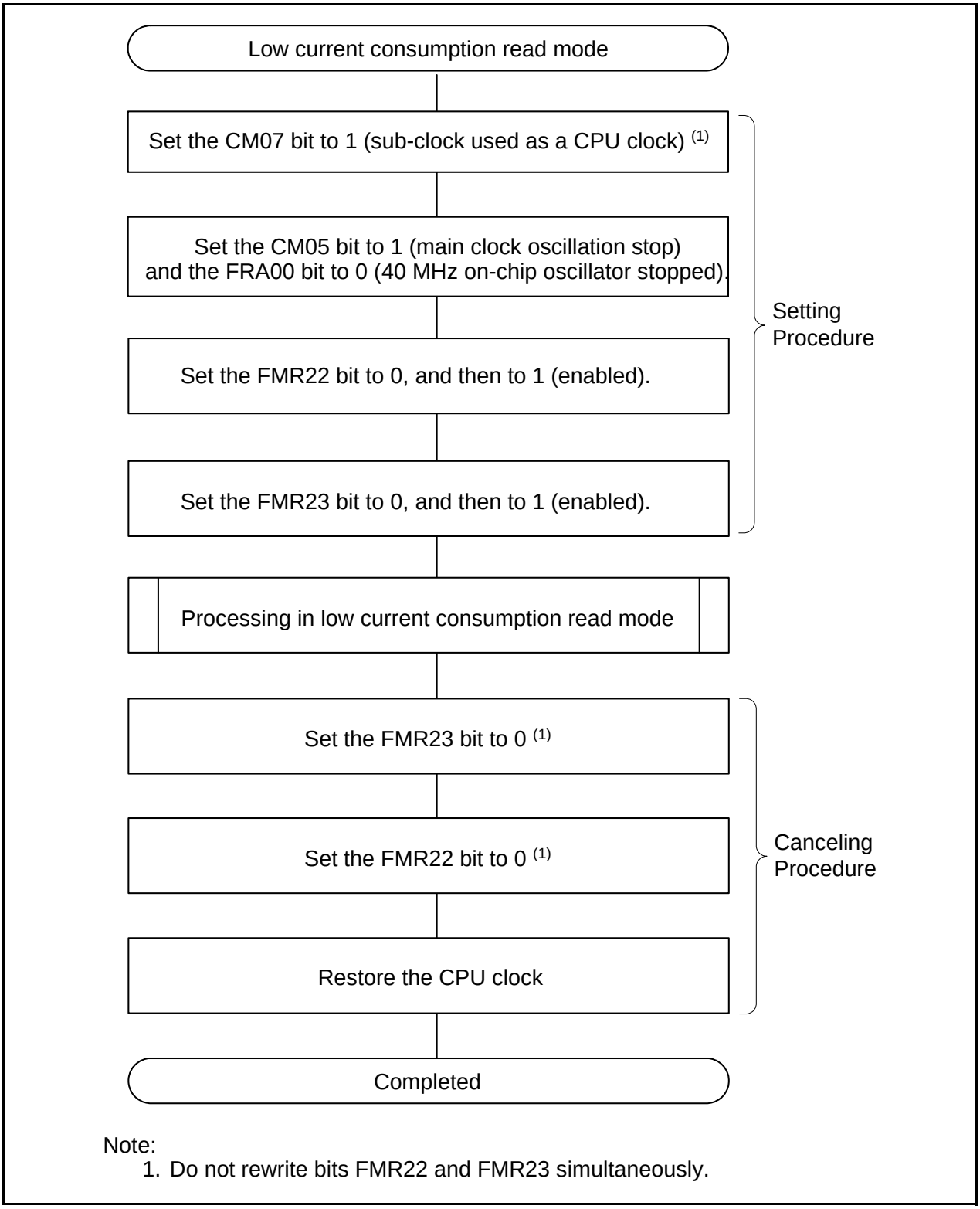


Figure 9.3 Setting and Canceling of Slow Read Mode

9.4.2.2 Low Current Consumption Read Mode

Low current consumption read mode can be used when the CM07 bit in the CM0 register is 1 (sub clock used as CPU clock). Figure 9.4 shows Setting and Canceling of Low Current Consumption Read Mode.



Note:
1. Do not rewrite bits FMR22 and FMR23 simultaneously.

Figure 9.4 Setting and Canceling of Low Current Consumption Read Mode

9.5 Reducing Power Consumption

To reduce power consumption, refer to the following descriptions when designing a system or writing a program.

9.5.1 Ports

The MCU retains the state of each I/O port even when it enters wait mode or stop mode. A current flows in the active output ports. A shoot-through current flows to the input ports in the high-impedance state. When entering wait mode or stop mode, set unused ports to input and stabilize the potential.

9.5.2 A/D Converter

When not executing A/D conversion, set the ADSTBY bit in the ADCON1 register to 0 (A/D operation stop). When executing A/D conversion, start the A/D conversion after setting the ADSTBY bit to 1 (A/D operation enabled) and waiting 1 ϕAD cycle or more.

9.5.3 D/A Converter

When not executing D/A conversion, set the DAiE bit (i = 0, 1) in the DACON register to 0 (output inhibited) and the DAi register to 00h.

9.5.4 Stopping Peripheral Functions

Use the CM02 bit in the CM0 register to stop the unnecessary peripheral functions while in wait mode.

9.5.5 Switching the Oscillation-Driving Capacity

Set the driving capacity to low when oscillation is stable.

9.6 Notes on Power Control

9.6.1 CPU Clock

- When switching clock sources of the CPU clock, wait until the clock oscillation switched to is stabilized.

9.6.2 Wait Mode

- After the WAIT instruction, insert at least four NOP instructions. When entering wait mode, the instruction queue reads ahead the instructions following WAIT. Thus, depending on timing, some of the instructions may be executed before the MCU enters wait mode.

  Program example when entering wait mode is shown below.

```
Program Example:  FSET  I   ;
                  WAIT      ; Enter wait mode
                  NOP       ; More than four NOP instructions
                  NOP
                  NOP
                  NOP
```

- Do not enter wait mode when the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled). Set the FMR23 bit to 0 (low current consumption read mode disabled) and the FMR01 bit to 0 (CPU rewrite mode disabled), and disable DMA transfer before entering wait mode.

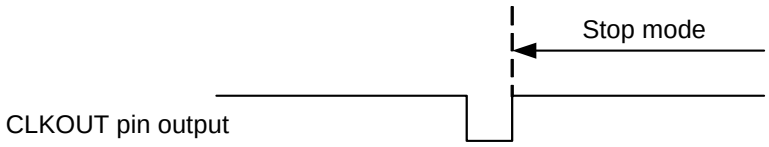
9.6.3 Stop Mode

- When exiting stop mode by hardware reset, drive the $\overline{\text{RESET}}$ pin low until main clock oscillation is stabilized.
- Set the MR0 bit in the TAiMR register (i = 0 to 4) to 0 (pulse not output) when using timer A to exit stop mode.
- When entering stop mode, insert a JMP.B instruction immediately after executing an instruction that sets the CM10 bit in the CM1 register to 1, and then insert at least four NOP instructions. When entering stop mode, the instruction queue reads ahead the instructions following the instruction which sets the CM10 bit to 1 (all clock stop). Thus, some of the instructions may be executed before the MCU enters stop mode or before the interrupt routine for returning from stop mode.

Program example when entering stop mode

```
Program Example:  FSET   I
                  BSET   0, CM1   ; Enter stop mode
                  JMP.B  L2       ; Insert a JMP.B instruction
            L2:
                  NOP             ; At least four NOP instructions
                  NOP
                  NOP
                  NOP
```

- The CLKOUT pin outputs a high-level signal in stop mode. Thus, if stop mode is entered right after output on the CLKOUT pin changes state from high to low, the high-level durations of the output signal to the CLKOUT pin becomes shorter.



- When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not enter stop mode. To enter stop mode, execute an instruction to set the CM10 bit in the CM1 register to 1 (stop mode) after setting the FMR23 bit to 0 (low current consumption read mode disabled), setting the FMR01 bit to 0 (CPU rewrite mode disabled), and disabling DMA transfer.

9.6.4 Low Current Consumption Read Mode

- Enter low current consumption read mode through slow read mode (refer to Figure 9.4 “Setting and Canceling of Low Current Consumption Read Mode”).
- When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not set the FMSTP bit to 1 (flash memory stopped). Also, when the FMSTP bit is 1, do not set the FMR23 bit to 1.

10. Processor Mode

Note

Do not use memory expansion mode and microprocessor mode in the 80-pin package.

10.1 Introduction

Three processor modes are available to choose from: single-chip mode, memory expansion mode, and microprocessor mode. Table 10.1 shows the Features of Processor Modes.

Table 10.1 Features of Processor Modes

Processor Mode	Access Space	Pins Assigned as I/O Ports
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins
Memory expansion mode	SFR, internal RAM, internal ROM, external area (1)	Some pins serve as bus control pins (1)
Microprocessor mode	SFR, internal RAM, external area (1)	Some pins serve as bus control pins (1)

Note:
1. Refer to 11. “Bus” for details.

Table 10.2 I/O Pins

Pin Name	I/O Type	Function
CNVSS	Input	Selects a processor mode

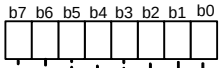
10.2 Registers

Table 10.3 Register Structure

Address	Register Name	Symbol	After Reset
0004h	Processor Mode Register 0	PM0	0000 0000b (CNVSS pin is low) 0000 0011b (CNVSS pin is high)
0005h	Processor Mode Register 1	PM1	0000 1000b
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b

10.2.1 Processor Mode Register 0 (PM0)

Processor Mode Register 0



Symbol	Address	After Reset
PM0	0004h	0000 0000b (CNVSS pin is held low) 0000 0011b (CNVSS pin is held high)

Bit Symbol	Bit Name	Function	RW
PM00	Processor mode bit	b1 b0 0 0 : Single-chip mode 0 1 : Memory expansion mode 1 0 : Do not set 1 1 : Microprocessor mode	RW
PM01			RW
PM02	R/W mode select bit	0 : $\overline{RD}$, $\overline{BHE}$, $\overline{WR}$ 1 : $\overline{RD}$, $\overline{WRH}$, $\overline{WRL}$	RW
PM03	Software reset bit	Setting this bit to 1 resets the MCU. Read as 0.	RW
PM04	Multiplexed bus space select bit	b5 b4 0 0 : Multiplexed bus is unused (separate bus in the entire $\overline{CS}$ space) 0 1 : Allocated to $\overline{CS2}$ space 1 0 : Allocated to $\overline{CS1}$ space 1 1 : Allocated to the entire $\overline{CS}$ space	RW
PM05			RW
PM06	Port P4_0 to P4_3 function select bit	0 : Address output 1 : Port function (address is not output)	RW
PM07	BCLK output disable bit	0 : BCLK is output 1 : BCLK is not output (pin is left in high-impedance)	RW

Rewrite this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
Bits PM01 to PM00 do not change at software reset, watchdog timer reset, oscillation stop detection reset, voltage monitor 1 reset, and voltage monitor 2 reset.

PM01 to PM00 (Processor Mode Bit) (b1 to b0)

Do not rewrite bits PM01 to PM00 and PM07 to PM02 at the same time.

10.2.2 Processor Mode Register 1 (PM1)

Processor Mode Register 1

b7	b6	b5	b4	b3	b2	b1	b0
	0						

Symbol	Address	After Reset
PM1	0005h	0000 1000b

Bit Symbol	Bit Name	Function	RW
PM10	$\overline{CS2}$ area switch bit (data flash enable bit)	0 : $\overline{CS2}$ (0E000h to 0FFFFh) 1 : Data flash (0E000h to 0FFFFh)	RW
PM11	Port P3_7 to P3_4 function select bit	0 : Address output 1 : Port function	RW
PM12	Watchdog timer function select bit	0 : Watchdog timer interrupt 1 : Watchdog timer reset	RW
PM13	Internal area expansion bit 0	Refer to the bit explanation below “PM13 (Internal Area Expansion Bit 0) (b3)”	RW
PM14	Memory area expansion bit	b5 b4 0 0 : 1-Mbyte mode (no expansion) 0 1 : Do not set 1 0 : Do not set 1 1 : 4-Mbyte mode	RW
PM15			RW
— (b6)	Reserved bit	Set to 0	RW
PM17	Wait bit	0 : No wait state 1 : Wait state (1 wait)	RW

Rewrite this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
The PM12 bit is set to 1 by writing 1 by a program (writing 0 has no effect).

PM10 ($\overline{CS2}$ Area Switch Bit (Data Flash Enable Bit)) (b0)

This bit is used to select the function of addresses 0E000h to 0FFFFh. Table 10.4 lists Data Flash (Addresses 0E000h to 0FFFFh).

Table 10.4 Data Flash (Addresses 0E000h to 0FFFFh)

PM10 bit in PM1 Register		0	1
Processor Mode	Single-chip mode	Reserved area	Data flash
	Memory expansion mode	External area	Data flash
	Microprocessor mode	External area	Reserved area

Data flash includes block A (addresses 0E000h to 0EFFFh) and block B (addresses 0F000h to 0FFFFh). When data flash is selected by the setting of the PM10 bit, both block A and block B can be used.
The PM10 bit is automatically set to 1 while the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode).

PM13 (Internal Area Expansion Bit 0) (b3)

This bit is used to select the range of the RAM, program ROM 1, and external area.
When the PM13 bit is 0, the size of the RAM and program ROM 1 is limited, but a wide range can be selected for the external area.
When the PM13 bit is 1, the entire RAM and the program ROM 1 in addresses 80000h to CFFFFh are available. Table 10.5 lists the Functions of Bits PM13 and IRON and Table 10.6 lists Functions of Addresses 80000h to CFFFFh.

Table 10.5 Functions of Bits PM13 and IRON

Access Area			Bit Setting		
			PM13 = 0	PM13 = 1	
			IRON = 0 (1)	IRON = 0	IRON = 1
Internal	RAM		Addresses 00400h up to 03FFFh (15 Kbytes) are available (addresses 0400h to 0CFFFh cannot be used).	The entire area is usable.	The entire area is usable.
	Program ROM 1		Addresses D0000h up to FFFFFh (192 Kbytes) are available (addresses 40000h to CFFFFh cannot be used).	Addresses 80000h up to FFFFFh are available (addresses 40000h to 7FFFFh cannot be used).	The entire area is usable.
External	Memory expansion mode	04000h to 0CFFFh	Usable	Reserved	Reserved
		40000h to 7FFFFh	Usable	Usable	Reserved
		80000 to CFFFFh	Usable	Reserved	Reserved
	Micro-processor mode	04000h to 0CFFFh	Usable	Reserved	Reserved
		40000h to 7FFFFh	Usable	Usable	Usable
		80000 to CFFFFh	Usable	Usable	Usable

PM13: Bit in the PM1 register
IRON: Bit in the PRG2C register
Note:
1. When the PM13 bit is 0, set the IRON bit to 0.

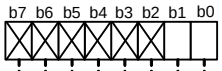
Table 10.6 Functions of Addresses 80000h to CFFFFh

PM13 Bit in PM1 Register		0	1
Processor Mode	Single-chip mode	Reserved area	Program ROM 1 (when program ROM 1 exists) if not, reserved area
	Memory expansion mode	External area	
	Microprocessor mode	External area	External area

The PM13 bit is automatically set to 1 while the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode).

10.2.3 Program 2 Area Control Register (PRG2C)

Program 2 Area Control Register



Symbol	Address	After Reset
PRG2C	0010h	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
PRG2C0	Program ROM 2 disable bit	0 : Enable program ROM 2 1 : Disable program ROM 2	RW
IRON	Internal area expansion bit 1	Program ROM 1 addresses (40000h to 7FFFFh) 0 : Disabled 1 : Enabled	RW
— (b7-b2)	No register bits. If necessary, set to 0. Read as undefined value		—

Rewrite this register after setting the PRC6 bit in the PRCR register to 1 (write enabled).

PRG2C0 (Program ROM 2 Disable Bit) (b0)

This bit is used to select the function of addresses 10000h to 13FFFh. Table 10.7 lists Program ROM 2 (Addresses 10000h to 13FFFh).

Table 10.7 Program ROM 2 (Addresses 10000h to 13FFFh)

PRG2C0 bit in PRG2C Register		0	1
Processor Mode	Single-chip mode	Program ROM 2	Reserved area
	Memory expansion mode	Program ROM 2	External area
	Microprocessor mode	Reserved area	External area

Program ROM 2 includes the on-chip debugger monitor area and user boot code area (refer to 30.7 “User Boot Function”).

IRON (Internal Area Expansion Bit 1) (b1)

This bit enables the program ROM 1 (addresses 40000h to 7FFFFh) for products with the size of program ROM 1 over 512 Kbytes. Table 10.8 lists Functions of Addresses 40000h to 7FFFFh. Table 10.5 lists Functions of Bits PM13 and IRON.

Set the IRON bit to 0 when either of the following is true.

- The PM13 bit in the PM1 register is 0 (maximum of 192 Kbytes are available in program ROM 1).
- Bits PM15 and PM14 in the PM1 register are set to “11b” (4-Mbyte mode).

Table 10.8 Functions of Addresses 40000h to 7FFFFh

IRON Bit in PRG2C Register		0	1
Processor Mode	Single-chip mode	Reserved area	Program ROM 1(when program ROM 1 exists) if not, reserved area
	Memory expansion mode	External area	
	Microprocessor mode	External area	External area

10.3 Operations

10.3.1 Processor Mode Settings

Processor mode is set by using the CNVSS pin and bits PM01 to PM00 in the PM0 register.
In hardware reset, power-on reset, or voltage monitor 0 reset, the processor mode is selected by the CNVSS pin input level. Table 10.9 lists Processor Mode after Hardware Reset, Power-On Reset, or Voltage Monitor 0 Reset.

Table 10.9 Processor Mode after Hardware Reset, Power-On Reset, or Voltage Monitor 0 Reset

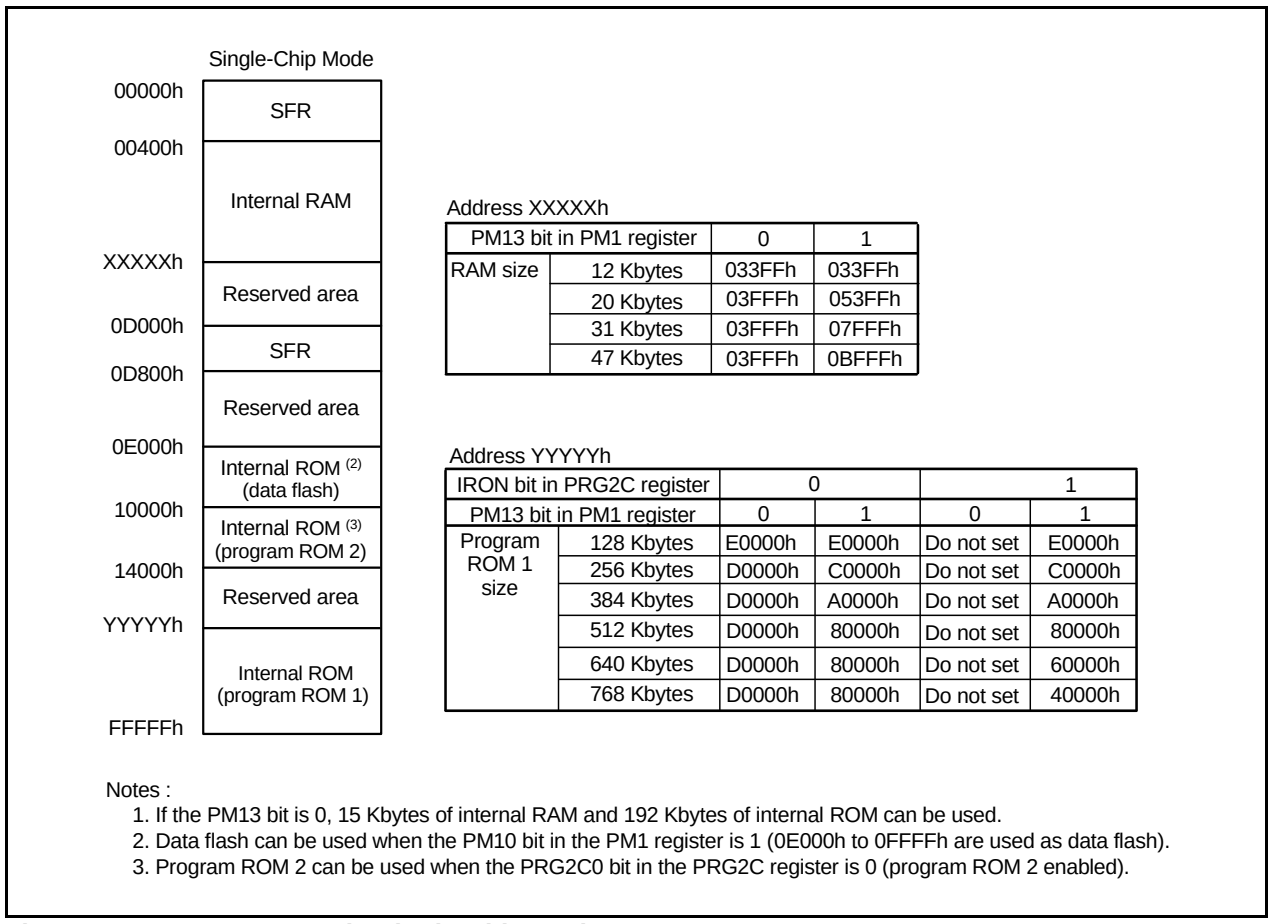
CNVSS Pin Input Level	Processor Mode	Bits PM01 to PM00 in the PM0 Register
VSS	Single-chip mode	00b (single-chip mode)
VCC1	Microprocessor mode	11b (microprocessor mode)

Rewriting bits PM01 to PM00 places the MCU in the mode corresponding to bits PM01 to PM00 regardless of whether the input level of the CNVSS pin is high or low. When VCC1 is applied to the CNVSS pin and then the MCU is reset by hardware reset, power-on reset, or voltage monitor 0 reset, the internal ROM cannot be accessed regardless of the value of bits PM01 to PM00. Table 10.10 lists Bits PM01 to PM00 Set Values and Processor Modes.
Do not rewrite these bits to enter microprocessor mode in the internal ROM, or to exit microprocessor mode in areas overlapping the internal ROM.

Table 10.10 Bits PM01 to PM00 Set Values and Processor Modes

Bits PM01 to PM00	Processor Mode
00b	Single-chip mode
01b	Memory expansion mode
10b	Do not set
11b	Microprocessor mode

Figure 10.1 shows Memory Map in Single-Chip Mode.



Address XXXXXh

PM13 bit in PM1 register		0	1
RAM size	12 Kbytes	033FFh	033FFh
	20 Kbytes	03FFFh	053FFh
	31 Kbytes	03FFFh	07FFFh
	47 Kbytes	03FFFh	0BFFFh

Address YYYYYh

IRON bit in PRG2C register		0		1	
PM13 bit in PM1 register		0	1	0	1
Program ROM 1 size	128 Kbytes	E0000h	E0000h	Do not set	E0000h
	256 Kbytes	D0000h	C0000h	Do not set	C0000h
	384 Kbytes	D0000h	A0000h	Do not set	A0000h
	512 Kbytes	D0000h	80000h	Do not set	80000h
	640 Kbytes	D0000h	80000h	Do not set	60000h
	768 Kbytes	D0000h	80000h	Do not set	40000h

Notes :
1. If the PM13 bit is 0, 15 Kbytes of internal RAM and 192 Kbytes of internal ROM can be used.
2. Data flash can be used when the PM10 bit in the PM1 register is 1 (0E000h to 0FFFFh are used as data flash).
3. Program ROM 2 can be used when the PRG2C0 bit in the PRG2C register is 0 (program ROM 2 enabled).

Figure 10.1 Memory Map in Single-Chip Mode

11. Bus

Note

Do not use bus control pins for the 80-pin package.

11.1 Introduction

Two types of buses are available:

- Internal bus in the MCU
- External bus which is used to access to external devices in memory expansion mode or microprocessor mode

Table 11.1 Bus Specifications

Item	Specification
Internal bus	• Used in all processor modes • Separate bus • 16-bit data bus width • 0 to 2 software waits can be inserted
External bus	• Used in memory expansion mode or microprocessor mode • Separate bus or multiplexed bus selectable • Data bus width selectable (8 or 16 bits) • Number of address buses selectable (12, 16, or 20 buses) • 4 chip select outputs $\overline{CS0}$ to $\overline{CS3}$ • Combinations of read and write signals selectable ($\overline{RD}$, $\overline{BHE}$, $\overline{WR}$ or $\overline{RD}$, $\overline{WRL}$, $\overline{WRH}$) • $\overline{RDY}$ available • $\overline{HOLD}$, $\overline{HDLA}$ available • 0 to 8 software waits can be inserted • Memory area expansion function (up to 4 Mbytes) (Refer to 12. “Memory Space Expansion Function”) • 3 V or 5 V interface

11.2 Registers

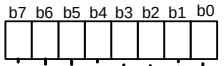
Table 11.2 lists bus related registers. Refer to 10. “Processor Mode” for registers PM1 and PM2. Refer to 30. “Flash Memory” for the FMR1 register.

Table 11.2 Register Structure

Address	Register Name	Register Symbol	After Reset
0005h	Processor Mode Register 1	PM1	0000 1000b
0008h	Chip Select Control Register	CSR	01h
0009h	External Area Recovery Cycle Control Register	EWR	XXXX XX00b
0011h	External Area Wait Control Expansion Register	EWC	00h
001Bh	Chip Select Expansion Control Register	CSE	00h
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb

11.2.1 Chip Select Control Register (CSR)

Chip Select Control Register



Symbol	Address	After Reset
CSR	0008h	01h

Bit Symbol	Bit Name	Function	RW
CS0	$\overline{CS0}$ output enable bit	0 : Chip select output disabled (functions as I/O port) 1 : Chip select output enabled	RW
CS1	$\overline{CS1}$ output enable bit		RW
CS2	$\overline{CS2}$ output enable bit		RW
CS3	$\overline{CS3}$ output enable bit		RW
CS0W	$\overline{CS0}$ wait bit	0 : Wait state 1 : No wait state	RW
CS1W	$\overline{CS1}$ wait bit		RW
CS2W	$\overline{CS2}$ wait bit		RW
CS3W	$\overline{CS3}$ wait bit		RW

CSiW ($\overline{CSi}$ Wait Bit) (b7-b4) (i = 0 to 3)

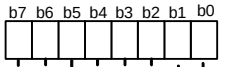
Set the CSiW bit to 0 (wait state) under the following conditions:

- The $\overline{RDY}$ signal is used in the area indicated by $\overline{CSi}$.
- Multiplexed bus is used in the area indicated by $\overline{CSi}$.
- The PM17 bit in the PM1 register is 1 (wait state).

When the CSiW bit is 0 (wait state), the number of wait states can be selected using bits CSEi1W to CSEi0W in the CSE register.

11.2.2 Chip Select Expansion Control Register (CSE)

Chip Select Expansion Control Register



Symbol	Address	After Reset
CSE	001Bh	00h

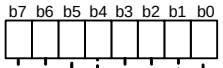
Bit Symbol	Bit Name	Function	RW
CSE00W	$\overline{CS0}$ wait expansion bit	b1 b0 0 0 : 1 wait (1ϕ + 1ϕ) 0 1 : 2 waits (1ϕ + 2ϕ) 1 0 : 3 waits (1ϕ + 3ϕ) 1 1 : Select wait states by bits EWC01 and EWC00 in the EWC register	RW
CSE01W			RW
CSE10W	$\overline{CS1}$ wait expansion bit	b3 b2 0 0 : 1 wait (1ϕ + 1ϕ) 0 1 : 2 waits (1ϕ + 2ϕ) 1 0 : 3 waits (1ϕ + 3ϕ) 1 1 : Select wait states by bits EWC11 and EWC10 in the EWC register	RW
CSE11W			RW
CSE20W	$\overline{CS2}$ wait expansion bit	b5 b4 0 0 : 1 wait (1ϕ + 1ϕ) 0 1 : 2 waits (1ϕ + 2ϕ) 1 0 : 3 waits (1ϕ + 3ϕ) 1 1 : Select wait states by bits EWC21 and EWC20 in the EWC register	RW
CSE21W			RW
CSE30W	$\overline{CS3}$ wait expansion bit	b7 b6 0 0 : 1 wait (1ϕ + 1ϕ) 0 1 : 2 waits (1ϕ + 2ϕ) 1 0 : 3 waits (1ϕ + 3ϕ) 1 1 : Select wait states by bits EWC31 and EWC30 in the EWC register	RW
CSE31W			RW

Set the CSiW bit (i = 0 to 3) in the CSR register to 0 (wait state) before writing to bits CSEi1W to CSEi0W. To set the CSiW bit to 1 (no wait state), set bits CSEi1W to CSEi0W to 00b first, and then set the CSiW bit to 1.

Do not set bits CSEi1W and CSEi0W to 11b for a multiplexed bus area.

11.2.3 External Area Wait Control Expansion Register (EWC)

External Area Wait Control Extension Register



Symbol	Address	After Reset
EWC	0011h	00h

Bit Symbol	Bit Name	Function	RW
EWC00	$\overline{CS0}$ area wait extention bit	b1 b0 0 0 : 2 ϕ + 3 ϕ 0 1 : 2 ϕ + 4 ϕ 1 0 : 3 ϕ + 4 ϕ 1 1 : 4 ϕ + 5 ϕ	RW
EWC01			RW
EWC10	$\overline{CS1}$ area wait extention bit	b3 b2 0 0 : 2 ϕ + 3 ϕ 0 1 : 2 ϕ + 4 ϕ 1 0 : 3 ϕ + 4 ϕ 1 1 : 4 ϕ + 5 ϕ	RW
EWC11			RW
EWC20	$\overline{CS2}$ area wait extention bit	b5 b4 0 0 : 2 ϕ + 3 ϕ 0 1 : 2 ϕ + 4 ϕ 1 0 : 3 ϕ + 4 ϕ 1 1 : 4 ϕ + 5 ϕ	RW
EWC21			RW
EWC30	$\overline{CS3}$ area wait extention bit	b7 b6 0 0 : 2 ϕ + 3 ϕ 0 1 : 2 ϕ + 4 ϕ 1 0 : 3 ϕ + 4 ϕ 1 1 : 4 ϕ + 5 ϕ	RW
EWC31			RW

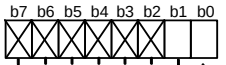
This register can be used as a separate bus area. When bits CSEi1W and CSEi0W in the CSE register are 11b (select wait states by bits EWCi1 to EWCi0), bits EWCi1 to EWCi0 are enabled. (i = 0 to 3)
The number of cycles is as follows.

Example: 2ϕ + 3ϕ

The number of cycles between the falling edge and the rising edge of the $\overline{RD}$ or $\overline{WR}$ signal
The number of cycles between bus access start and the falling edge of the $\overline{RD}$ or $\overline{WR}$ signal

11.2.4 External Area Recovery Cycle Control Register (EWR)

External Area Recovery Cycle Control Register



Symbol	Address	After Reset
EWR	0009h	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
EWR0	Recovery cycle insert bit	b1 b0 0 0 : No recovery cycle 0 1 : 1 recovery cycle inserted 1 0 : 2 recovery cycles inserted 1 1 : 3 recovery cycles inserted	RW
EWR1			RW
— (b7-b2)	No register bits. If necessary, set to 0. Read as undefined value		—

The EWR register is enabled when bits CSEi1W to CSEi0W in the CSE register is 11b.

11.3 Operations

11.3.1 Common Specifications of Internal Bus and External Bus

11.3.1.1 Reference Clock

Both the internal and external buses operate based on the BCLK. However, the area accessed and wait states affect bus operation. Refer to 11.3.2.1 “Software Wait States of the Internal Bus” and 11.3.5.10 “Software Wait States” for details.

11.3.1.2 Bus Hold

Both the internal and external buses are in a hold state under the following conditions:

- Rewriting the flash memory in EW1 mode while auto-programming or auto-erasing
- Inputting a low-level signal to the $\overline{\text{HOLD}}$ pin in memory expansion mode or microprocessor mode

When the bus is in hold state, the following occur:

- CPU is stopped
- DMAC is stopped
- Watchdog timer is stopped when the CSPRO bit in the CSPR register is 0 (count source protection mode disabled)

Bus use priority is given to bus hold, DMAC, and CPU in descending order. However, if the CPU is accessing an odd address in word units, the DMAC cannot gain control of the bus between two separate accesses.

Bus Hold > DMAC > CPU

Figure 11.1 Bus Use Priority

11.3.2 Internal Bus

The internal bus is used to access the internal area in the MCU.

11.3.2.1 Software Wait States of the Internal Bus

The PM17 bit in the PM1 register, which is a software-wait-related bit, affects both the internal memory and the external area. Table 11.3 lists Bits and Bus Cycles Related to Software Wait States (SFR and Internal Memory).

The data flash of the internal ROM is affected by both the PM17 bit in the PM1 register and the FMR17 bit in the FMR1 register.

Table 11.3 Bits and Bus Cycles Related to Software Wait States (SFR and Internal Memory)

Area		Setting of Software-Wait-Related Bits			Software Wait States	Bus cycle
		PM2 Register PM20 Bit (1)	FMR1 Register FMR17 Bit	PM1 Register PM17 Bit		
SFR		1	0 or 1	0 or 1	1	2 BCLK cycles (2)
		0	0 or 1	0 or 1	2	3 BCLK cycles
Internal RAM		0 or 1	0 or 1	0	None	1 BCLK cycle (2)
				1	1	2 BCLK cycles
Internal ROM	Program ROM 1 Program ROM 2	0 or 1	0 or 1	0	None	1 BCLK cycle (2)
				1	1	2 BCLK cycles
	Data flash	0 or 1	0	0 or 1	1	2 BCLK cycles (2)
			1	0	None	1 BCLK cycle
				1	1	2 BCLK cycle

Notes:
1. The PM20 bit is valid when the PLC07 bit in the PLC0 register is set to 1 (PLL operation).
2. Status after reset.

11.3.3 External Bus

The external bus is used to access external devices in memory expansion mode or microprocessor mode.

In memory expansion or microprocessor mode, some pins serve as the bus control pins to perform data input to and output from external devices. The bus control pins are as follows: A0 to A19, D0 to D15, $\overline{CS0}$ to $\overline{CS3}$, $\overline{RD}$, $\overline{WRL}$ /$\overline{WR}$, $\overline{WRH}$ / $\overline{BHE}$, ALE, $\overline{RDY}$, $\overline{HOLD}$, $\overline{HLDA}$, and BCLK.

11.3.4 External Bus Mode

Multiplexed bus mode or separate bus mode can be selected using bits PM05 to PM04 in the PM0 register. Table 11.4 shows the Difference between Separate Bus and Multiplexed Bus Modes.

11.3.4.1 Separate Bus

In external bus mode, data and address are separate.

11.3.4.2 Multiplexed Bus

In external bus mode, data and address are multiplexed.

- When input level to the BYTE pin is high (8-bit data bus)
  D0 to D7 and A0 to A7 are multiplexed.
- When input level to the BYTE pin is low (16-bit data bus)
  D0 to D7 and A1 to A8 are multiplexed. D8 to D15 are not multiplexed (do not use these pins).
  External devices connected to a multiplexed bus are assigned only even addresses of the MCU.

Table 11.4 Difference between Separate Bus and Multiplexed Bus Modes

Pin Name (1)	Separate Bus	Multiplexed Bus	
		BYTE = high	BYTE = low
P0_0 to P0_7/D0 to D7	D0 to D7	(Note 2)	(Note 2)
P1_0 to P1_7/D8 to D15	D8 to D15	I/O port P1_0 to P1_7	(Note 2)
P2_0/A0 (/ D0 / -)	A0	A0 D0	A0
P2_1 to P2_7/A1 to A7 (/ D1 to D7 / D0 to D6)	A1 to A7	A1 to A7 D1 to D7	A1 to A7 D0 to D6
P3_0/A8 (/ - / D7)	A8	A8	A8 D7

Notes:
1. See Table 11.9 “Pin Functions for Each Processor Mode”, for bus control signals other than the above.
2. Depends on the setting of PM05 and PM04, and area being accessed.
   See Table 11.9 “Pin Functions for Each Processor Mode”, for details.

11.3.5 External Bus Control

The following describes the signals needed for accessing external devices and the functionality of software wait states.

11.3.5.1 Address Bus

The address bus consists of 20 lines: A0 to A19. The address bus width can be set to 12, 16, or 20 bits using the PM06 bit in the PM0 register, and the PM11 bit in the PM1 register. Table 11.5 lists the Set Value of Bits PM06 and PM11 and the Corresponding Address Bus Widths.

Table 11.5 Set Value of Bits PM06 and PM11 and the Corresponding Address Bus Widths

Bit Set Value (1)	Pin Function	Address Bus Width
PM11 = 1	P3_4 to P3_7	12 bits
PM06 = 1	P4_0 to P4_3	
PM11 = 0	A12 to A15	16 bits
PM06 = 1	P4_0 to P4_3	
PM11 = 0	A12 to A15	20 bits
PM06 = 0	A16 to A19	

Note:
1. Only the values listed above can be set.

When the processor mode is changed from single-chip mode to memory expansion mode, the address bus is undefined until an external area is accessed.

11.3.5.2 Data Bus

When input to the BYTE pin is high (8-bit width), eight lines (D0 to D7) comprise the data bus. When input to the BYTE pin is low (16-bit width), 16 lines (D0 to D15) comprise the data bus.
Do not change the input level to the BYTE pin.

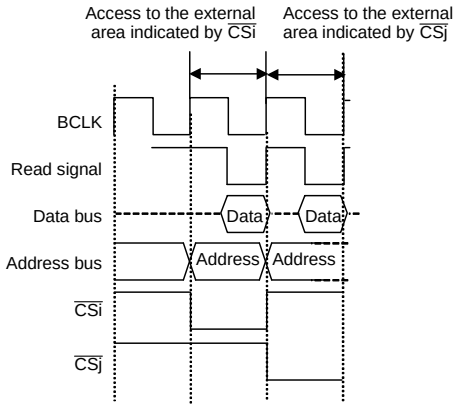
11.3.5.3 Chip Select Signal

The chip select signals (hereafter referred to as $\overline{CS}$) are output from the $\overline{CSi}$ (i = 0 to 3) pin. These pins can be set to function as I/O ports or as $\overline{CS}$ using the $\overline{CSi}$ bit in the CSR register.
In 1-Mbyte mode, the external area can be separated into a maximum of four spaces by the $\overline{CSi}$ signal. In 4-Mbyte mode, a $\overline{CSi}$ signal or bank number is output from the $\overline{CSi}$ pin. Refer to 12. “Memory Space Expansion Function”. Figure 11.2 shows Examples of Address Bus and $\overline{CSi}$ Signal Output in 1-Mbyte Mode.

Example 1

Accessing the external area indicated by $\overline{CSj}$ in the next cycle after accessing the external area indicated by $\overline{CSi}$.

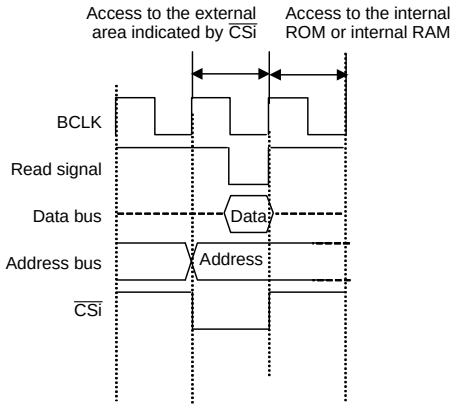
The address bus and chip select signal both change state between these two cycles.



Example 2

Accessing the internal ROM or internal RAM in the next cycle after accessing the external area indicated by $\overline{CSi}$.

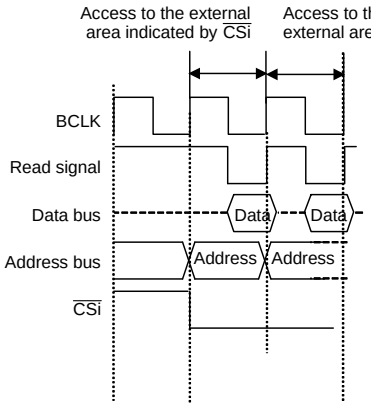
The chip select signal changes state but the address bus does not change state.



Example 3

Accessing the external area indicated by $\overline{CSi}$ in the next cycle after accessing the external area indicated by the same $\overline{CSi}$.

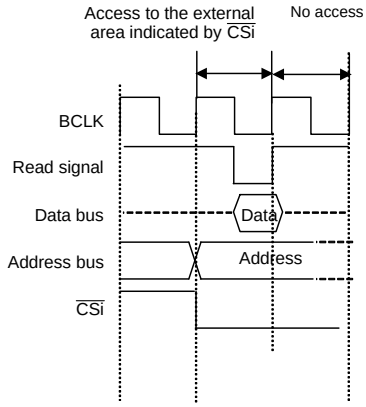
The address bus changes state but the chip select signal does not change state.



Example 4

Not accessing any area (no instruction prefetch generated) in the next cycle after accessing the external area indicated by $\overline{CSi}$.

Neither the address bus nor the chip select signal changes state between these two cycles.



Note:
1. These examples show the address bus and chip select signal when accessing areas in two successive cycles. The chip select bus cycle may be extended to more than two cycles depending on the combination of these examples.

Shown above is the case where separate bus is selected and the area is accessed for read without wait states.
i = 0 to 3, j = 0 to 3 (not including i, however)

Figure 11.2 Examples of Address Bus and $\overline{CSi}$ Signal Output in 1-Mbyte Mode

11.3.5.4 Read and Write Signals

When the data bus is 16 bits wide, the read and write signals can be selected based on combinations of $\overline{RD}$, $\overline{BHE}$, and $\overline{WR}$, or combinations of $\overline{RD}$, $\overline{WRL}$, and $\overline{WRH}$ using the PM02 bit in the PM0 register. When the data bus is 8 bits wide, use combinations of $\overline{RD}$, $\overline{WR}$, and $\overline{BHE}$.
Table 11.6 shows Operation of the $\overline{RD}$, $\overline{WRL}$ and $\overline{WRH}$ Signals. Table 11.7 shows Operation of the $\overline{RD}$, $\overline{WR}$ and $\overline{BHE}$ Signals.

Table 11.6 Operation of the $\overline{RD}$, $\overline{WRL}$ and $\overline{WRH}$ Signals

Data Bus Width	$\overline{RD}$	$\overline{WRL}$	$\overline{WRH}$	Status of External Data Bus
16-bit (BYTE pin input = low)	L	H	H	Read data
	H	L	H	Write 1 byte of data to an even address
	H	H	L	Write 1 byte of data to an odd address
	H	L	L	Write data to both even and odd addresses

Table 11.7 Operation of the $\overline{RD}$, $\overline{WR}$ and $\overline{BHE}$ Signals

Data Bus Width	$\overline{RD}$	$\overline{WR}$	$\overline{BHE}$	A0	Status of External Data Bus
16-bit (BYTE pin input = low)	H	L	L	H	Write 1 byte of data to an odd address.
	L	H	L	H	Read 1 byte of data from an odd address.
	H	L	H	L	Write 1 byte of data to an even address.
	L	H	H	L	Read 1 byte of data from an even address.
	H	L	L	L	Write data to both even and odd addresses.
	L	H	L	L	Read data from both even and odd addresses.
8-bit (BYTE pin input = high)	H	L	– (1)	H or L	Write 1 byte of data.
	L	H	– (1)	H or L	Read 1 byte of data.

Note:
1. Do not use.

11.3.5.5 ALE Signal

The ALE signal is used to latch the address when a multiplexed bus space is accessed. Latch the address at the falling edge of the ALE signal.

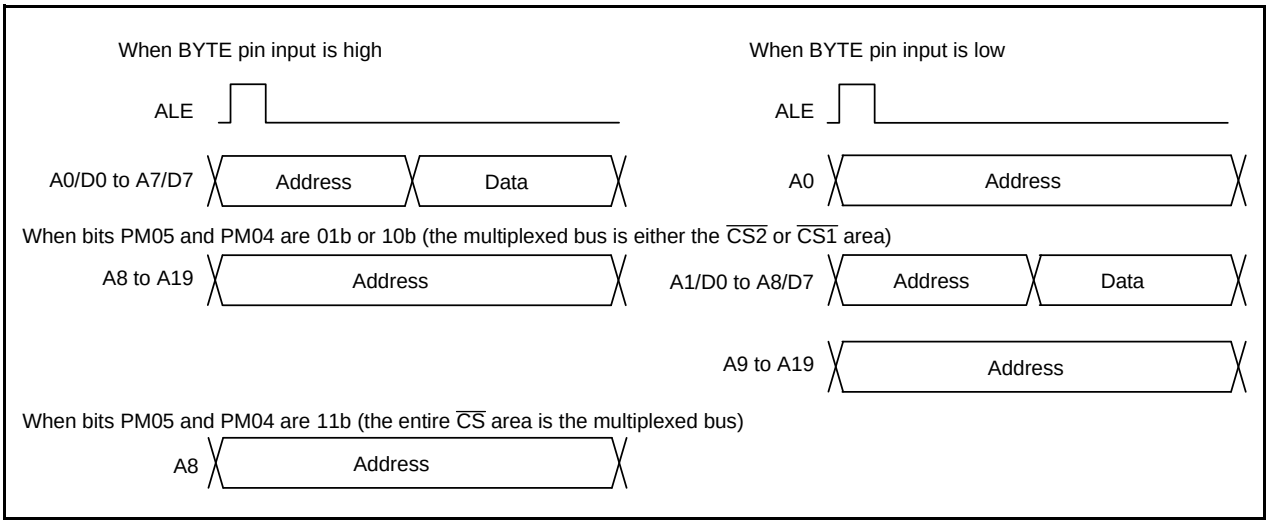
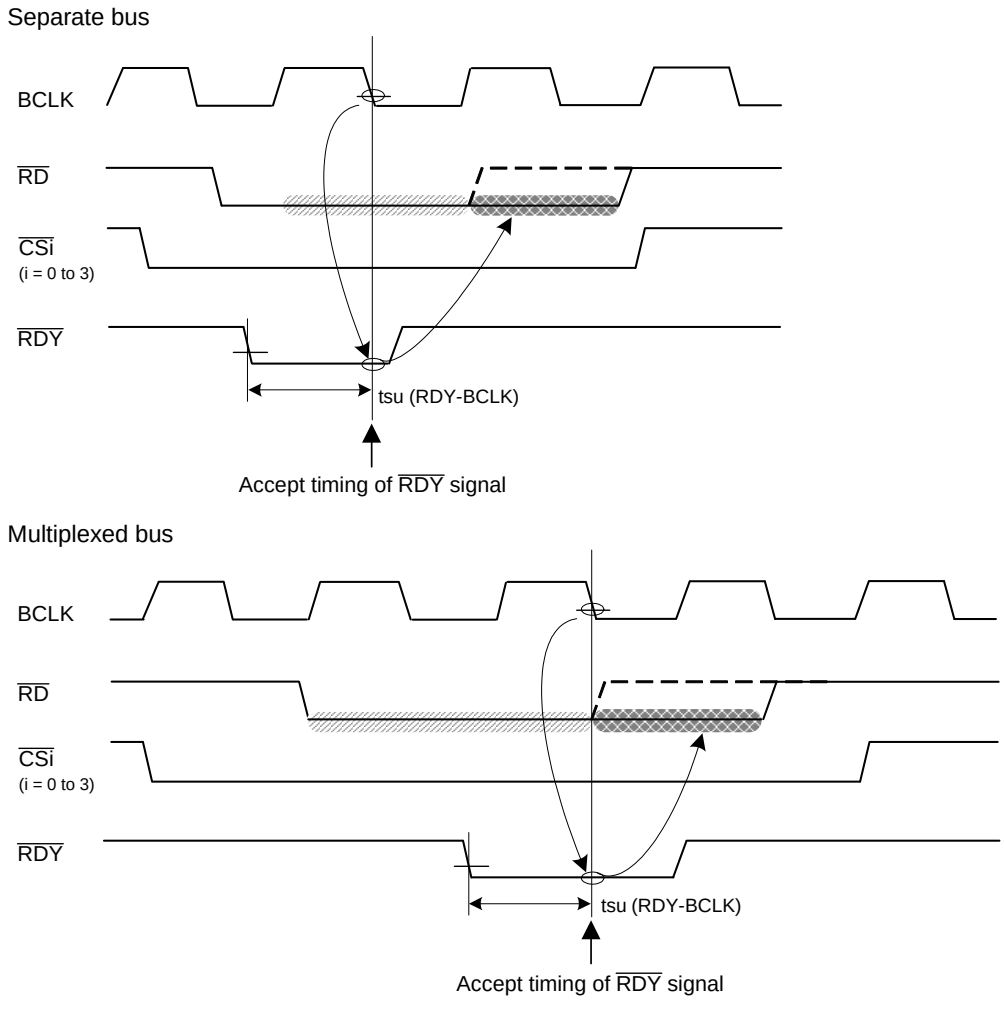


Figure 11.3 ALE Signal, Address Bus, and Data Bus

11.3.5.6 $\overline{\text{RDY}}$ Signal

This signal is provided for accessing external devices which need to be accessed at low speed. If input to the $\overline{\text{RDY}}$ pin is low at the last falling edge of BCLK in the bus cycle, one wait state is inserted in the bus cycle. While in wait state, the following signals retain the state in which they were when the $\overline{\text{RDY}}$ signal was acknowledged:
A0 to A19, D0 to D15, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{RD}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, ALE, $\overline{\text{HLDA}}$

Then, when input to the $\overline{\text{RDY}}$ pin is detected high at the falling edge of BCLK, the remaining bus cycle is executed. Figure 11.4 shows Examples in Which Wait State Was Inserted into Read Cycle by $\overline{\text{RDY}}$ Signal. To use the $\overline{\text{RDY}}$ signal, set the corresponding bit (among bits CS3W to CS0W) in the CSR register to 0 (with wait state). When not using the $\overline{\text{RDY}}$ signal, pull-up the $\overline{\text{RDY}}$ pin.



Shown above is a case where bits CSEi1W to CSEi0W (i = 0 to 3) in the CSE register are 00b (one wait state).

Figure 11.4 Examples in Which Wait State Was Inserted into Read Cycle by $\overline{\text{RDY}}$ Signal

11.3.5.7 $\overline{\text{HOLD}}$ Signal

This signal is used to transfer control of the bus from the CPU or DMAC to an external circuit. When input to the $\overline{\text{HOLD}}$ pin is pulled low, the bus is placed in a hold state after the current bus access is completed. While the $\overline{\text{HOLD}}$ pin is held low, the bus remains in a hold state. When the bus is in a hold state, the $\overline{\text{HLDA}}$ pin outputs a low-level signal.
Table 11.8 shows the Pin Status in Hold State Caused by the $\overline{\text{HOLD}}$ Input.

Table 11.8 Pin Status in Hold State Caused by the $\overline{\text{HOLD}}$ Input

Item		Status
BCLK		Output
A0 to A19, D0 to D15, $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$, $\overline{\text{RD}}$, $\overline{\text{WRL}}$,$\overline{\text{WRH}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$		High-impedance
I/O ports	P0, P1, P3, P4 (1)	High-impedance
	P6 to P14	Maintains status when $\overline{\text{HOLD}}$ signal is received
$\overline{\text{HLDA}}$		Low-level output
ALE		Undefined

Note:
1. When I/O port function is selected.

11.3.5.8 BCLK Output

When the PM07 bit in the PM0 register is set to 0 (output enabled), a clock with the same frequency as the CPU clock is output as BCLK from the BCLK pin. Refer to 8.4 “CPU Clock and Peripheral Function Clocks”.

Table 11.9 Pin Functions for Each Processor Mode

Processor Mode		Memory Expansion Mode or Microprocessor Mode				Memory Expansion Mode
Bits PM05 to PM04		00b (separate bus)		01b ($\overline{CS2}$ is for multiplexed bus and the others are for separate bus) 10b ($\overline{CS1}$ is for multiplexed bus and the others are for separate bus)		11b (the entire space of $\overline{CS}$ is for multiplexed bus) (1), (2), (3)
Data bus width BYTE Pin		8 bits High	16 bits Low	8 bits High	16 bits Low	8 bits High
P0_0 to P0_7		D0 to D7	D0 to D7	D0 to D7 (6)	D0 to D7 (6)	I/O ports
P1_0 to P1_7		I/O ports	D8 to D15	I/O ports	D8 to D15(6)	I/O ports
P2_0		A0	A0	A0/D0 (4)	A0	A0/D0
P2_1 to P2_7		A1 to A7	A1 to A7	A1 to A7 /D1 to D7 (4)	A1 to A7 /D0 to D6 (4)	A1 to A7 /D1 to D7
P3_0		A8	A8	A8	A8/D7 (4)	A8
P3_1 to P3_3		A9 to A11				I/O ports
P3_4 to P3_7	PM11 = 0	A12 to A15				I/O ports
	PM11 = 1	I/O ports				
P4_0 to P4_3	PM06 = 0	A16 to A19				I/O ports
	PM06 = 1	I/O ports				
P4_4	CS0 = 0	I/O ports				
	CS0 = 1	$\overline{CS0}$				
P4_5	CS1 = 0	I/O ports				
	CS1 = 1	$\overline{CS1}$				
P4_6	CS2 = 0	I/O ports				
	CS2 = 1	$\overline{CS2}$				
P4_7	CS3 = 0	I/O ports				
	CS3 = 1	$\overline{CS3}$				
P5_0	PM02 = 0	$\overline{WR}$				
	PM02 = 1	– (5)	$\overline{WRL}$	– (5)	$\overline{WRL}$	– (5)
P5_1	PM02 = 0	$\overline{BHE}$				
	PM02 = 1	– (5)	$\overline{WRH}$	– (5)	$\overline{WRH}$	– (5)
P5_2		$\overline{RD}$				
P5_3		BCLK				
P5_4		$\overline{HLDA}$				
P5_5		$\overline{HOLD}$				
P5_6		ALE				
P5_7		$\overline{RDY}$				

I/O port: Functions as I/O ports or peripheral function I/O pins.

Notes:

1. When bits PM01 to PM00 are 01b (memory expansion mode), and bits PM05 to PM04 are set to 11b (multiplexed bus assigned to the entire $\overline{CS}$ space), apply a high-level signal to the BYTE pin (external data bus 8 bits wide).
2. While the CNVSS pin is driven high (= VCC1), do not set bits PM05 to PM04 to 11b.
3. When bits PM05 to PM04 are set to 11b in memory expansion mode, P3_1 to P3_7 and P4_0 to P4_3 become I/O ports, in which case the accessible area for each CS is 256 bytes.
4. In separate bus mode, these pins serve as the address bus.
5. When the data bus is 8 bits wide, set the PM02 bit to 0 ($\overline{RD}$, $\overline{BHE}$, $\overline{WR}$).
6. When accessing an area using a multiplexed bus, these pins output an undefined value while writing.

11.3.5.9 External Bus Status When Internal Area is Accessed

Table 11.10 lists the External Bus Status When an Internal Area is Accessed. Figure 11.5 shows the Typical Bus Timings When Accessing SFRs.

Table 11.10 External Bus Status When an Internal Area is Accessed

Item		SFR Accessed	Internal ROM or RAM Accessed
A0 to A19		Address output	Maintain the last accessed address of external area or SFR
D0 to D15	Read	High-impedance	High-impedance
	Write	Data output	Undefined
$\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{WRH}$		$\overline{RD}$, $\overline{WR}$, $\overline{WRL}$, $\overline{WRH}$ output	High-level output
$\overline{BHE}$		$\overline{BHE}$ output	Maintain the last accessed status of external area or SFRs
$\overline{CS0}$ to $\overline{CS3}$		High-level output	High-level output
ALE		Low-level output	Low-level output

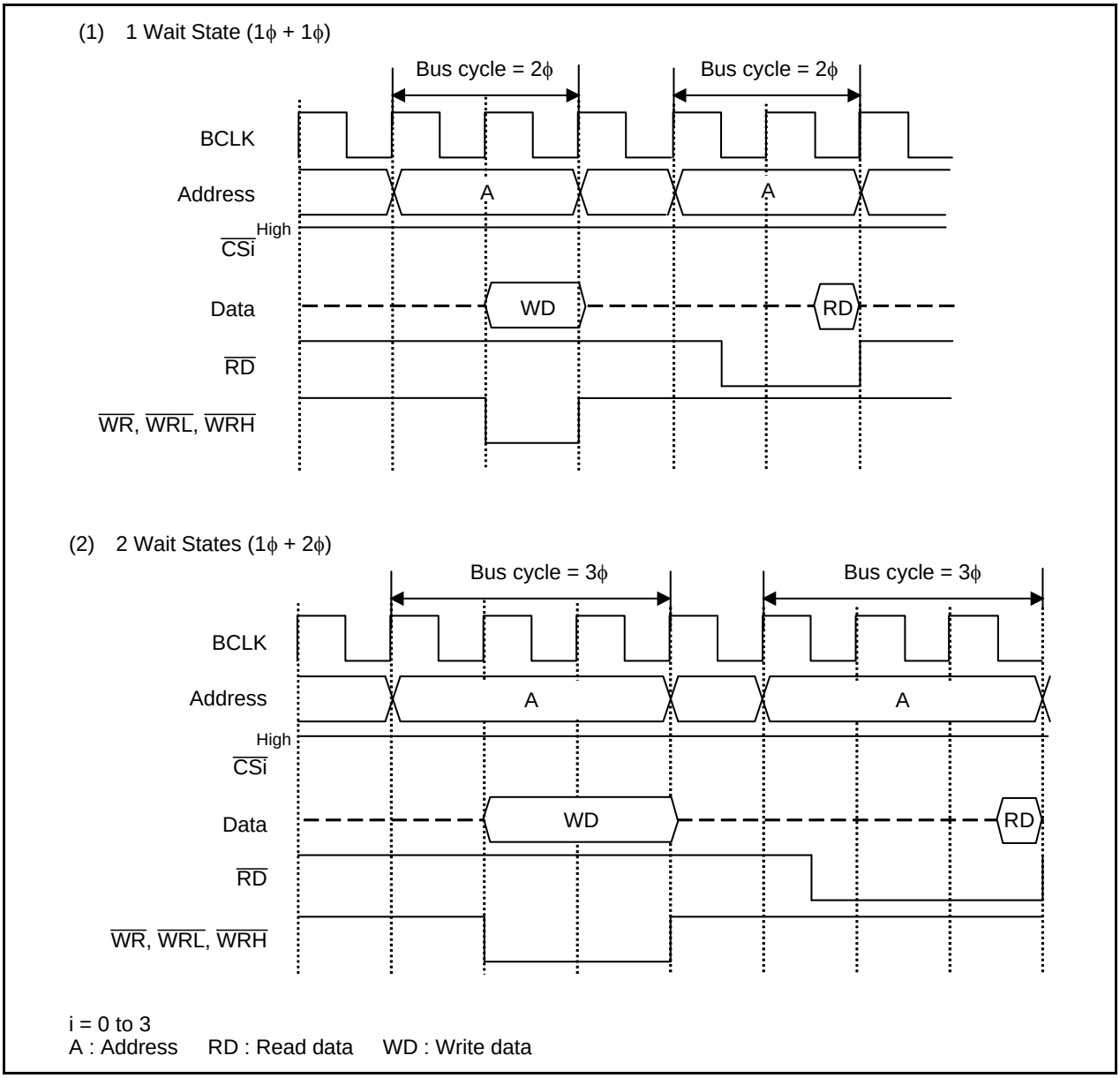


Figure 11.5 Typical Bus Timings When Accessing SFRs

11.3.5.10 Software Wait States

The PM17 bit in the PM1 register, which is a software-wait-related bit, affects both the internal memory and the external area.

Software wait states can be inserted to the external area by setting the PM17 bit or setting the CSiW bit in the CSR register or bits CSEi1W to CSEi0W in the CSE register for each $\overline{CSi}$ (i = 0 to 3). To use the $\overline{RDY}$ signal, set the corresponding CSiW bit to 0 (wait state). Refer to Table 11.11 “Bits and Bus Cycles Related to Software Wait States (External Area)”, for details.

Table 11.11 Bits and Bus Cycles Related to Software Wait States (External Area)

Area	Bus Mode	Setting of Software-Wait-Related Bits				Software Wait Cycles	Bus Cycles
		PM17	CSiW	CSEi1W, CSEi0W	EWCi1, EWCi0		
External area	Separate bus	0	1	00b	-	None	1 BCLK cycle (read)
							2 BCLK cycles (write)
		-	0	00b	-	1 (1ϕ + 1ϕ)	2 BCLK cycles (4)
		-	0	01b	-	2 (1ϕ + 2ϕ)	3 BCLK cycles
		-	0	10b	-	3 (1ϕ + 3ϕ)	4 BCLK cycles
		-	0	11b	00b	(2ϕ + 3ϕ)	5 BCLK cycles
					01b	(2ϕ + 4ϕ)	6 BCLK cycles
					10b	(3ϕ + 4ϕ)	7 BCLK cycles
					11b	(4ϕ + 5ϕ)	9 BCLK cycles
		1	0 (3)	00b	-	1 (1ϕ + 1ϕ)	2 BCLK cycles
	Multiplexed bus	-	0 (2)	00b	-	1	3 BCLK cycles
		-	0 (2)	01b	-	2	3 BCLK cycles
		-	0 (2)	10b	-	3	4 BCLK cycles
		1	0 (2), (3)	00b	-	1	3 BCLK cycles

i = 0 to 3

– indicates that either 0 or 1 can be set.

PM17: Bit in the PM1 register

CSiW: Bits in the CSR register (1)

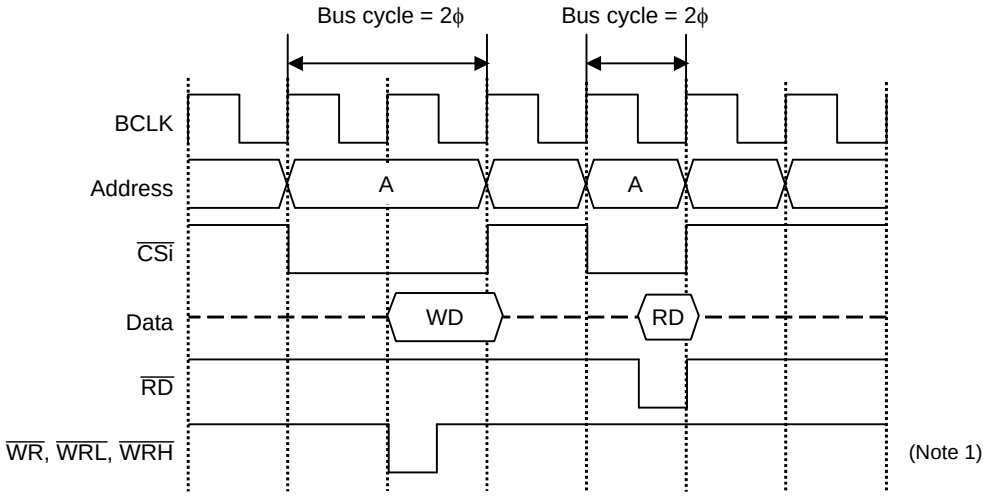
CSEi1W, CSEi0W: Bits in the CSE register

EWCi1, EWCi0: Bits in the EWC register

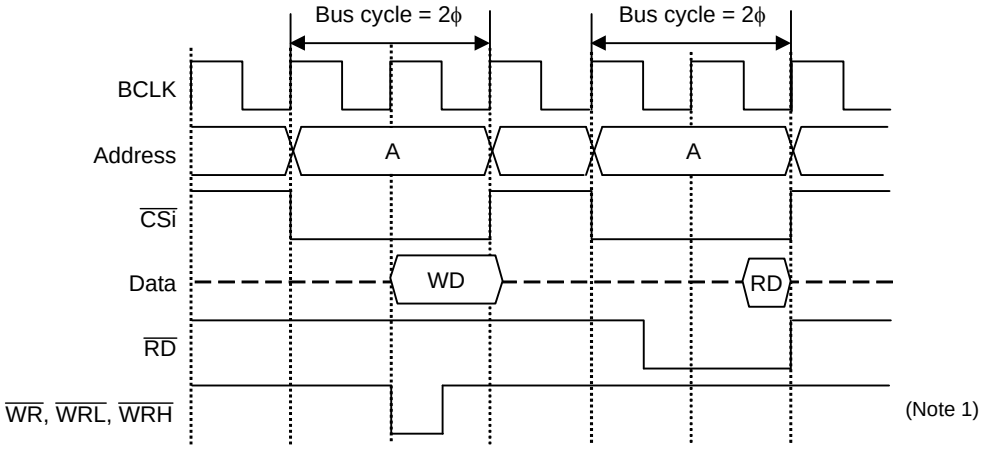
Notes:

1. To use the $\overline{RDY}$ signal, set the CSiW bit to 0 (wait state).
2. To access in multiplexed bus mode, set the CSiW bit to 0 (wait state).
3. To access an external area when the PM17 bit is 1, set the CSiW bit to 0 (wait state).
4. After reset, the PM17 bit is set to 0 (no wait state), bits CS0W to CS3W are set to 0 (wait state), and the CSE register is set to 00h (one wait state for $\overline{CS0}$ to $\overline{CS3}$). Therefore, all external areas are accessed with one wait state.

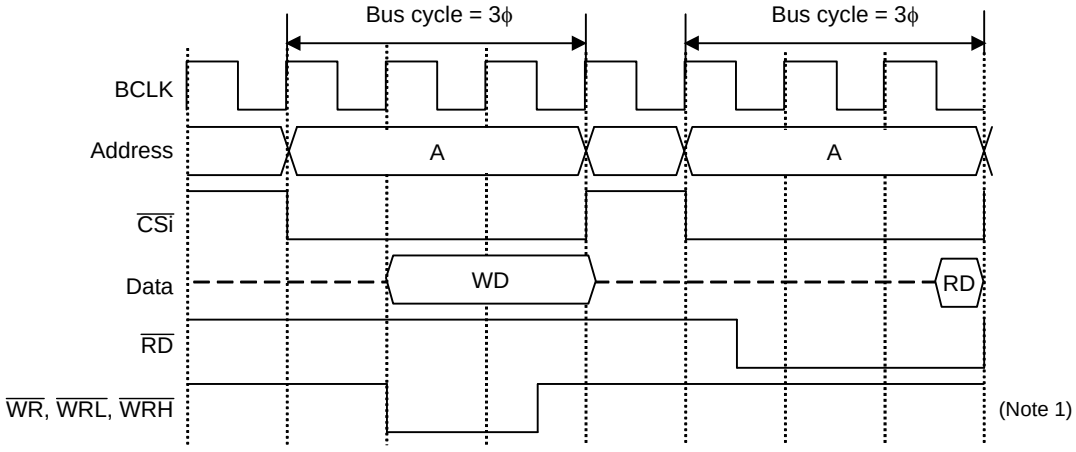
(1) Separate Bus, No Wait States



(2) Separate Bus, One Wait State (1ϕ + 1ϕ)



(3) Separate Bus, Two Wait States (1ϕ + 2ϕ)

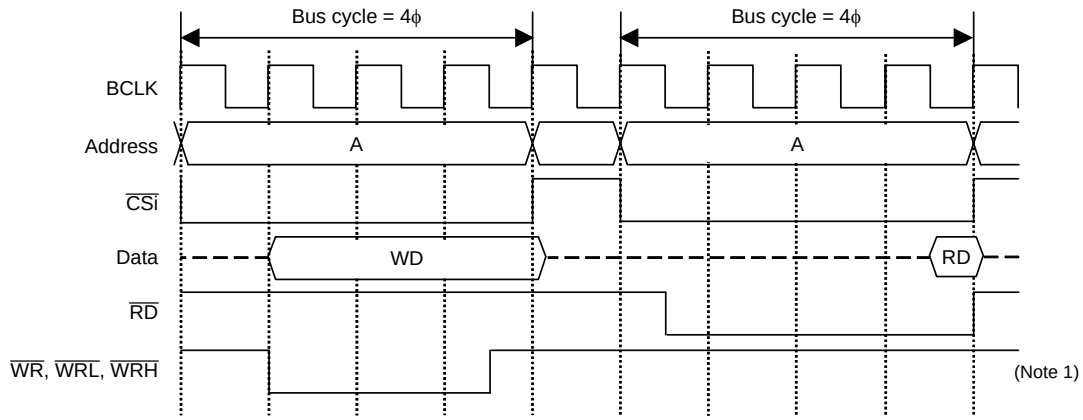


i = 0 to 3
A : Address RD : Read data (input) WD : Write data (output)

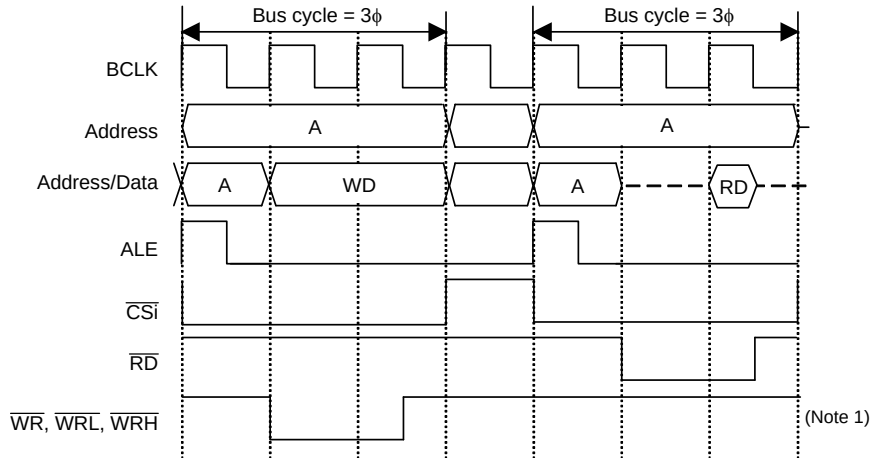
Note:
1. When accessing consecutively to the same chip-select area, $\overline{CSi}$ keeps ouputting low level.

Figure 11.6 Typical Bus Timings Using Software Wait States (1/4)

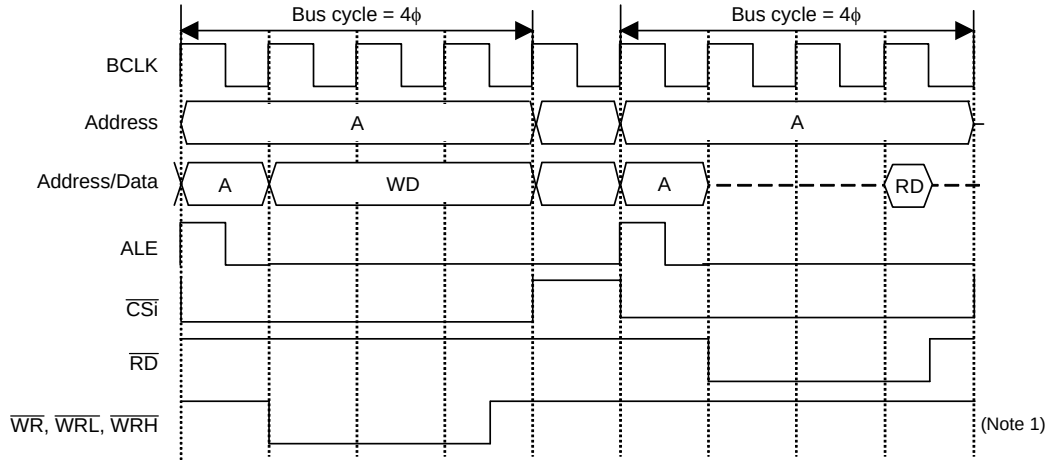
(1) Separate Bus, Three Wait States (1ϕ + 3ϕ)



(2) Multiplexed Bus, One or Two Wait States (1ϕ + 2ϕ)



(3) Multiplexed Bus, Three Wait States (1ϕ + 3ϕ)

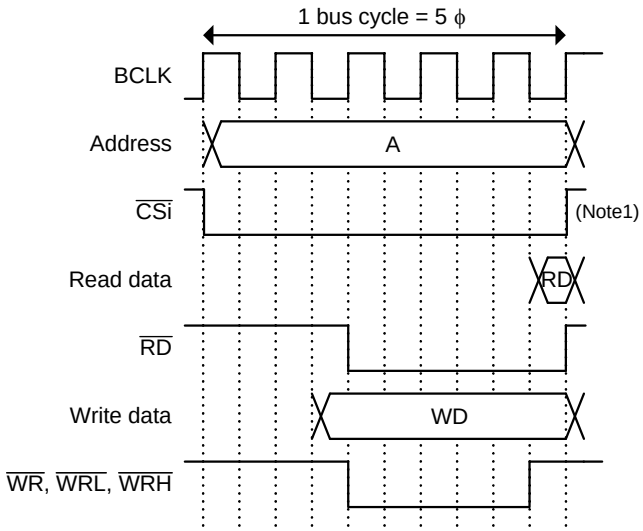


i = 0 to 3
A : Address RD : Read data (input) WD : Write data (output)

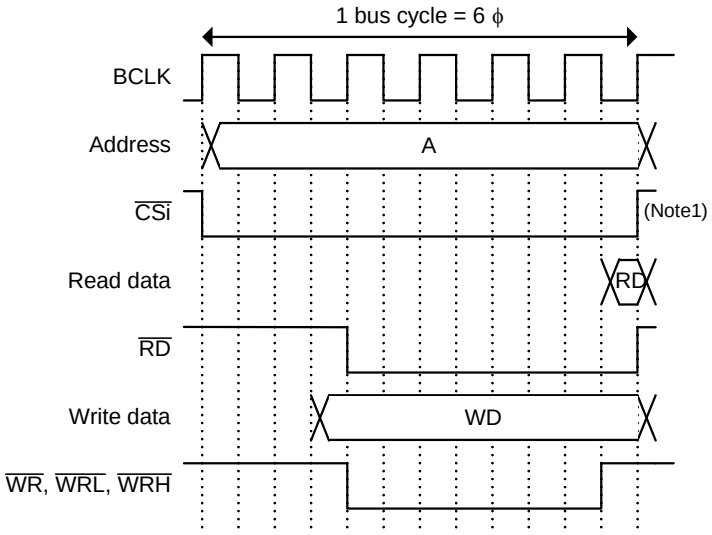
Note:
1. When accessing consecutively to the same chip-select area, CSi keeps ouputting low level.

Figure 11.7 Typical Bus Timings Using Software Wait States (2/4)

(1) Bus cycle 2 ϕ + 3 ϕ



(2) Bus cycle 2 ϕ + 4 ϕ

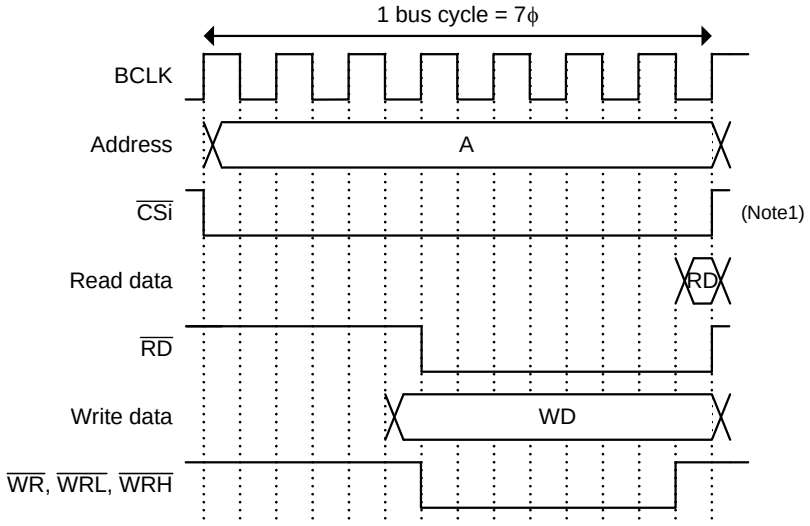


i = 0 to 3
A : Address RD : Read data (input) WD : Write data (output)

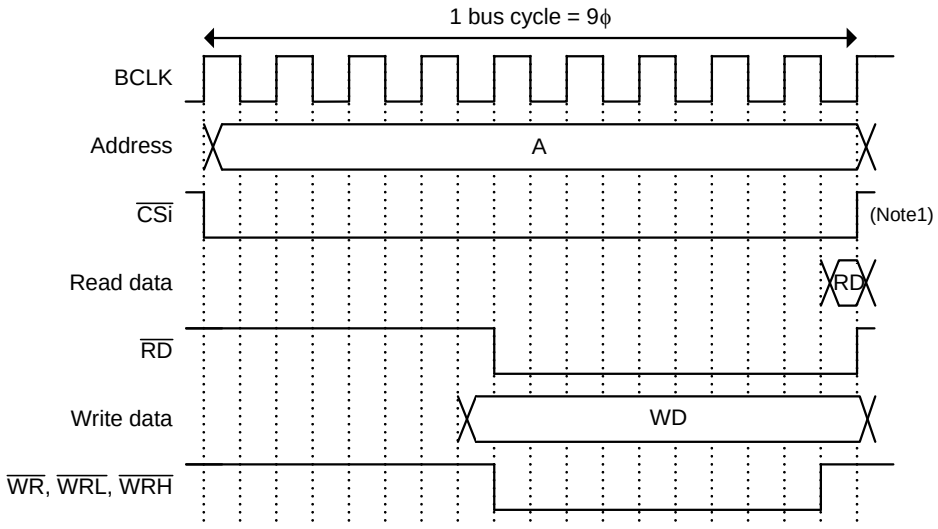
Note:
1. When accessing consecutively to the same chip-select area, CSi keeps ouputting low level.

Figure 11.8 Typical Bus Timings Using Software Wait States (3/4)

(3) Bus cycle 3ϕ + 4ϕ



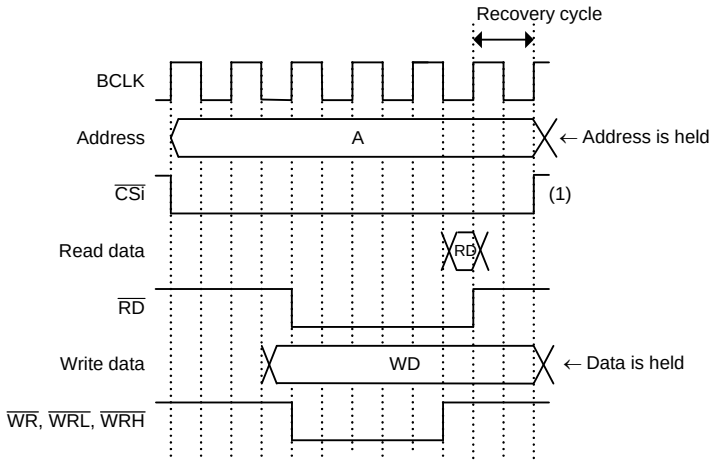
(4) Bus cycle 4ϕ + 5ϕ



i = 0 to 3
A : Address RD : Read data (input) WD : Write data (output)

Note:
1. When accessing consecutively to the same chip-select area, CSi keeps ouputting low level.

Figure 11.9 Typical Bus Timings Using Software Wait States (4/4)



i = 0 to 3
A: Address RD: Read data (input) WD: Write data (output)

Note:
1. When consecutively accessing to the same chip-select area, CSi keeps outputting a low level.
The above diagram shows a case under the following conditions:
- Bits EWR1 and EWR0 in the EWR register are 01b (one recovery cycle inserted).
- The CSiW bit in the CSR register is 0 (wait state).
- Bits CSEi1W and CSEi0W in the CSE register are 11b (select a bus cycle pattern by the EWC register).
- Bits EWCi1 and EWCi0 in the EWC register are 00b (2 ϕ + 3 ϕ).

Figure 11.10 Recovery Cycle

11.4 Notes on Bus

11.4.1 Reading Data Flash

When 2.7 V ≤ VCC1 ≤ 3.0 V and f(BCLK) ≥ 16 MHz, or when 3.0 V < VCC1 ≤ 5.5 V and f(BCLK) ≥ 20 MHz, one wait state is necessary to read data flash. Use the PM17 bit or the FMR17 bit to specify one wait state.

11.4.2 External Bus

When a hardware reset, power-on reset or voltage monitor 0 reset is performed with a high-level input on the CNVSS pin, contents of internal ROM cannot be read.

11.4.3 External Access Soon After Writing to the SFRs

When writing to the SFRs is followed by accessing to an external device, the write signal and $\overline{CSi}$ signal switch simultaneously. Thus, adjust the capacity of individual signal not to make a write signal delay.

12. Memory Space Expansion Function

Note

Do not use this function for the 80-pin package.

12.1 Introduction

The following describes the memory space expansion function. In memory expansion or microprocessor mode, the memory space expansion function allows the access space to be expanded. Table 12.1 lists Specifications of Memory Space Expansion Function. In this chapter, the space for the external devices accessed by the $\overline{CSi}$ (i = 0 to 3) signal is referred to as the $\overline{CSi}$ area.

Table 12.1 Specifications of Memory Space Expansion Function

Item	Specifications
1-Mbyte mode	• Memory space 1 Mbyte (no expansion) • Specify the space for the external devices accessed by the $\overline{CSi}$ signal.
4-Mbyte mode	• Memory space 4 Mbytes • Select bank numbers to access to data. • Allows the accessed address to be offset by 40000h • The $\overline{CSi}$ pin function differs depending on the area to be accessed.

i = 0 to 3

12.2 Registers

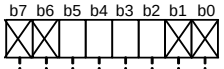
Table 12.2 lists registers related to the memory expansion function. Refer to 10. “Processor Mode” for the PM1 register.

Table 12.2 Register Structure

Address	Register Name	Register Symbol	After Reset
0005h	Processor Mode Register 1	PM1	0000 1000b
000Bh	Data Bank Register	DBR	00h

12.2.1 Data Bank Register (DBR)

Data Bank Register



Symbol	Address	After Reset
DBR	000Bh	00h

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	No register bits. If necessary, set to 0. Read as 0		—
OFS	Offset bit	0 : No offset 1 : Offset	RW
BSR0	Bank select bit	b5 b4 b3 0 0 0 : Bank 0 0 1 0 : Bank 2 1 0 0 : Bank 4 1 1 0 : Bank 6 b5 b4 b3 0 0 1 : Bank 1 0 1 1 : Bank 3 1 0 1 : Bank 5 1 1 1 : Bank 7	RW
BSR1			RW
BSR2			RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as 0		—

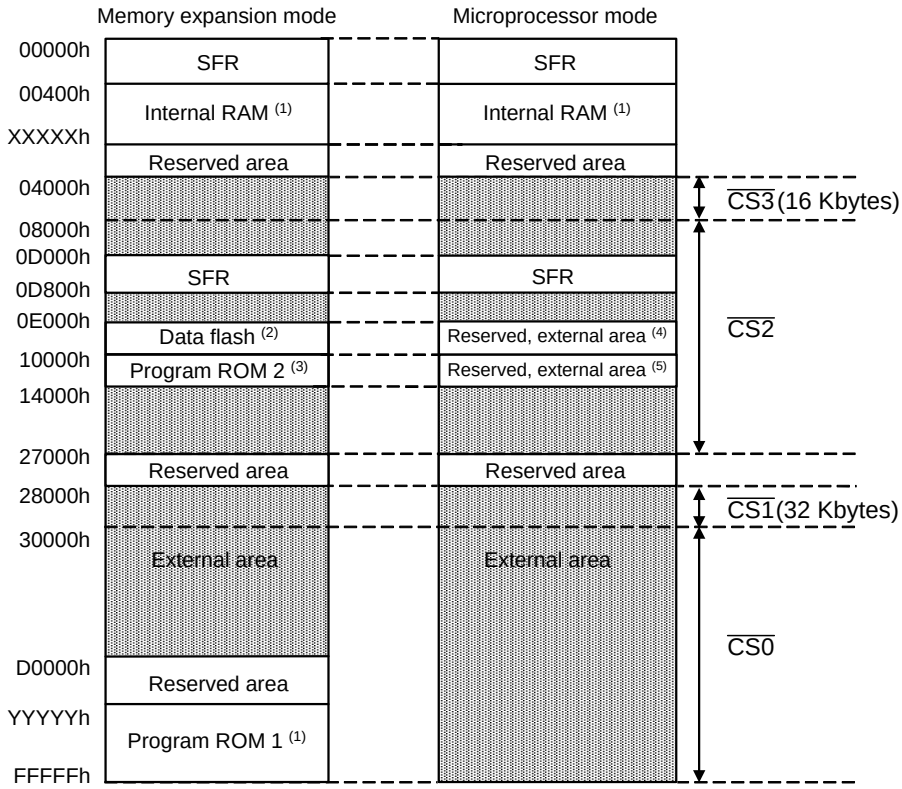
The DBR register is valid when bits PM01 to PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).

A write to the DBR register is enabled when bits PM15 to PM14 in the PM1 register is 11b (4-Mbyte mode).

12.3 Operations

12.3.1 1-Mbyte Mode

In 1-Mbyte mode, the memory space is 1 Mbyte. The external area to be accessed is specified using the $\overline{CSi}$ signals. Figure 12.1 and Figure 12.2 show the memory mapping and $\overline{CS}$ areas in 1-Mbyte mode.

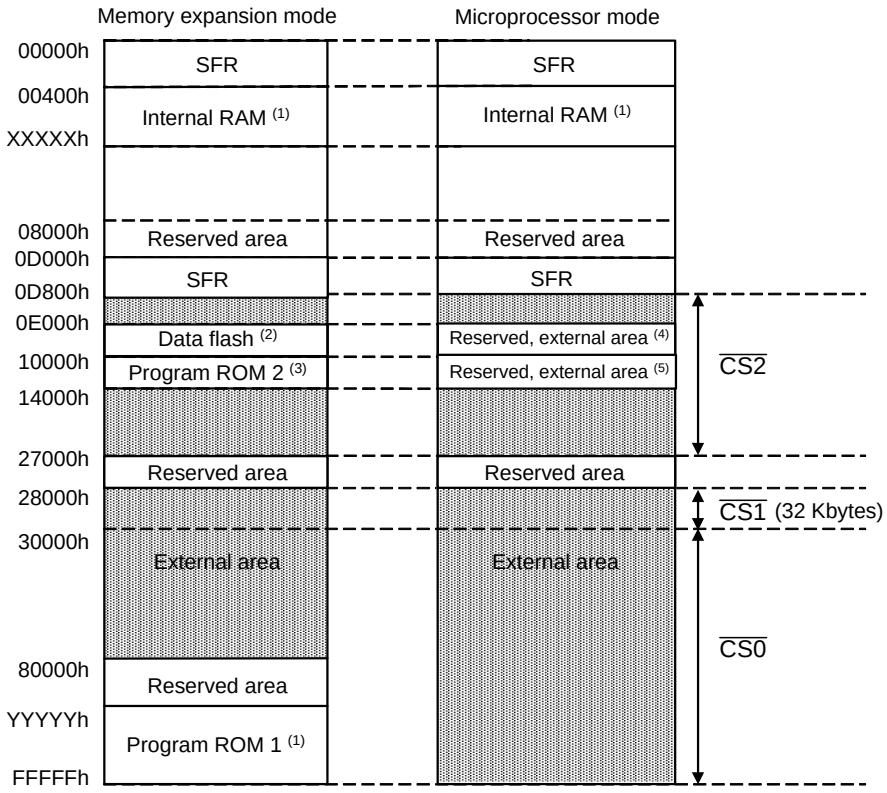


Notes :
1. When the PM13 bit in the PM1 register is 0, 15 Kbytes of the internal RAM and 192 Kbytes of the internal ROM can be used. See the table below for addresses XXXXXh and YYYYYh.

Internal RAM		Program ROM1	
Capacity	Address XXXXXh	Capacity	Address YYYYYh
12 Kbytes	033FFh	128 Kbytes	E0000h
20 Kbytes	03FFFh	256 Kbytes	D0000h
31 Kbytes	03FFFh	384 Kbytes	D0000h
47 Kbytes	03FFFh	512 Kbytes	D0000h
		640 Kbytes	D0000h
		768 Kbytes	D0000h

2. When the PM10 bit is 0, this area is used as an external area; when 1, used as internal ROM (data flash).
3. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when 0, used as internal ROM (program ROM 2).
4. When the PM10 bit is 0, this area is used as an external area; when 1, used as a reserved area.
5. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when 0, used as a reserved area.

Figure 12.1 Memory Mapping and $\overline{CS}$ Areas in 1-Mbyte Mode (PM13 = 0)



Notes :
1. See the table below for addresses XXXXXh and YYYYYh.

Internal RAM		Program ROM1	
Capacity	Address XXXXXh	Capacity	Address YYYYYh
12 Kbytes	033FFh	128 Kbytes	E0000h
20 Kbytes	053FFh	256 Kbytes	C0000h
31 Kbytes	07FFFh	384 Kbytes	A0000h
47 Kbytes	0BFFFh	512 Kbytes	80000h
		640 Kbytes	80000h (when IRON = 0) 60000h (when IRON = 1)
		768 Kbytes	80000h (when IRON = 0) 40000h (when IRON = 1)

IRON : Bit in the PRG2C register

2. When the PM10 bit is 0, this area is used as an external area; when 1, used as internal ROM (data flash).
3. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when 0, used as internal ROM (program ROM 2).
4. When the PM10 bit is 0, this area is used as an external area; when 1, used as a reserved area.
5. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when 0, used as a reserved area.

Figure 12.2 Memory Mapping and $\overline{CS}$ Areas in 1-Mbyte Mode (PM13 = 1)

12.3.2 4-Mbyte Mode

In 4-Mbyte mode, the memory space is 4 Mbytes. Set the IRON bit in the PRG2C register to 0 (program ROM 1 addresses 40000h to 7FFFFh disabled). Bits BSR2 to BSR0 in the DBR register select the bank number to be accessed to read or write data. Setting the OFS bit to 1 (offset) allows the accessed address to be offset by 40000h.

In 4-Mbyte mode, the $\overline{CSi}$ pin function differs depending on the area to be accessed.

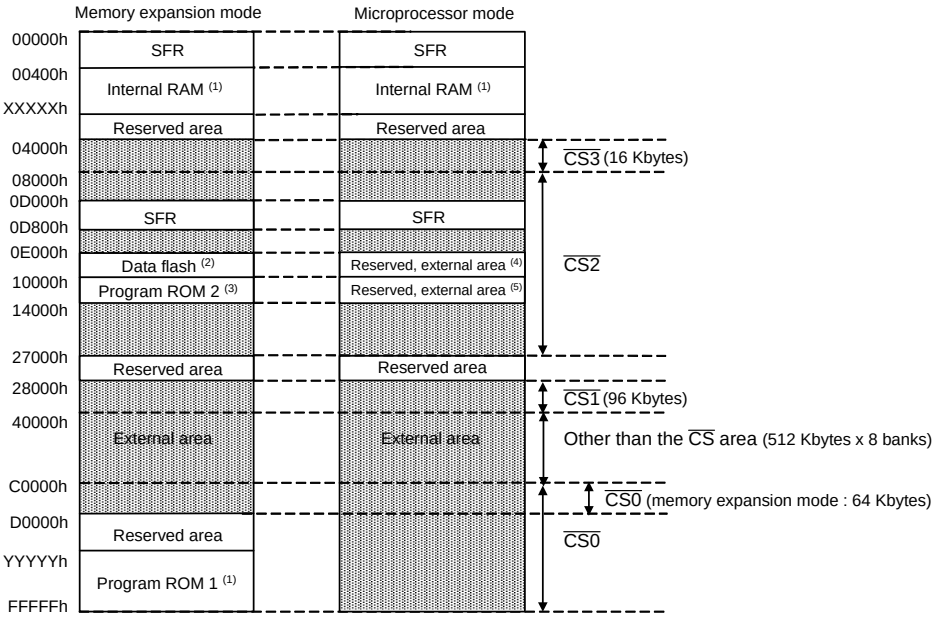
12.3.2.1 Addresses 04000h to 3FFFFh, C0000h to FFFFFh

- The $\overline{CSi}$ signal is output from the $\overline{CSi}$ pin (same operation as 1-Mbyte mode, except the last address of the $\overline{CS1}$ area is up to 3FFFFh).

12.3.2.2 Addresses 40000h to BFFFFh

- The $\overline{CS0}$ pin outputs a low-level signal.
- Pins $\overline{CS1}$ to $\overline{CS3}$ output the setting values of bits BSR2 to BSR0 (bank number).

Figure 12.3 and Figure 12.4 show the memory mapping and $\overline{CS}$ areas in 4-Mbyte mode. Note that banks 0 to 6 are data-only areas. Place programs in bank 7 or the $\overline{CSi}$ area.

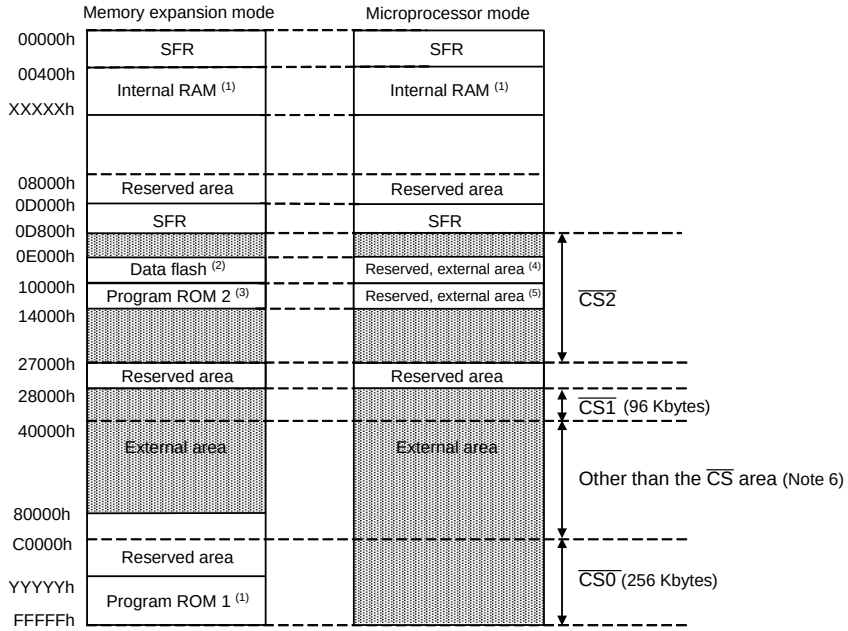


Notes :
1. When the PM13 bit in the PM1 register is 0, 15 Kbytes of the internal RAM and 192 Kbytes of the internal ROM can be used. See the table below for addresses XXXXXh and YYYYYh.

Internal RAM		Program ROM 1	
Capacity	Address XXXXXh	Capacity	Address YYYYYh
12 Kbytes	033FFh	128 Kbytes	E0000h
20 Kbytes	03FFFh	256 Kbytes	D0000h
31 Kbytes	03FFFh	384 Kbytes	D0000h
47 Kbytes	03FFFh	512 Kbytes	D0000h
		640 Kbytes	D0000h
		768 Kbytes	D0000h

2. When the PM10 bit is 0, this area is used as an external area; when 1, used as internal ROM (data flash).
3. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when 0, used as internal ROM (program ROM 2).
4. When the PM10 bit is 0, this area is used as an external area; when 1, used as a reserved area.
5. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when 0, used as a reserved area.
6. The $\overline{CS0}$ pin outputs a low signal, and pins $\overline{CS1}$ to $\overline{CS3}$ output a bank number.

Figure 12.3 Memory Mapping and $\overline{CS}$ Areas in 4-Mbyte Mode (PM13 = 0)



Notes :
1. See the table below for addresses XXXXXh and YYYYYh.

Internal RAM		Program ROM 1	
Capacity	Address XXXXXh	Capacity	Address YYYYYh
12 Kbytes	033FFh	128 Kbytes	E0000h
20 Kbytes	053FFh	256 Kbytes	C0000h
31 Kbytes	07FFFh	384 Kbytes	A0000h
47 Kbytes	0BFFFh	512 Kbytes	80000h
		640 Kbytes	80000h
		768 Kbytes	80000h

2. When the PM10 bit is 0, this area is used as an external area; when 1, used as internal ROM (data flash).
3. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when 0, used as internal ROM (program ROM 2).
4. When the PM10 bit is 0, this area is used as an external area; when 1, used as a reserved area.
5. When the PRG2C0 bit in the PRG2C register is 1, this area is used as an external area; when 0, used as a reserved area.
6. The $\overline{CS0}$ pin outputs a low signal, and pins $\overline{CS1}$ to $\overline{CS3}$ output a bank number.

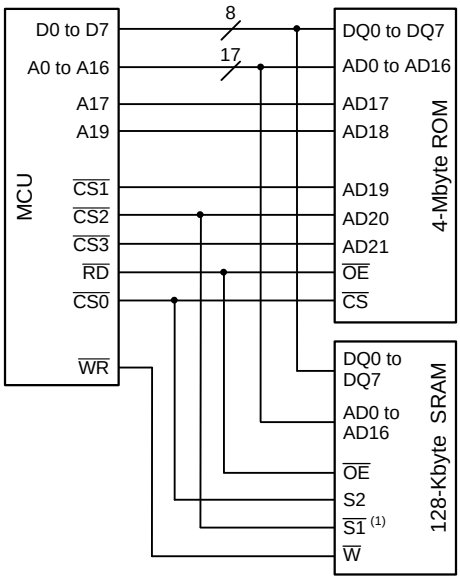
Figure 12.4 Memory Mapping and $\overline{CS}$ Areas in 4-Mbyte Mode (PM13 = 1)

In the example below, the $\overline{CS}$ pin of a 4-Mbyte ROM is connected to the MCU's $\overline{CS0}$ pin. The 4-Mbyte ROM address input pins AD21, AD20, and AD19 are connected to the MCU's $\overline{CS3}$, $\overline{CS2}$, and $\overline{CS1}$ pins, respectively. The address input AD18 pin is connected to the MCU's A19 pin. Figure 12.6 to Figure 12.8 show the relationship of addresses between the 4-Mbyte ROM and the MCU in the connection example of Figure 12.5.

In microprocessor mode or memory expansion mode, where the PM13 bit in the PM1 register is 0, banks are located every 512 Kbytes. Setting the OFS bit in the DBR register to 1 (offset) allows the accessed address to be offset by 40000h, allowing even data overlapping at a bank boundary to be accessed in succession.

In memory expansion mode, where the PM13 bit is 1, each 512-Kbyte bank can be accessed in 256 Kbyte units by switching them with the OFS bit.

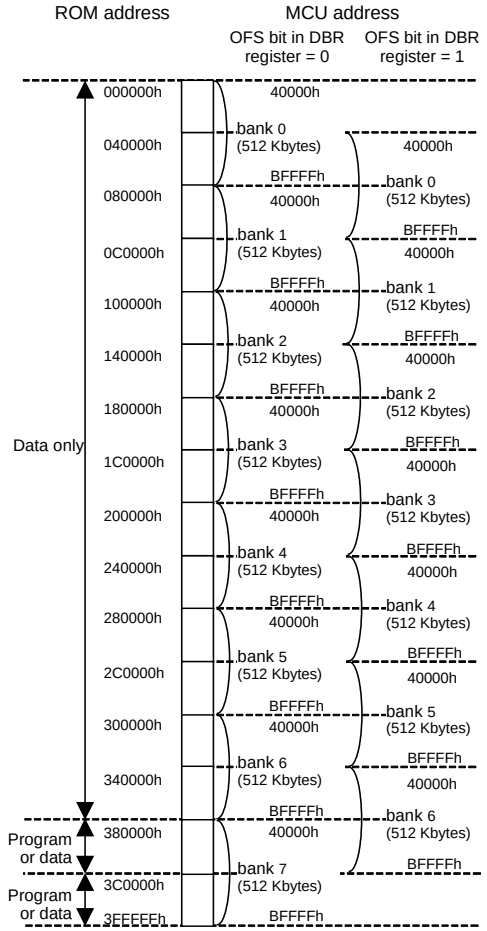
Because the SRAM can be accessed when the chip select signals S2 is high and $\overline{S1}$ is low, $\overline{CS0}$ and $\overline{CS2}$ can be connected to S2 and $\overline{S1}$, respectively. If SRAM does not have the input pins that accept high active and low active chip select signals ($\overline{S1}$, S2), $\overline{CS0}$ and $\overline{CS2}$ should be decoded externally to the chip.



Note :
1. If only one chip select pin ($\overline{S1}$ or S2) is present, an external circuit must be used for decoding.

Figure 12.5 External Memory Connection Example in 4-Mbyte Mode

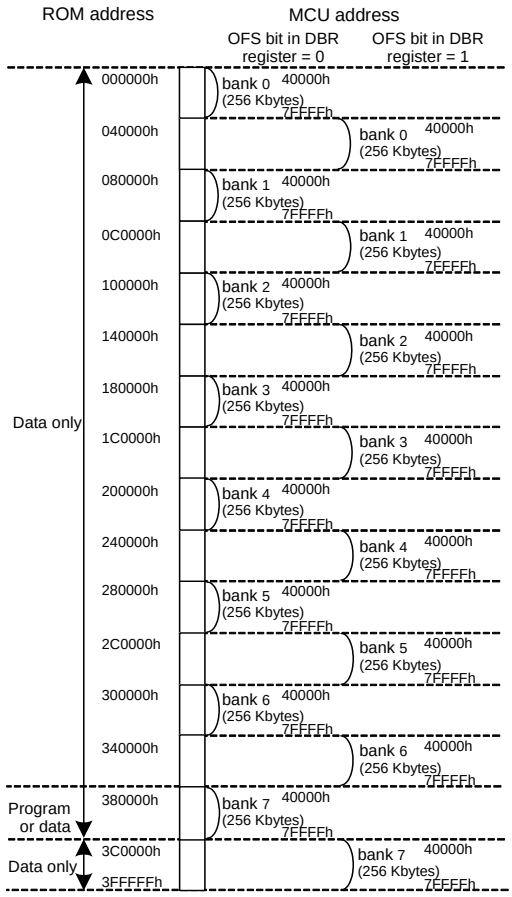
Memory expansion mode where PM13 is 0



Bank Number	OFS	Access Area	Output from the MCU Pins								
			$\overline{CS}$ Output			Address Output					
			$\overline{CS3}$	$\overline{CS2}$	$\overline{CS1}$	A19	A18	A17	A16	A15 to A0	
0	0	40000h	0	0	0	0	1	0	0	0000h	000000h
		BFFFFFh	0	0	0	1	0	1	1	FFFFh	07FFFFh
	1	40000h	0	0	0	1	0	0	0	0000h	040000h
		BFFFFFh	0	0	1	0	1	1	1	FFFFh	0BFFFFh
1	0	40000h	0	0	1	0	1	0	0	0000h	080000h
		BFFFFFh	0	0	1	1	0	1	1	FFFFh	0FFFFFh
	1	40000h	0	0	1	1	0	0	0	0000h	0C0000h
		BFFFFFh	0	1	0	0	1	1	1	FFFFh	13FFFFh
2	0	40000h	0	1	0	0	1	0	0	0000h	100000h
		BFFFFFh	0	1	0	1	0	1	1	FFFFh	17FFFFh
	1	40000h	0	1	0	1	0	0	0	0000h	140000h
		BFFFFFh	0	1	1	0	1	1	1	FFFFh	1BFFFFh
3	0	40000h	0	1	1	0	1	0	0	0000h	180000h
		BFFFFFh	0	1	1	1	0	1	1	FFFFh	1FFFFFh
	1	40000h	0	1	1	1	0	0	0	0000h	1C0000h
		BFFFFFh	1	0	0	0	1	1	1	FFFFh	23FFFFh
4	0	40000h	1	0	0	0	1	0	0	0000h	200000h
		BFFFFFh	1	0	0	1	0	1	1	FFFFh	27FFFFh
	1	40000h	1	0	0	1	0	0	0	0000h	240000h
		BFFFFFh	1	0	1	0	1	1	1	FFFFh	2BFFFFh
5	0	40000h	1	0	1	0	1	0	0	0000h	280000h
		BFFFFFh	1	0	1	1	0	1	1	FFFFh	2FFFFFh
	1	40000h	1	0	1	1	0	0	0	0000h	2C0000h
		BFFFFFh	1	1	0	0	1	1	1	FFFFh	33FFFFh
6	0	40000h	1	1	0	0	1	0	0	0000h	300000h
		BFFFFFh	1	1	0	1	0	1	1	FFFFh	37FFFFh
	1	40000h	1	1	0	1	0	0	0	0000h	340000h
		BFFFFFh	1	1	1	0	1	1	1	FFFFh	3BFFFFh
7	0	40000h	1	1	1	0	1	0	0	0000h	380000h
		7FFFFh	1	1	1	0	1	1	1	FFFFh	3BFFFFh
		80000h	1	1	1	1	0	0	0	0000h	3C0000h
		BFFFFFh	1	1	1	1	0	1	1	FFFFh	3FFFFFh
		C0000h	1	1	1	1	1	0	0	0000h	3C0000h
		CFFFFFh	1	1	1	1	1	0	0	FFFFh	3CFFFFh
		D0000h									Internal ROM access
		DFFFFFh									Internal ROM access
		D0000h									Internal ROM access
		DFFFFFh									Internal ROM access
			A21	A20	A19	A18	N.C.	A17	A16	A15 to A0	4-Mbyte ROM access area
			Address input for 4-Mbyte ROM								

Figure 12.6 Relationship between Addresses in 4-Mbyte ROM and Those in MCU (1/3)

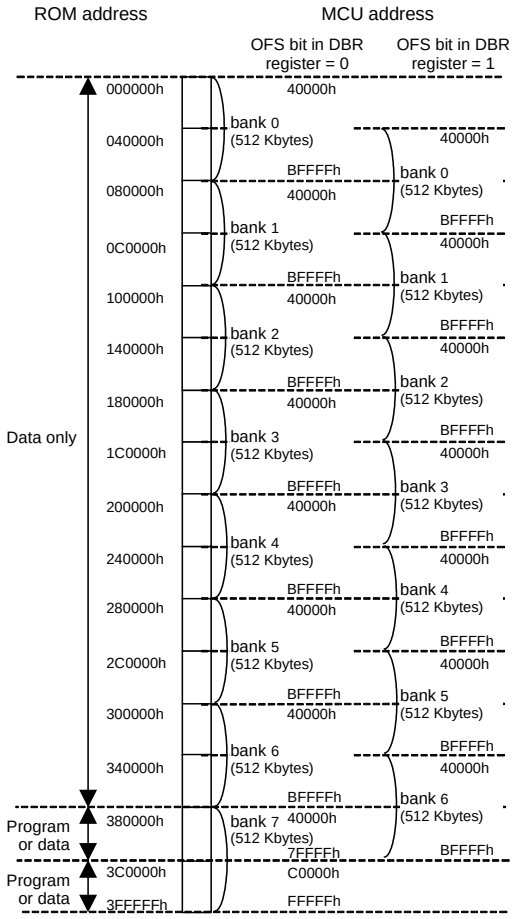
Memory expansion mode where PM13 is 1



Bank Number	OFS	Access Area	Output from the MCU Pins								
			$\overline{CS}$ Output			Address Output					
			$\overline{CS3}$	$\overline{CS2}$	$\overline{CS1}$	A19	A18	A17	A16	A15 to A0	
0	0	40000h	0	0	0	0	1	0	0	0000h	000000h
		7FFFFh	0	0	0	0	1	1	1	FFFFh	03FFFFh
	1	40000h	0	0	0	1	0	0	0	0000h	040000h
		7FFFFh	0	0	0	1	0	1	1	FFFFh	07FFFFh
1	0	40000h	0	0	1	0	1	0	0	0000h	080000h
		7FFFFh	0	0	1	0	1	1	1	FFFFh	0BFFFFh
	1	40000h	0	0	1	1	0	0	0	0000h	0C0000h
		7FFFFh	0	0	1	1	0	1	1	FFFFh	0FFFFFh
2	0	40000h	0	1	0	0	1	0	0	0000h	100000h
		7FFFFh	0	1	0	0	1	1	1	FFFFh	13FFFFh
	1	40000h	0	1	0	1	0	0	0	0000h	140000h
		7FFFFh	0	1	0	1	0	1	1	FFFFh	17FFFFh
3	0	40000h	0	1	1	0	1	0	0	0000h	180000h
		7FFFFh	0	1	1	0	1	1	1	FFFFh	1BFFFFh
	1	40000h	0	1	1	1	0	0	0	0000h	1C0000h
		7FFFFh	0	1	1	1	0	1	1	FFFFh	1FFFFFh
4	0	40000h	1	0	0	0	1	0	0	0000h	200000h
		7FFFFh	1	0	0	0	1	1	1	FFFFh	23FFFFh
	1	40000h	1	0	0	1	0	0	0	0000h	240000h
		7FFFFh	1	0	0	1	0	1	1	FFFFh	27FFFFh
5	0	40000h	1	0	1	0	1	0	0	0000h	280000h
		7FFFFh	1	0	1	0	1	1	1	FFFFh	2BFFFFh
	1	40000h	1	0	1	1	0	0	0	0000h	2C0000h
		7FFFFh	1	0	1	1	0	1	1	FFFFh	2FFFFFh
6	0	40000h	1	1	0	0	1	0	0	0000h	300000h
		7FFFFh	1	1	0	0	1	1	1	FFFFh	33FFFFh
	1	40000h	1	1	0	1	0	0	0	0000h	340000h
		7FFFFh	1	1	0	1	0	1	1	FFFFh	37FFFFh
7	0	40000h	1	1	1	0	1	0	0	0000h	380000h
		7FFFFh	1	1	1	0	1	1	1	FFFFh	3BFFFFh
		80000h									Internal ROM access
		FFFFFh									Internal ROM access
7	1	40000h	1	1	1	1	0	0	0	0000h	3C0000h
		7FFFFh	1	1	1	1	0	1	1	FFFFh	3FFFFFh
		80000h									Internal ROM access
		FFFFFh									Internal ROM access
			A21	A20	A19	A18	N.C.	A17	A16	A15 to A0	4-Mbyte ROM access area
			Address input for 4-Mbyte ROM								

Figure 12.7 Relationship between Addresses in 4-Mbyte ROM and Those in MCU (2/3)

Microprocessor mode



Bank Number	OFS	Access Area	Output from the MCU Pins								4-Mbyte ROM access area
			$\overline{CS}$ Output			Address Output					
			$\overline{CS3}$	$\overline{CS2}$	$\overline{CS1}$	A19	A18	A17	A16	A15 to A0	
0	0	40000h	0	0	0	0	1	0	0	0000h	000000h
		BFFFFFh	0	0	0	1	0	1	1	FFFFh	07FFFFh
	1	40000h	0	0	0	1	0	0	0	0000h	040000h
		BFFFFFh	0	0	1	0	1	1	1	FFFFh	0BFFFFh
1	0	40000h	0	0	1	0	1	0	0	0000h	080000h
		BFFFFFh	0	0	1	1	0	1	1	FFFFh	0FFFFFh
	1	40000h	0	0	1	1	0	0	0	0000h	0C0000h
		BFFFFFh	0	1	0	0	1	1	1	FFFFh	13FFFFh
2	0	40000h	0	1	0	0	1	0	0	0000h	100000h
		BFFFFFh	0	1	0	1	0	1	1	FFFFh	17FFFFh
	1	40000h	0	1	0	1	0	0	0	0000h	140000h
		BFFFFFh	0	1	1	0	1	1	1	FFFFh	1BFFFFh
3	0	40000h	0	1	1	0	1	0	0	0000h	180000h
		BFFFFFh	0	1	1	1	0	1	1	FFFFh	1FFFFFh
	1	40000h	0	1	1	1	0	0	0	0000h	1C0000h
		BFFFFFh	1	0	0	0	1	1	1	FFFFh	23FFFFh
4	0	40000h	1	0	0	0	1	0	0	0000h	200000h
		BFFFFFh	1	0	0	1	0	1	1	FFFFh	27FFFFh
	1	40000h	1	0	0	1	0	0	0	0000h	240000h
		BFFFFFh	1	0	1	0	1	1	1	FFFFh	2BFFFFh
5	0	40000h	1	0	1	0	1	0	0	0000h	280000h
		BFFFFFh	1	0	1	1	0	1	1	FFFFh	2FFFFFh
	1	40000h	1	0	1	1	0	0	0	0000h	2C0000h
		BFFFFFh	1	1	0	0	1	1	1	FFFFh	33FFFFh
6	0	40000h	1	1	0	0	1	0	0	0000h	300000h
		BFFFFFh	1	1	0	1	0	1	1	FFFFh	37FFFFh
	1	40000h	1	1	0	1	0	0	0	0000h	340000h
		BFFFFFh	1	1	1	0	1	1	1	FFFFh	3BFFFFh
7	0	40000h	1	1	1	0	1	0	0	0000h	380000h
		7FFFFh	1	1	1	0	1	1	1	FFFFh	3BFFFFh
		80000h	1	1	1	1	0	0	0	0000h	3C0000h
		BFFFFFh	1	1	1	1	0	1	1	FFFFh	3FFFFFh
		C0000h	1	1	1	1	1	0	0	0000h	3C0000h
		FFFFFh	1	1	1	1	1	1	1	FFFFh	3FFFFFh
			A21	A20	A19	A18	N.C.	A17	A16	A15 to A0	
			Address input for 4-Mbyte ROM								

Figure 12.8 Relationship between Addresses in 4-Mbyte ROM and Those in MCU (3/3)

13. Programmable I/O Ports

Note

P1, P4_4 to P4_7, P7_2 to P7_5, and P9_1 of the 80-pin package have no external connections. Program the direction bits of these ports to 1 (output mode) and the output data to 0 (low level).
For the 80-pin and 100-pin packages, do not access the addresses of registers P11 to P14, PD11 to PD14 and PUR3.

13.1 Introduction

Table 13.1 lists Programmable I/O Ports Specifications (hereafter referred to as I/O ports).
Each pin functions as an I/O port, a peripheral function input/output, or a bus control pin.
To set peripheral functions, refer to the description for the individual function. To use ports as peripheral function input/output pins, refer to 13.4 “Peripheral Function I/O”.
To use ports as bus control pins, refer to 11.3.5 “External Bus Control”.

Table 13.1 Programmable I/O Ports Specifications

Item		Specification		
		128-pin package	100-pin package	80-pin package
The number of ports	Total	114	88	71
	CMOS output	111	85	68
	N-channel open-drain output	3	3	3
Input/output	VCC2 level	P0 to P5, P12, P13 (1)	P0 to P5	-
	VCC1 level	P6 to P11, P14 (1)	P6 to P10	P0, P2 to P10
Input/output level		Select input or output for each individual port by a program.		
Select function		Select a pull-up resistor in 4-bit units.		

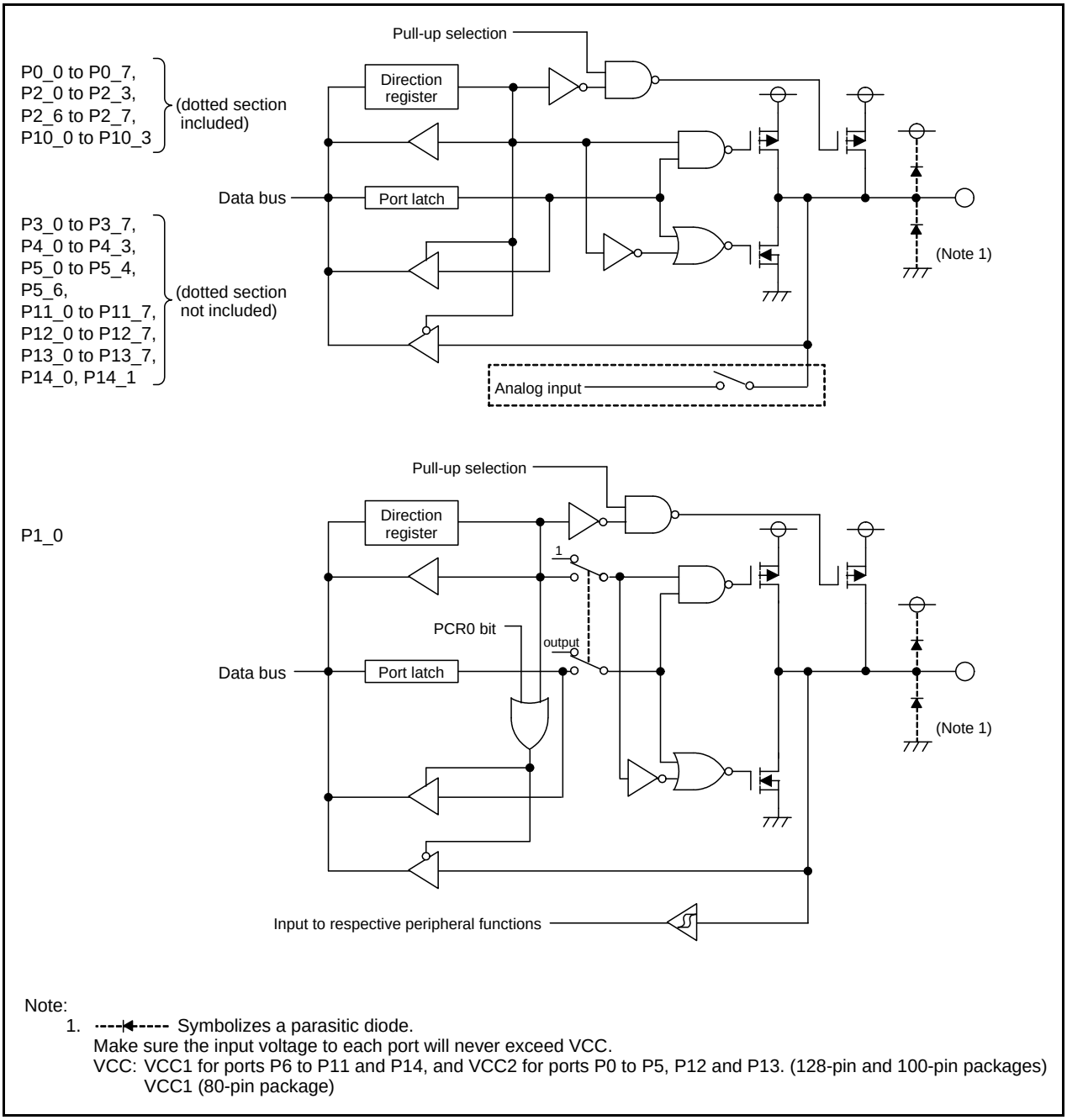
Note:
1. P11 to P14 can be used when the PU37 bit in the PUR3 register is 1 (P11 to P14 enabled).

Table 13.2 I/O Pins

Pin Name	I/O Type	Function
P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7	I/O	Input/output port CMOS output, pull-up resistor selectable
P7_0 to P7_7	I/O	Input/output port P7_0 to P7_1: N-channel open-drain output, no pull-up resistor P7_2 to P7_7: CMOS output, pull-up resistor selectable
P8_0 to P8_7	I/O	Input/output port P8_0 to P8_4, P8_6, P8_7: CMOS output, pull-up resistor selectable P8_5: N-channel open-drain output, no pull-up resistor
P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0 to P14_1	I/O	Input/output port CMOS output, pull-up resistor selectable

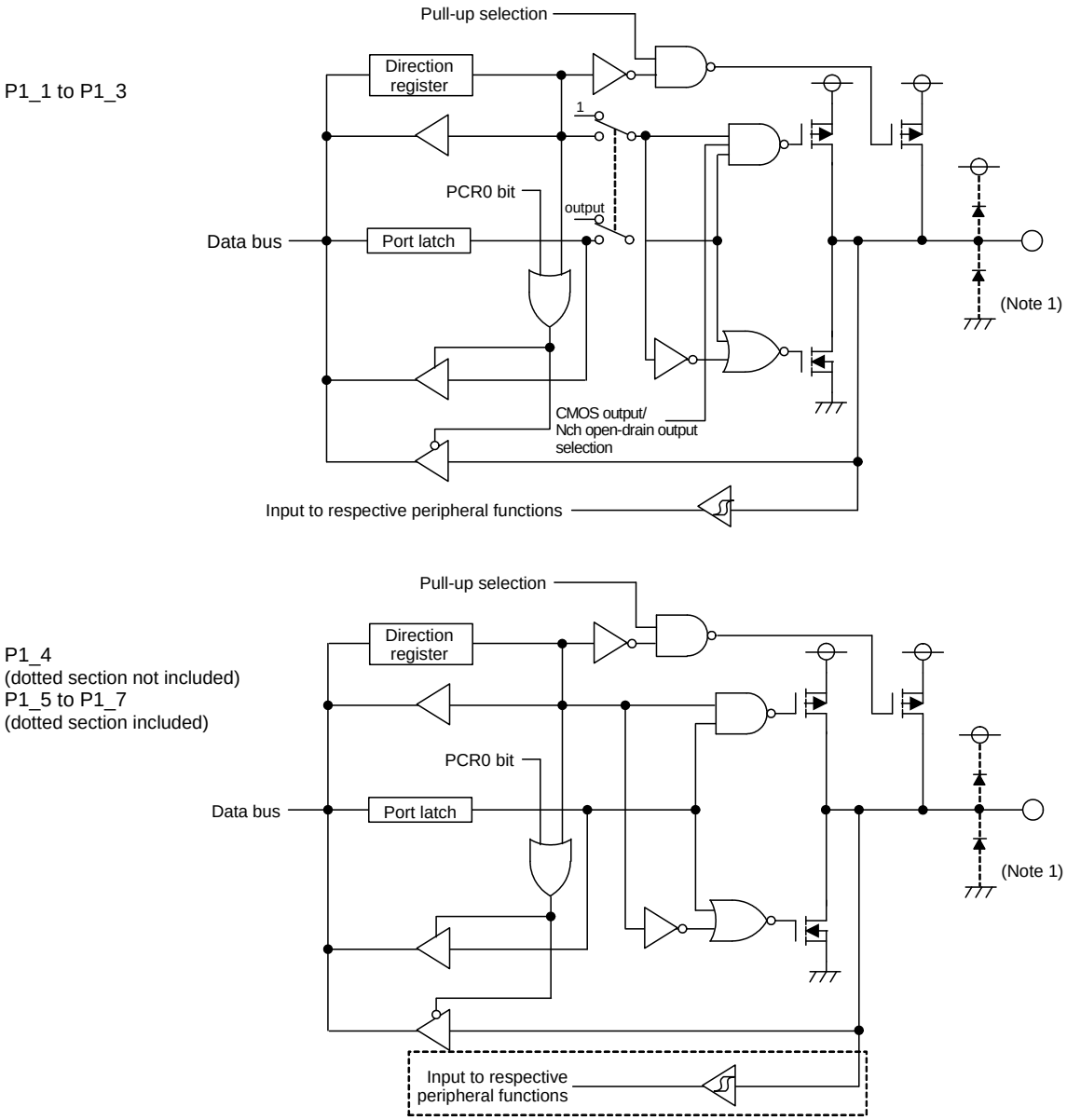
13.2 I/O Ports and Pins

Figure 13.1 to Figure 13.9 show I/O Ports, and Figure 13.10 shows I/O Pins.



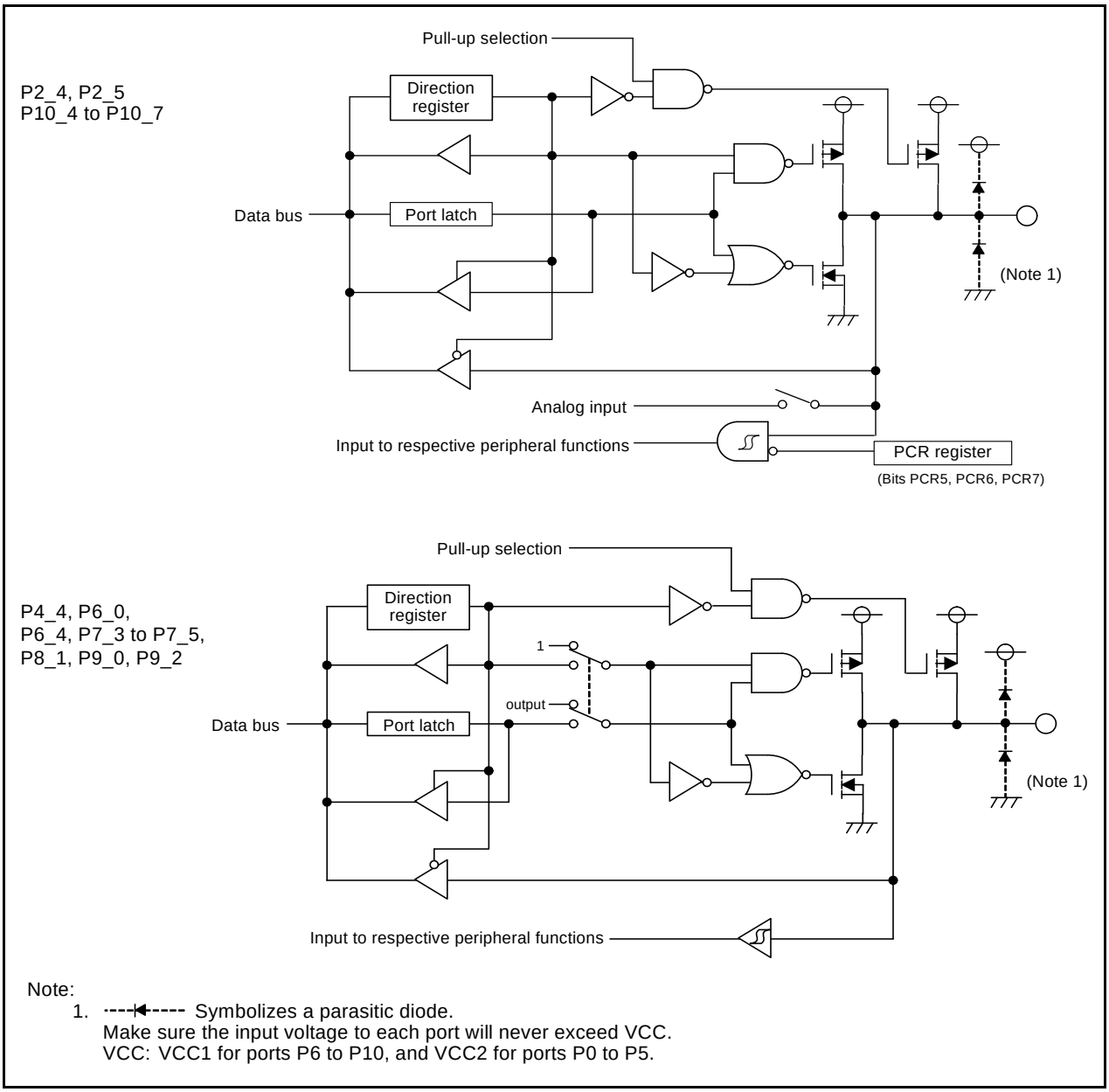
Note:
1. ----|◄|---- Symbolizes a parasitic diode.
Make sure the input voltage to each port will never exceed VCC.
VCC: VCC1 for ports P6 to P11 and P14, and VCC2 for ports P0 to P5, P12 and P13. (128-pin and 100-pin packages)
VCC1 (80-pin package)

Figure 13.1 I/O Ports (1/9)



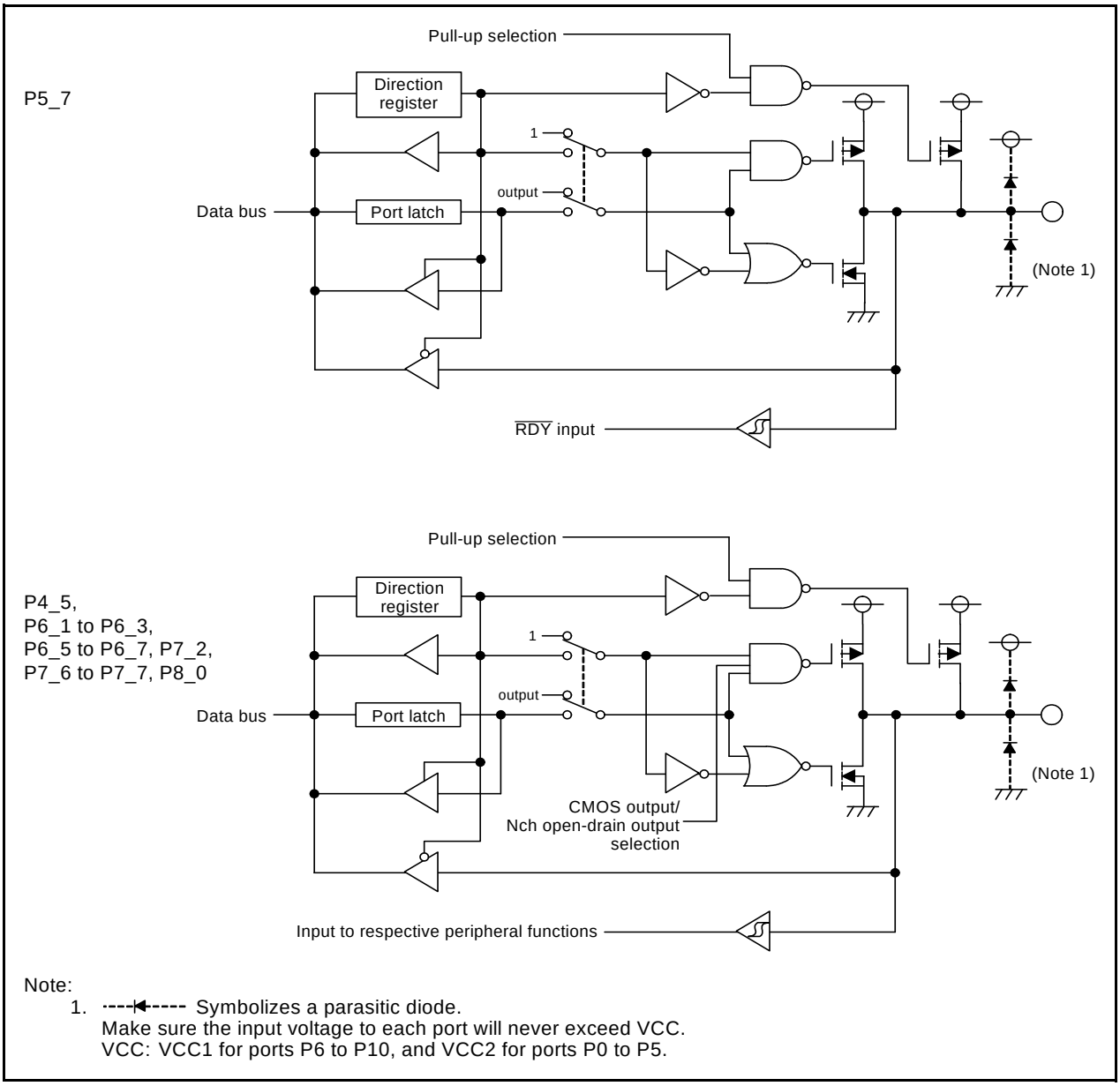
Note:
1. ----◄----- Symbolizes a parasitic diode.
Make sure the input voltage to each port will never exceed VCC.
VCC: VCC1 for ports P6 to P11 and P14, and VCC2 for ports P0 to P5, P12 and P13. (128-pin and 100-pin packages)
VCC1 (80-pin package).

Figure 13.2 I/O Ports (2/9)



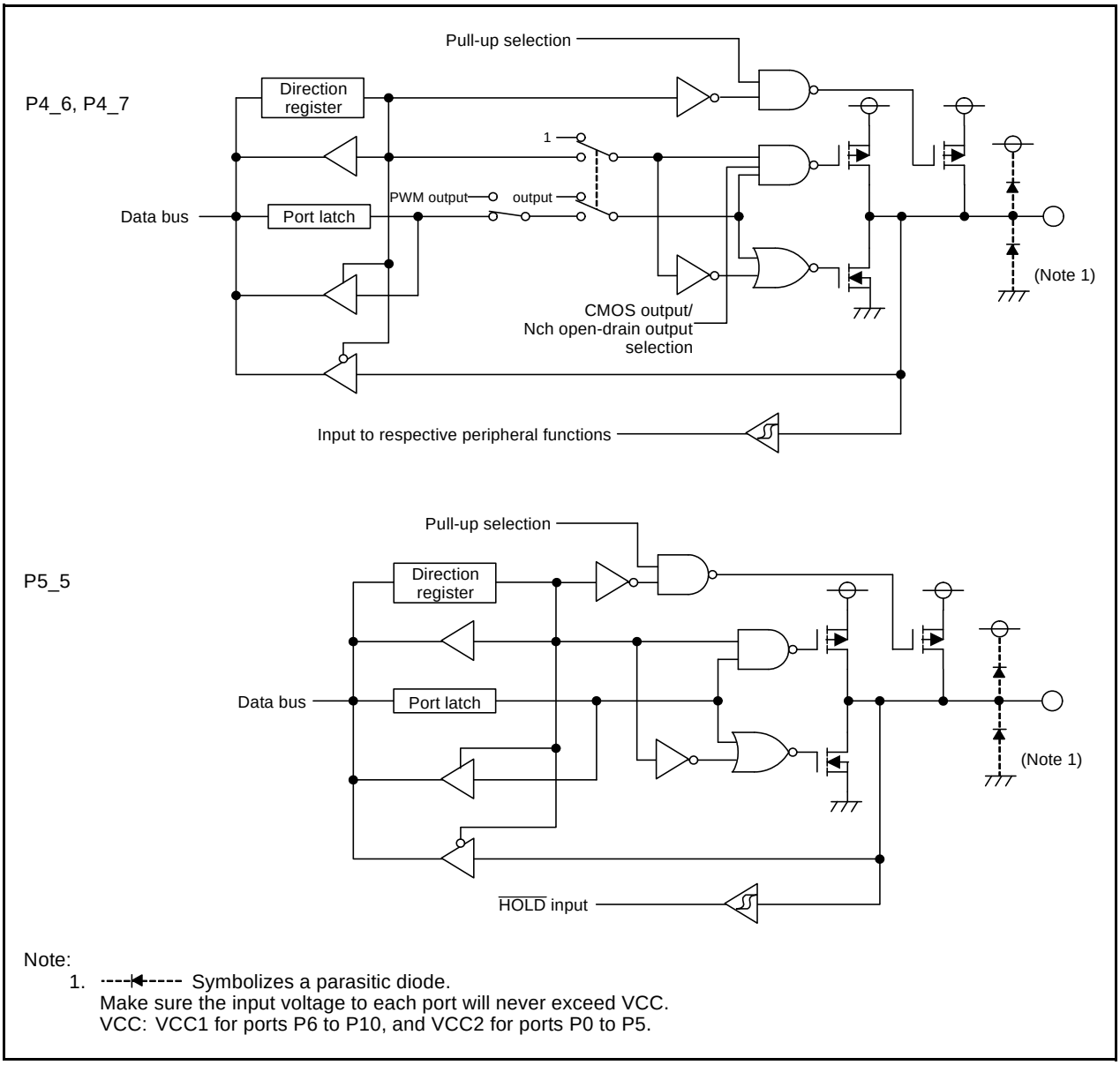
Note:
1. ----|◄----- Symbolizes a parasitic diode.
Make sure the input voltage to each port will never exceed VCC.
VCC: VCC1 for ports P6 to P10, and VCC2 for ports P0 to P5.

Figure 13.3 I/O Ports (3/9)



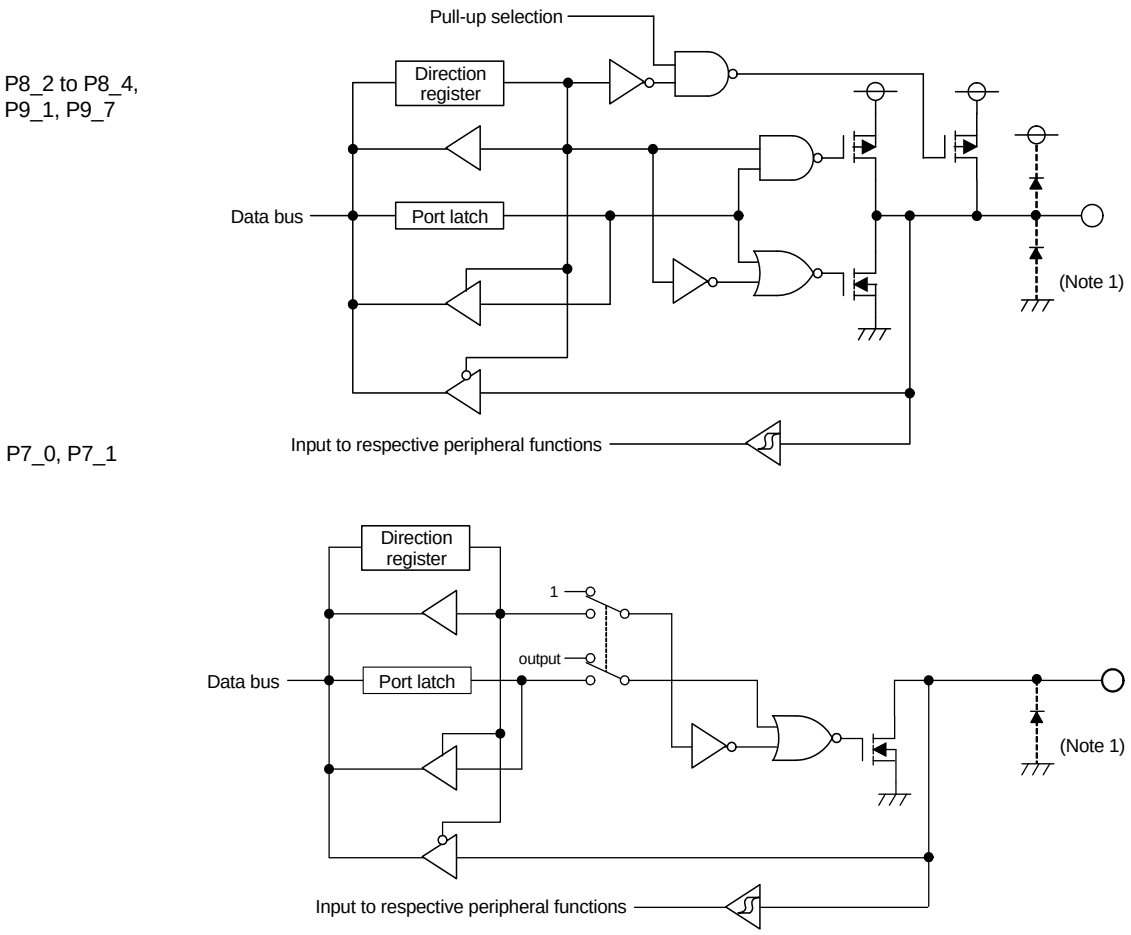
Note:
1. ----|◄----- Symbolizes a parasitic diode.
Make sure the input voltage to each port will never exceed VCC.
VCC: VCC1 for ports P6 to P10, and VCC2 for ports P0 to P5.

Figure 13.4 I/O Ports (4/9)



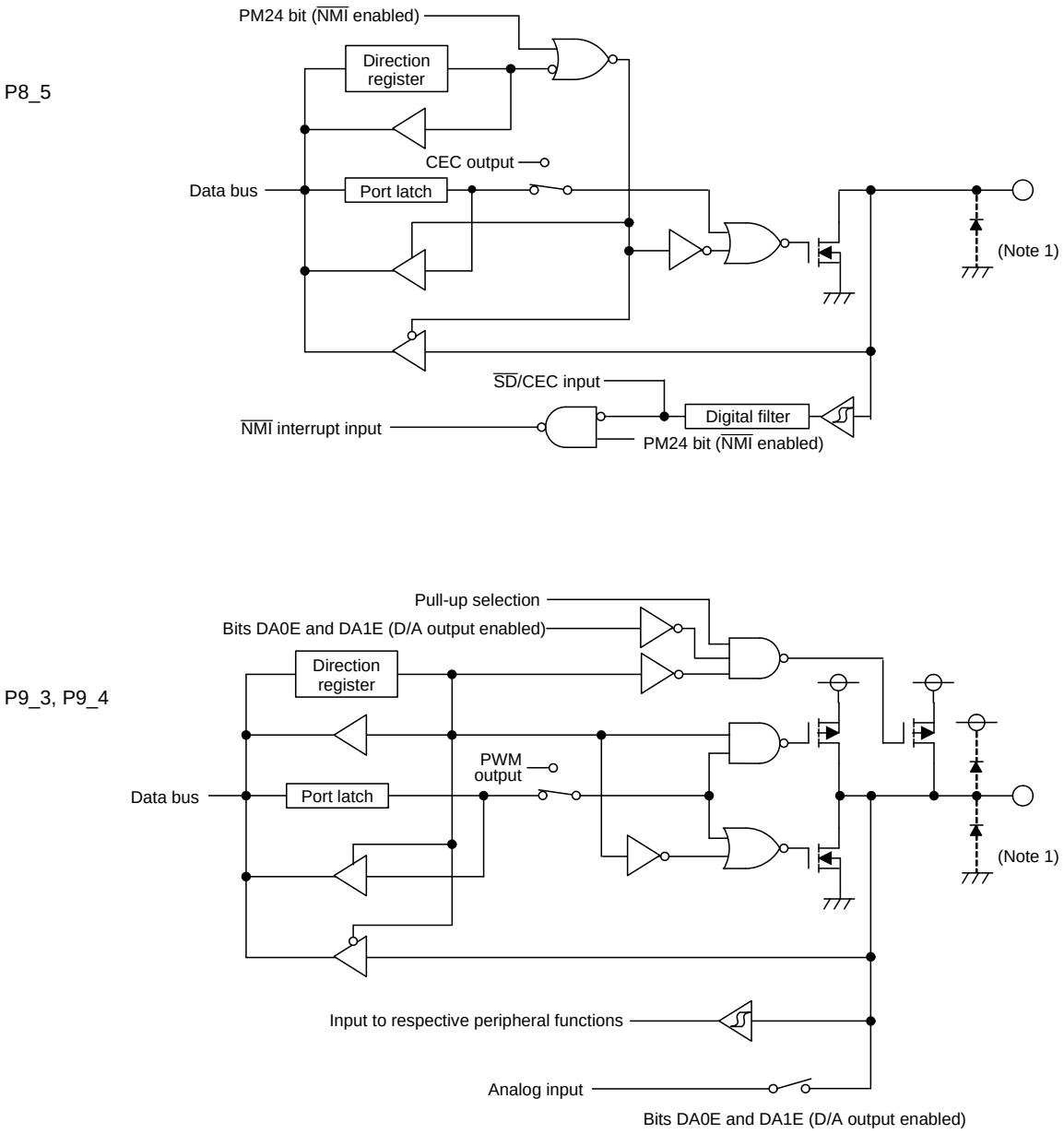
Note:
1. ----|◄----- Symbolizes a parasitic diode.
Make sure the input voltage to each port will never exceed VCC.
VCC: VCC1 for ports P6 to P10, and VCC2 for ports P0 to P5.

Figure 13.5 I/O Ports (5/9)



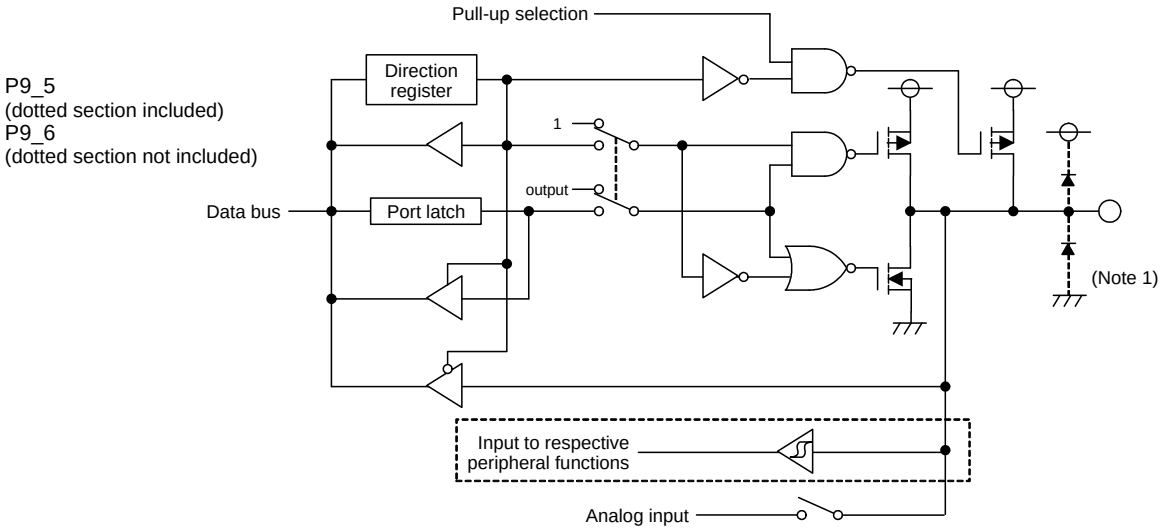
Note:
1. ----|◄----- Symbolizes a parasitic diode.
Make sure the input voltage to each port will never exceed VCC.
VCC: VCC1 for ports P6 to P11 and P14, and VCC2 for ports P0 to P5, P12 and P13. (128-pin and 100-pin packages)
VCC1 (80-pin package)

Figure 13.6 I/O Ports (6/9)



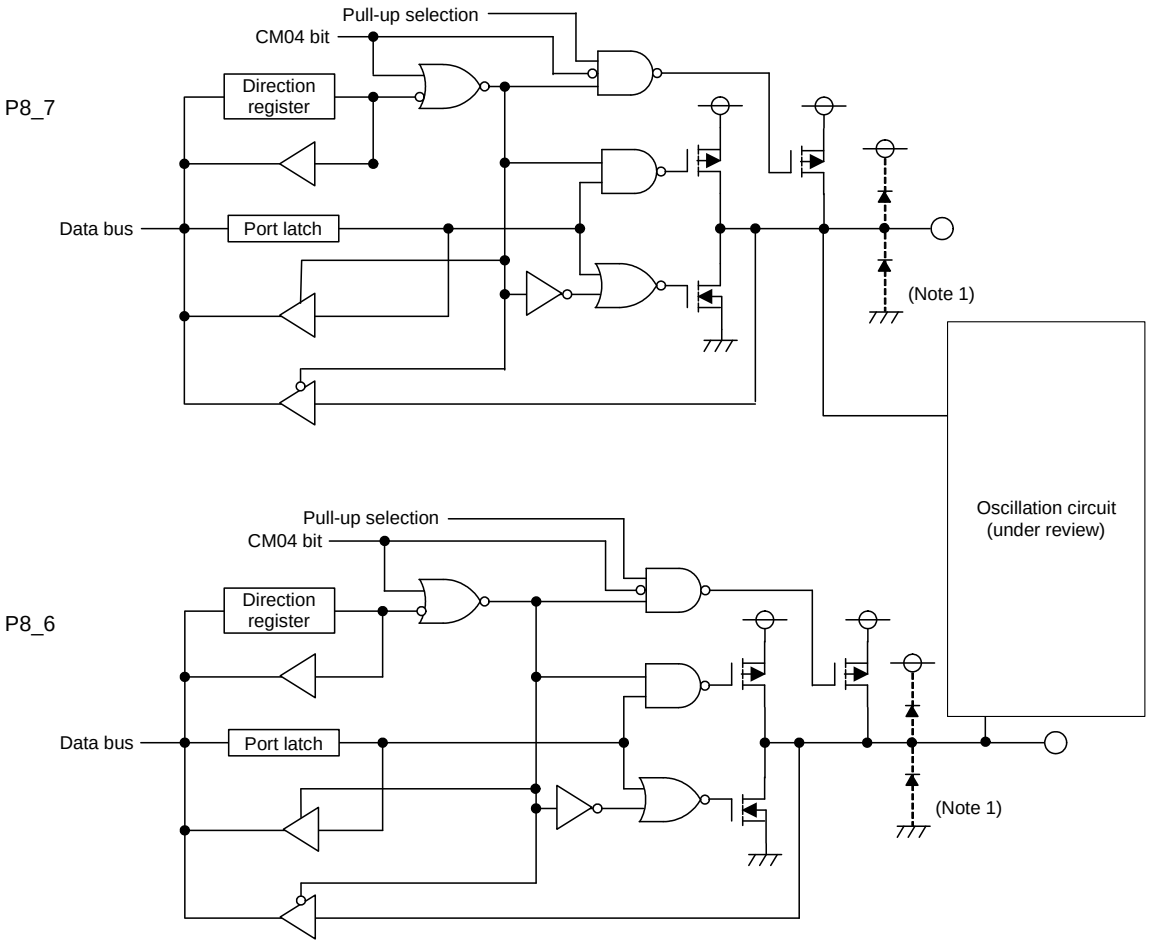
Note:
1. ----◄----- Symbolizes a parasitic diode.
Make sure the input voltage to each port will never exceed VCC.
VCC: VCC1 for ports P6 to P11 and P14, and VCC2 for ports P0 to P5, P12 and P13. (128-pin and 100-pin packages)
VCC1 (80-pin package)

Figure 13.7 I/O Ports (7/9)



Note:
1. ----◄---- Symbolizes a parasitic diode.
Make sure the input voltage to each port will never exceed VCC.
VCC: VCC1 for ports P6 to P11 and P14, and VCC2 for ports P0 to P5, P12 and P13. (128-pin and 100-pin packages)
VCC1 (80-pin package)

Figure 13.8 I/O Ports (8/9)



Note:
1. ----◄----- Symbolizes a parasitic diode.
Make sure the input voltage to each port will never exceed VCC.
VCC: VCC1 for ports P6 to P11 and P14, and VCC2 for ports P0 to P5, P12 and P13. (128-pin and 100-pin packages)
VCC1 (80-pin package)

Figure 13.9 I/O Ports (9/9)

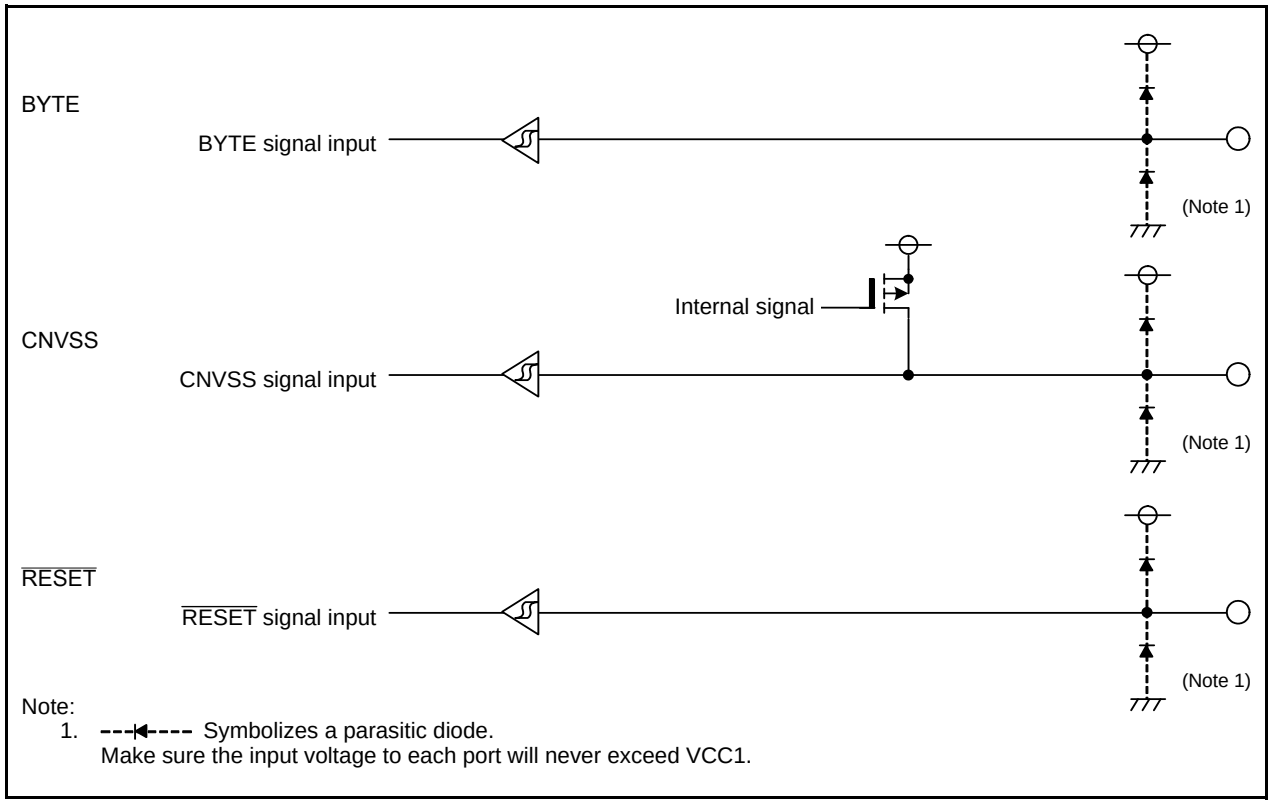


Figure 13.10 I/O Pins

13.3 Registers

Table 13.3 Register Structure

Address	Register Name	Register Symbol	After Reset
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	0000 0000b (1) 0000 0010b
0362h	Pull-Up Control Register 2	PUR2	00h
0363h	Pull-Up Control Register 3	PUR3	00h
0366h	Port Control Register	PCR	0000 0XX0b
0369h	NMI/SD Digital Filter Register	NMIDF	XXXX X000b
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h	Port P4 Register	P4	XXh
03E9h	Port P5 Register	P5	XXh
03EAh	Port P4 Direction Register	PD4	00h
03EBh	Port P5 Direction Register	PD5	00h
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	00h
03F4h	Port P10 Register	P10	XXh
03F5h	Port P11 Register	P11	XXh
03F6h	Port P10 Direction Register	PD10	00h
03F7h	Port P11 Direction Register	PD11	00h
03F8h	Port P12 Register	P12	XXh
03F9h	Port P13 Register	P13	XXh
03FAh	Port P12 Direction Register	PD12	00h
03FBh	Port P13 Direction Register	PD13	00h
03FCh	Port P14 Register	P14	XXh
03FEh	Port P14 Direction Register	PD14	XXXX XX00b

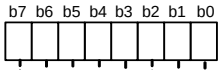
Note:

1. Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:
   - 00000000b when input on the CNVSS pin is low
   - 00000010b when input on the CNVSS pin is high

   Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, or oscillation stop detection reset are as follows:
   - 00000000b when bits PM01 to PM00 in the PM0 register are 00b (single-chip mode).
   - 00000010b when bits PM01 to PM00 in the PM0 register are 01b (memory expansion mode) or 11b (microprocessor mode).

13.3.1 Pull-Up Control Register 0 (PUR0)

Pull-Up Control Register 0



Symbol: PUR0 | Address: 0360h | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
PU00	P0_0 to P0_3 pull-up	0 : Not pulled high 1 : Pulled high	RW
PU01	P0_4 to P0_7 pull-up		RW
PU02	P1_0 to P1_3 pull-up		RW
PU03	P1_4 to P1_7 pull-up		RW
PU04	P2_0 to P2_3 pull-up		RW
PU05	P2_4 to P2_7 pull-up		RW
PU06	P3_0 to P3_3 pull-up		RW
PU07	P3_4 to P3_7 pull-up		RW

In memory expansion or microprocessor mode, the corresponding register contents can be modified, but the pins are not pulled high.

PU0i Bit (b7-b0) (i = 0 to 7)

The pin for which the PU0i bit is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.

13.3.2 Pull-Up Control Register 1 (PUR1)

Pull-Up Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0

Symbol: PUR1 | Address: 0361h | After Reset: 0000 0000b, 0000 0010b

Bit Symbol	Bit Name	Function	RW
PU10	P4_0 to P4_3 pull-up	0 : Not pulled high 1 : Pulled high	RW
PU11	P4_4 to P4_7 pull-up		RW
PU12	P5_0 to P5_3 pull-up		RW
PU13	P5_4 to P5_7 pull-up		RW
PU14	P6_0 to P6_3 pull-up		RW
PU15	P6_4 to P6_7 pull-up		RW
PU16	P7_2 to P7_3 pull-up		RW
PU17	P7_4 to P7_7 pull-up		RW

Values after hardware reset, power-on reset, or voltage monitor 0 reset are as follows:

- 00000000b when input on the CNVSS pin is low
- 00000010b when input on the CNVSS pin is high

Values after voltage monitor 1 reset, voltage monitor 2 reset, software reset, watchdog timer reset, ro oscillation stop detection reset are as follows:

- 00000000b when bits PM01 to PM00 are 00b (single-chip mode)
- 00000010b when bits PM01 to PM00 are 01b (memory expansion mode) or 11b (microprocessor mode)

PU10 (P4_0 to P4_3 Pull-Up) (b0)
PU11 (P4_4 to P4_7 Pull-Up) (b1)
PU12 (P5_0 to P5_3 Pull-Up) (b2)
PU13 (P5_4 to P5_7 Pull-Up) (b3)

The pin for which the bit in the PU1i bit (i = 0 to 3) is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.
In memory expansion and microprocessor modes, pins are not pulled high although the contents of these bits can be modified.

PU14 (P6_0 to P6_3 Pull-Up) (b4)
PU15 (P6_4 to P6_7 Pull-Up) (b5)
PU17 (P7_4 to P7_7 Pull-Up) (b7)

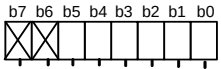
The pin for which the bit in the PU1i bit (i = 4, 5, 7) is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.

PU16 (P7_2 to P7_3 Pull-Up) (b6)

The pin for which the bit in the PU16 bit is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.
Pins P7_0 and P7_1 are not pulled high.

13.3.3 Pull-Up Control Register 2 (PUR2)

Pull-up Control Register 2



Symbol: PUR2 | Address: 0362h | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
PU20	P8_0 to P8_3 pull-up	0 : Not pulled high 1 : Pulled high	RW
PU21	P8_4 to P8_7 pull-up		RW
PU22	P9_0 to P9_3 pull-up		RW
PU23	P9_4 to P9_7 pull-up		RW
PU24	P10_0 to P10_3 pull-up		RW
PU25	P10_4 to P10_7 pull-up		RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as 0		—

The pin for which the bit in the PUR2 register is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.

PU21 (P8_4 to P8_7 Pull-Up) (b1)

The P8_5 pin is not pulled high.

13.3.4 Pull-Up Control Register 3 (PUR3)

Pull-Up Control Register 3

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
								PUR3	0363h	00h

Bit Symbol	Bit Name	Function	RW
PU30	P11_0 to P11_3 pull-up	0 : Not pulled high 1 : Pulled high	RW
PU31	P11_4 to P11_7 pull-up		RW
PU32	P12_0 to P12_3 pull-up		RW
PU33	P12_4 to P12_7 pull-up		RW
PU34	P13_0 to P13_3 pull-up		RW
PU35	P13_4 to P13_7 pull-up		RW
PU36	P14_0, P14_1 pull-up		RW
PU37	P11 to P14 enable bit	0 : Disabled 1 : Enabled	RW

PU3i Bit (b6-b0) (i = 0 to 6)

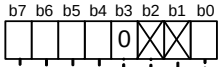
The pin for which the PU3i bit is 1 (pulled high) and the direction bit is 0 (input mode) is pulled high.

PU37 (P11 to P14 Enable Bit) (b7)

When the PU37 bit is 1 (P11 to P14 enabled), registers P11 to P14 and registers PD0 to PD14 are enabled.

13.3.5 Port Control Register (PCR)

Port Control Register



Symbol: PCR | Address: 0366h | After Reset: 0000 0XX0b

Bit Symbol	Bit Name	Function	RW
PCR0	Port P1 control bit	Operation performed when the P1 register is read 0 : When the port is set to input, the input levels of pins P1_0 to P1_7 are read. When set to output, the port latch is read. 1 : The port latch is read regardless of whether the port is set to input or output.	RW
— (b2-b1)	No register bits. If necessary, set to 0. Read as undefined		—
— (b3)	Reserved bit	Set to 0	RW
PCR4	CEC output enable bit	0 : CEC output disabled 1 : CEC output enabled	RW
PCR5	$\overline{\text{INT6}}$ input enable bit	0 : Enabled 1 : Disabled	RW
PCR6	$\overline{\text{INT7}}$ input enable bit	0 : Enabled 1 : Disabled	RW
PCR7	Key input enable bit	0 : Enabled 1 : Disabled	RW

PCR0 (Port P1 Control Bit) (b0)

When the P1 register is read after the PCR0 bit is set to 1, the corresponding port latch is read regardless of the PD1 register setting.

13.3.6 Port Pi Registers (Pi) (i = 0 to 14)

Port Pi Register (i = 0 to 13)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
P0 to P3	03E0h, 03E1h, 03E4h, 03E5h	Undefined
P4 to P7	03E8h, 03E9h, 03ECh, 03EDh	Undefined
P8 to P11	03F0h, 03F1h, 03F4h, 03F5h	Undefined
P12 to P13	03F8h, 03F9h	Undefined

Bit Symbol	Bit Name	Function	RW
Pi_0	Port Pi_0 bit	The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register 0 : Low level 1 : High level	RW
Pi_1	Port Pi_1 bit		RW
Pi_2	Port Pi_2 bit		RW
Pi_3	Port Pi_3 bit		RW
Pi_4	Port Pi_4 bit		RW
Pi_5	Port Pi_5 bit		RW
Pi_6	Port Pi_6 bit		RW
Pi_7	Port Pi_7 bit		RW

Port P14 Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
P14	03FCh	Undefined

Bit Symbol	Bit Name	Function	RW
P14_0	Port P14_0 bit	The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register 0 : Low level 1 : High level	RW
P14_1	Port P14_1 bit		RW
— (b7-b2)	No register bit. If necessary, set to 0. Read as undefined value		—

Data input/output to and from external devices are accomplished by reading and writing to the Pi register.

Each bit of the Pi register consists of a port latch to hold the output data and a circuit to read the pin status.

For ports set to input mode, the input level of the pin can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register.

For ports set to output mode, the port latch can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register. The data written to the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

In memory expansion and microprocessor modes, the Pi register for the pins functioning as bus control pins (A0 to A19, D0 to D15, $\overline{CS0}$ to $\overline{CS3}$, $\overline{RD}$, $\overline{WRL}$/$\overline{WR}$, $\overline{WRH}$/$\overline{BHE}$, ALE, $\overline{RDY}$, $\overline{HOLD}$, $\overline{HLDA}$, and BCLK) cannot be modified (writing a value has no effect).

Since P7_0, P7_1, and P8_5 are N-channel open- drain ports, when set to 1, the pin status becomes high-impedance.

When the CM04 bit in the CM0 register is 1 (XCIN-XCOUT oscillation function) and bits PD8_6 and PD8_7 in the PD8 register are 0 (input mode), values of bits P8_6 and P8_7 in the P8 register are undefined.

Registers P11 to P14 are enabled when the PU37 bit in the PUR3 register is 1 (P11 to P14 enabled). Access to registers P11 to P14 after setting the PU37 bit to 1. When the PU37 bit in the PUR3 register is 0 (P11 to P14 disabled), the contents of registers P11 to P14 are retained. In this case, read as undefined value.

13.3.7 Port Pi Direction Registers (PDi) (i = 0 to 14)

Port Pi Direction Register (i = 0 to 13)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
PD0 to PD3	03E2h, 03E3h, 03E6h, 03E7h	00h
PD4 to PD7	03EAh, 03EBh, 03EEh, 03EFh	00h
PD8 to PD11	03F2h, 03F3h, 03F6h, 03F7h	00h
PD12 to PD13	03FAh, 03FBh	00h

Bit Symbol	Bit Name	Function	RW
PDi_0	Port Pi_0 direction bit	0 : Input mode (Functions as an input port) 1 : Output mode (Functions as an output port)	RW
PDi_1	Port Pi_1 direction bit		RW
PDi_2	Port Pi_2 direction bit		RW
PDi_3	Port Pi_3 direction bit		RW
PDi_4	Port Pi_4 direction bit		RW
PDi_5	Port Pi_5 direction bit		RW
PDi_6	Port Pi_6 direction bit		RW
PDi_7	Port Pi_7 direction bit		RW

Port P14 Direction Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
PD14	03FEh	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
PD14_0	Port P14_0 direction bit	0 : Input mode (Functions as an input port) 1 : Output mode (Functions as an output port)	RW
PD14_1	Port P14_1 direction bit		RW
— (b7-b2)	No register bit. If necessary, set to 0. Read as undefined value		—

Write to the PD9 register in the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled).

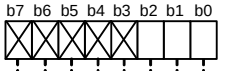
These registers select whether I/O ports are to be used for input or output. Each bit in the PDi register has its corresponding port.

In memory expansion mode or microprocessor mode, the PDi register for the pins functioning as bus control pins (A0 to A19, D0 to D15, $\overline{CS0}$ to $\overline{CS3}$, $\overline{RD}$, $\overline{WRL}/\overline{WR}$, $\overline{WRH}/\overline{BHE}$, ALE, $\overline{RDY}$, $\overline{HOLD}$, $\overline{HLDA}$, and BCLK) cannot be modified (Writing a value has no effect).

Registers PD11 to PD14 are enabled when the PU37 bit in the PUR3 register is 1 (P11 to P14 enabled). Access to registers PD11 to PD14 after setting the PU37 bit to 1. When the PU37 bit in the PUR3 register is 0 (P11 to P14 disabled), the contents of registers PD11 to PD14 are retained. In this case, read as undefined value.

13.3.8 NMI/SD Digital Filter Register (NMIDF)

$\overline{NMI}/\overline{SD}$ Digital Filter Register



Symbol	Address	After Reset
NMIDF	0369h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
NMIDF0	$\overline{NMI}/\overline{SD}$ filter sampling clock select bit	b2 b1 b0 0 0 0 : No filter 0 0 1 : CPU clock divided by 2 0 1 0 : CPU clock divided by 4 0 1 1 : CPU clock divided by 8 1 0 0 : CPU clock divided by 16 1 0 1 : CPU clock divided by 32 1 1 0 : CPU clock divided by 64 1 1 1 : CPU clock divided by 128	RW
NMIDF1			RW
NMIDF2			RW
— (b7-b3)	No register bits. If necessary, set to 0. Read as undefined value		—

13.4 Peripheral Function I/O

13.4.1 Peripheral Function I/O and Port Direction Bits

Programmable I/O ports can share pins with peripheral function I/O. (See to Table 1.11 to Table 1.12 “Pin Names, Pin Package”.) Some peripheral function I/O are affected by a port direction bit which shares the same pin. Table 13.4 lists The Setting of Direction Bits Functioning as Peripheral Function I/O. For peripheral function settings, see descriptions of each function.

Table 13.4 The Setting of Direction Bits Functioning as Peripheral Function I/O

Peripheral Function I/O		The Setting of the Port Direction Bit Sharing the Same Pin
Input		Set to 0 (input mode).
Output	PWM	Set to 1 (output mode).
	D/A converter	Set to 0 (input mode).
	Others	Set to either 0 or 1. (Outputs regardless of the direction bit setting)

13.4.2 Priority Level of Peripheral Function I/O

Multiple peripheral functions can share the same pin.
For example, when peripheral function A and peripheral function B share a pin, input and output are as follows:

- When the pin functions as input for peripheral functions A and B
  The same signal is input as each input signal. However, the timing of accepting the signal differs depending on conditions (e.g. internal delay) of functions A and B.
- When the pin functions as output for peripheral function A and as input for peripheral function B
  Peripheral function A outputs a signal from the pin, and peripheral function B inputs the signal.
- When the pin functions as output for peripheral functions A and B
  Peripheral function with higher priority is output. Table 13.5 lists Priority Level of Peripheral Function Output.

Table 13.5 Priority Level of Peripheral Function Output

Priority Level	Function	Output Pin
High ↑	Multi-master I^2C-bus interface	SCLMM, SDAMM
	PWM	PWM0, PWM1
	Serial interface UART0 to UART2, UART5 to UART7, SI/O3, SI/O4	$\overline{RTS}$i, CLKi, TXDi, SCLi, SDAi (i = 0 to 2, 5 to 7), CLK3, SOUT3, CLK4, SOUT4
	CEC	CEC
	Timer timer A, three-phase control timer function	TA0OUT, TA1OUT, TA2OUT, TA3OUT, TA4OUT U, V, W, $\overline{U}$, $\overline{V}$, $\overline{W}$
↓ Low	Real-time clock	RTCOUT
	D/A converter	DA0, DA1

13.4.3 $\overline{\text{NMI}}/\overline{\text{SD}}$ Digital Filter

The $\overline{\text{NMI}}/\overline{\text{SD}}$ input circuit includes a digital filter. Sampling clock can be selected by bits NMIDF2 to NMIDF0 in the NMIDF register. The $\overline{\text{NMI}}$ level is sampled for every sampling clock. When the same sampled level is detected three times in a row, the level is transferred to the internal circuit.
When using the $\overline{\text{NMI}}/\overline{\text{SD}}$ digital filter, do not enter wait mode or stop mode.
Port P8_5 is not affected by the digital filter.
When using the CEC function, set bits NMIDF2 to NMIDF0 to 000b ($\overline{\text{NMI}}/\overline{\text{SD}}$ digital filter disabled).
Figure 13.11 shows $\overline{\text{NMI}}/\overline{\text{SD}}$ Digital Filter, and Figure 13.12 shows $\overline{\text{NMI}}/\overline{\text{SD}}$ Digital Filter Operation Example.

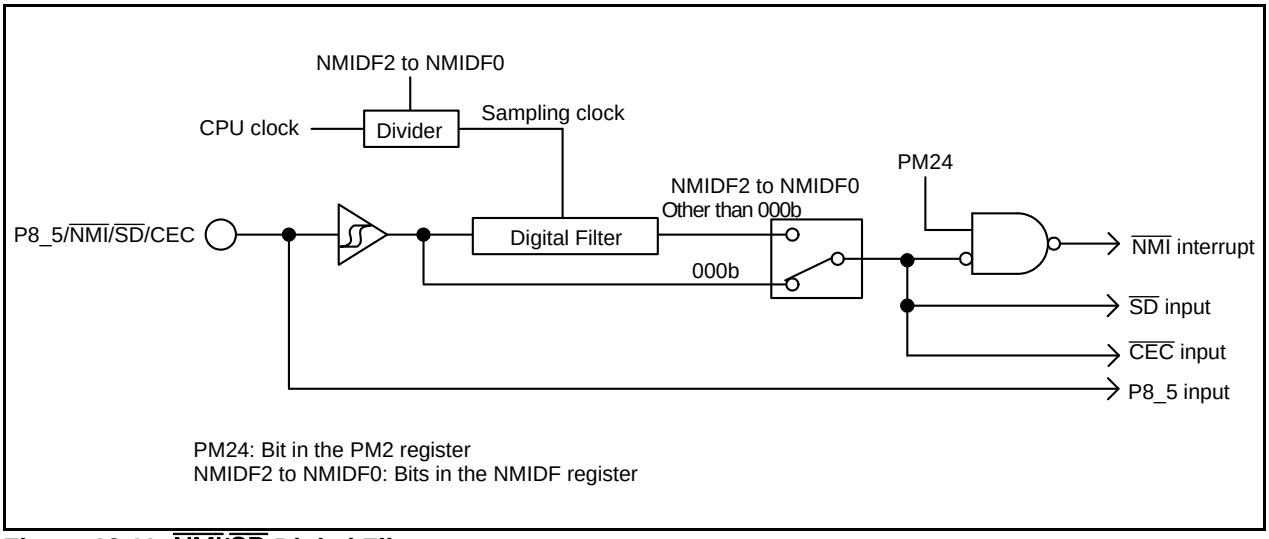


Figure 13.11 $\overline{\text{NMI}}/\overline{\text{SD}}$ Digital Filter

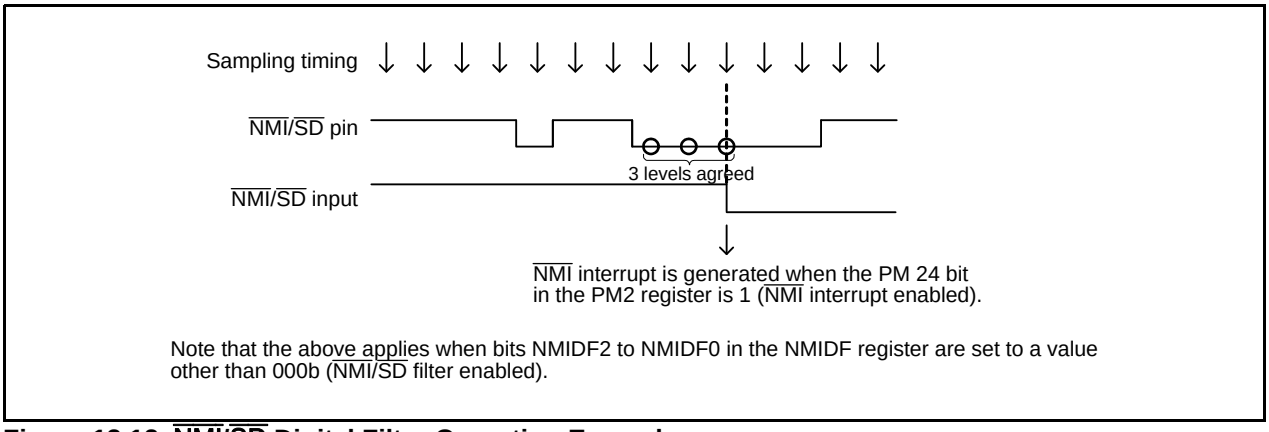


Figure 13.12 $\overline{\text{NMI}}/\overline{\text{SD}}$ Digital Filter Operation Example

13.4.4 CNVSS

The built-in pull-up resistor of the CNVSS pin is activated after watchdog timer reset, hardware reset, power-on reset or voltage monitor 0 reset. Thus, the CNVSS pin outputs a high-level signal up to two cycles of the fOCO-S. Connect the CNVSS pin to VSS via a resistor to use it in single-chip mode.

13.5 Unassigned Pin Handling

Table 13.6 Unassigned Pin Handling in Single-Chip Mode

Pin Name	Connection (2)
Ports P0 to P5, P12, P13	One of the following: • Set to input mode and connect a pin to VSS via a resistor (pull-down) • Set to input mode and connect a pin to VCC2 via a resistor (pull-up) (5) • Set to output mode and leave the pins open (1)
Ports P6 to P11, P14	One of the following: • Set to input mode and connect a pin to VSS via a resistor (pull-down) • Set to input mode and connect a pin to VCC1 via a resistor (pull-up) • Set to output mode and leave the pins open (1), (3)
XOUT (4)	Open
XIN	Connect to VCC1 via a resistor (pull-up)
AVCC	Connect to VCC1
AVSS, VREF, BYTE	Connect to VSS

Notes:
1. When setting a port to output mode and leaving it open, be aware that the port remains in input mode until it is switched to output mode by a program after reset. For this reason, the voltage level on the pin becomes undefined, causing the power supply current to increase while the port remains in input mode.
   Furthermore, since the contents of the direction registers could be changed by noise or noise-induced loss of control, it is recommended that the contents of the direction registers be regularly reset in software to improve the reliability of the program.
2. Make sure the unassigned pins are connected with the shortest possible wiring from the MCU pins (maximum 2 cm).
3. Ports P7_0, P7_1 and P8_5 are N-channel open-drain outputs.
   When ports P7_0, P7_1 and P8_5 are set to output mode, make sure a low-level signal is output from the pins.
4. This applies when an external clock is input to the XIN pin or when VCC1 is connected via a resistor.
5. In 80-package, a port is set to input mode and is connected to VCC1 via a resistor (pull-up).

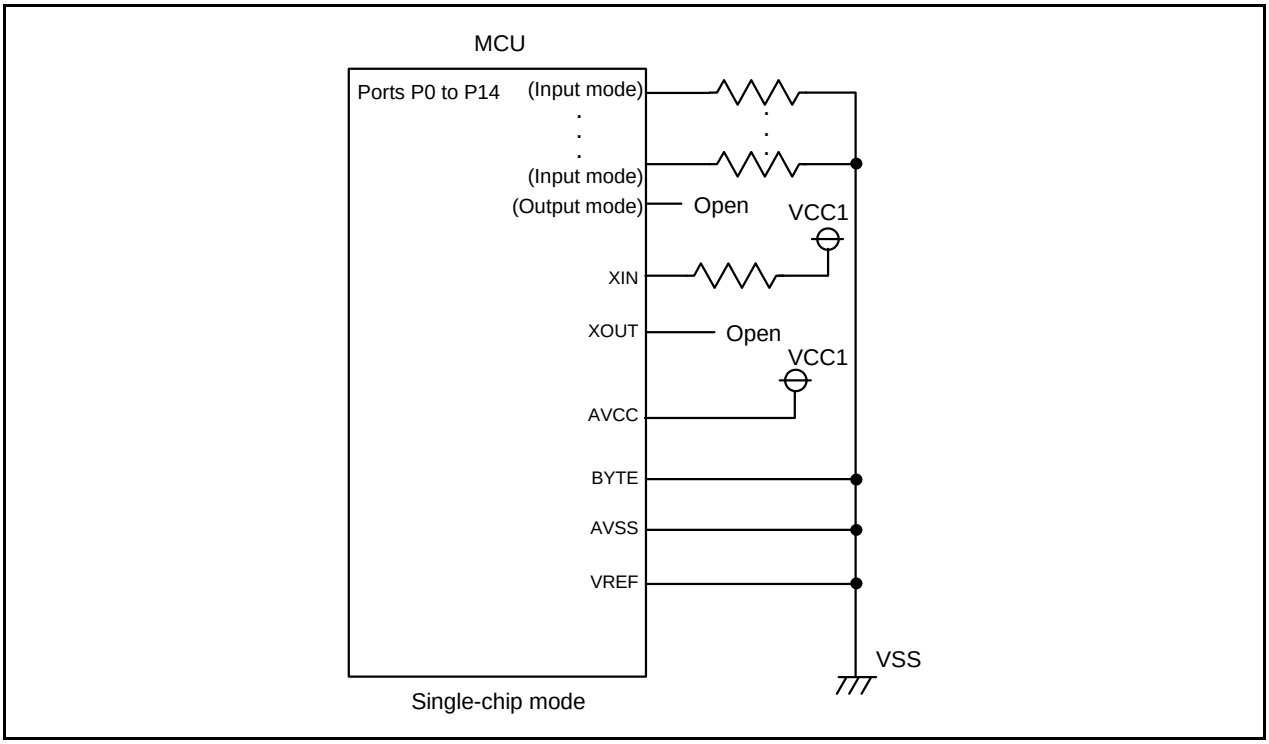


Figure 13.13 Unassigned Pin Handling in Single-Chip Mode

Table 13.7 Unassigned Pin Handling in Memory Expansion Mode and Microprocessor Mode

Pin Name	Connection (2)
Ports P0 to P5, P12, P13	One of the following: • Set to input mode and connect a pin to VSS via a resistor (pull-down) • Set to input mode and connect a pin to VCC2 via a resistor (pull-up) • Set to output mode and leave the pins open (1), (3)
Ports P6 to P11, P14	One of the following: • Set to input mode and connect a pin to VSS via a resistor (pull-down) • Set to input mode and connect a pin to VCC1 via a resistor (pull-up) • Set to output mode and leave the pins open (1), (4)
$\overline{BHE}$, ALE, $\overline{HLDA}$, XOUT (5), BCLK (6)	Open
$\overline{HOLD}$, $\overline{RDY}$	Connect to VCC2 via a resistor (pull-up)
XIN	Connect to VCC1 via a resistor (pull-up)
AVCC	Connect to VCC1
AVSS, VREF	Connect to VSS

Notes:
1. When setting a port to output mode and leaving it open, be aware that the port remains in input mode until it is switched to output mode by a program after reset. For this reason, the voltage level on the pin becomes undefined, causing the power supply current to increase while the port remains in input mode.
   Furthermore, since the contents of the direction registers could be changed by noise or noise-induced loss of control, it is recommended that the contents of the direction registers be regularly reset in software to improve the reliability of the program.
2. Make sure the unassigned pins are connected with the shortest possible wiring from the MCU pins (maximum 2 cm).
3. If the CNVSS pin has the VSS level applied to it, these pins are set as input ports until the processor mode is switched by a program after reset. For this reason, the voltage levels on these pins become undefined, causing the power supply current to increase while they remain set as input ports.
4. Ports P7_0, P7_1, and P8_5 are N-channel open-drain outputs.
   When ports P7_0, P7_1, and P8_5 are set to output mode, make sure a low-level signal is output from the pins.
5. This applies when an external clock is input to the XIN pin or when VCC1 is connected via a resistor.
6. If the PM07 bit in the PM0 register is set to 1 (BCLK not output), connect this pin to VCC2 via a resistor (pulled high).

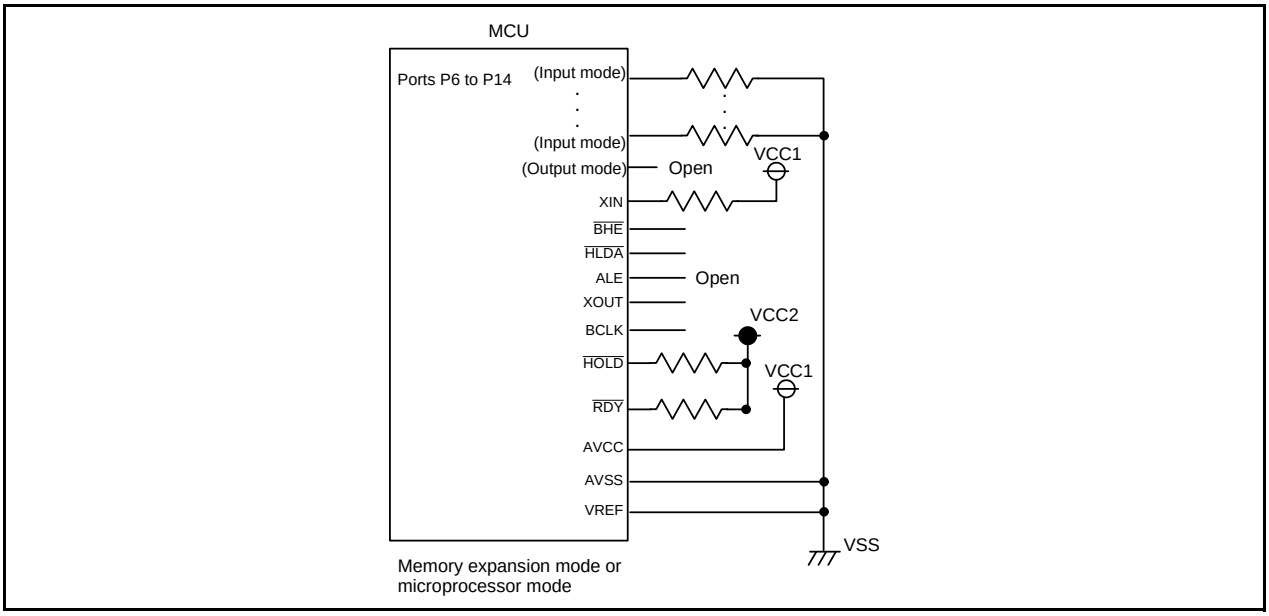


Figure 13.14 Unassigned Pin Handling in Memory Expansion Mode and Microprocessor Mode

13.6 Notes on Programmable I/O Ports

13.6.1 Influence of the $\overline{SD}$ Input

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins P7_2 to P7_5 and P8_0 and P8_1 go to the high-impedance state.

13.6.2 Influence of SI/O3 and SI/O4

Setting the SM32 bit in the S3C register to 1 causes the P9_2 pin to go to the high-impedance state. Similarly, setting the SM42 bit in the S4C register to 1 causes the P9_6 pin to go to the high-impedance state.

13.6.3 100-Pin Package

Do not access to the addresses assigned to registers P11 to P14 and the PUR register.

13.6.4 80-Pin Package

Do not access to the addresses assigned to registers P11 to P14 and the PUR register.
Set the direction bits of the ports corresponding to P1, P4_4 to P4_7, P7_2 to P7_5 and P9_1 to 1 (output mode). Set the output data to 0 (low-level signal).

14. Interrupts

Note

Do not use $\overline{INT3}$ to $\overline{INT5}$ for the 80-pin package.

14.1 Introduction

Table 14.1 lists Types of Interrupt, and Table 14.2 lists I/O Pins. The pins shown in Table 14.2 are external interrupt input pins. Refer to the peripheral functions for the pins related to the peripheral functions.

Table 14.1 Types of Interrupt

Type		Interrupt	Function
Software		Undefined instruction (UND instruction) Overflow (INTO instruction) BRK instruction INT instruction	An interrupt is generated by executing an instruction. Non-maskable interrupt (2)
Hardware	Specific	$\overline{NMI}$ Watchdog timer Oscillation stop and re-oscillation detection Voltage monitor 1 Voltage monitor 2 Address match Single step (1) $\overline{DBC}$ (1)	Interrupt by the MCU hardware Non-maskable interrupt (2)
	Peripheral function	$\overline{INT}$, timers, etc. (See 14.6.2 “Relocatable Vector Tables”.)	Interrupt by the peripheral functions in the MCU Maskable interrupt (interrupt priority level: 7 levels) (2)

Notes:
1. This interrupt is provided exclusively for developers and should not be used.
2. Maskable interrupt: Interrupt status (enabled or disabled) can be selected by the interrupt enable flag (I flag).
   Interrupt priority can be changed by the interrupt priority level.
   Non-maskable interrupt: Interrupt status (enabled or disabled) cannot be selected by the interrupt enable flag (I flag).
   Interrupt priority cannot be changed by the interrupt priority level.

Table 14.2 I/O Pins

Pin Name	I/O Type	Function
$\overline{NMI}$	I	$\overline{NMI}$ interrupt input
$\overline{INTi}$	I (1)	$\overline{INTi}$ interrupt input
$\overline{KI0}$ to $\overline{KI3}$	I (1)	Key input

i = 0 to 7

Note:
1. Set the port direction bits which share pins to 0 (input mode).

14.2 Registers

Table 14.3 Register Structure (1/2)

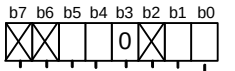
Address	Register Name	Register Symbol	After Reset
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
0042h	$\overline{\text{INT7}}$ Interrupt Control Register	INT7IC	XX00 X000b
0043h	$\overline{\text{INT6}}$ Interrupt Control Register	INT6IC	XX00 X000b
0044h	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register UART1 Bus Collision Detection Interrupt Control Register	TB4IC, U1BCNIC	XXXX X000b
0047h	Timer B3 Interrupt Control Register, UART0 Bus Collision Detection Interrupt Control Register	TB3IC, U0BCNIC	XXXX X000b
0048h	SI/O4 Interrupt Control Register, $\overline{\text{INT5}}$ Interrupt Control Register	S4IC, INT5IC	XX00 X000b
0049h	SI/O3 Interrupt Control Register, $\overline{\text{INT4}}$ Interrupt Control Register	S3IC, INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register CEC1 Interrupt Control Register	U5BCNIC, CEC1IC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register CEC2 Interrupt Control Register	S5TIC, CEC2IC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b

Table 14.4 Register Structure (2/2)

Address	Register Name	Register Symbol	After Reset
006Eh	UART6 Bus Collision Detection Interrupt Control Register, Real-Time Clock Period Interrupt Control Register	U6BCNIC, RTCTIC	XXXX X000b
006Fh	UART6 Transmit Interrupt Control Register, Real-Time Clock Compare Match Interrupt Control Register	S6TIC, RTCCIC	XXXX X000b
0070h	UART6 Receive Interrupt Control Register	S6RIC	XXXX X000b
0071h	UART7 Bus Collision Detection Interrupt Control Register, Remote Control Signal Receiver 0 Interrupt Control Register	U7BCNIC, PMC0IC	XXXX X000b
0072h	UART7 Transmit Interrupt Control Register, Remote Control Signal Receiver 1 Interrupt Control Register	S7TIC, PMC1IC	XXXX X000b
0073h	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
007Bh	IICBus Interface Interrupt Control Register	IICIC	XXXX X000b
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	XXXX X000b
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b
0210h 0211h 0212h	Address Match Interrupt Register 0	RMAD0	00h 00h X0h
0214h 0215h 0216h	Address Match Interrupt Register 1	RMAD1	00h 00h X0h
0218h 0219h 021Ah	Address Match Interrupt Register 2	RMAD2	00h 00h X0h
021Ch 021Dh 021Eh	Address Match Interrupt Register 3	RMAD3	00h 00h X0h
0366h	Port Control Register	PCR	0000 0XX0b
0369h	NMI/SD Digital Filter Register	NMIDF	XXXX X000b

14.2.1 Processor Mode Register 2 (PM2)

Processor Mode Register 2



Symbol	Address	After Reset
PM2	001Eh	XX00 0X01b

Bit Symbol	Bit Name	Function	RW
PM20	Specifying wait when accessing SFR at PLL operation	0 : 2 waits 1 : 1 wait	RW
PM21	System clock protection bit	0 : Clock is protected by PRCR register 1 : Clock change disabled	RW
— (b2)	No register bit. If necessary, set to 0. Read as 0		—
— (b3)	Reserved bit	Set to 0	RW
PM24	$\overline{\text{NMI}}$ interrupt enable bit	0 : $\overline{\text{NMI}}$ interrupt disabled 1 : $\overline{\text{NMI}}$ interrupt enabled	RW
PM25	Peripheral clock fC provide bit	0 : Provided 1 : Not provide	RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as undefined value		—

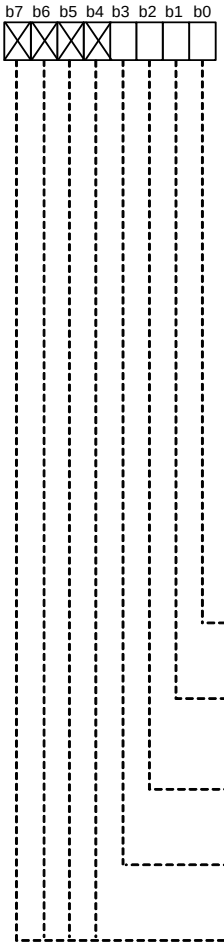
Set the PRC1 bit in the PRCR register to 1 (write enabled) before the PM2 register is rewritten.

PM24 ($\overline{\text{NMI}}$ Interrupt Enable Bit) (b4)

Once this bit is set to 1, it cannot be set to 0 by a program (writing a 0 has no effect).

14.2.2 Interrupt Control Register 1 (TB5IC, TB4IC/U1BCNIC, TB3IC/U0BCNIC, BCNIC, DM0IC to DM3IC, KUPIC, ADIC, S0TIC to S2TIC, S0RIC to S2RIC, TA0IC to TA4IC, TB0IC to TB2IC, U5BCNIC/CEC1IC, S5TIC/CEC2IC, S5RIC to S7RIC, U6BCNIC/RTCTIC, S6TIC/RTCCIC, U7BCNIC/PMC0IC, S7TIC/PMC1IC, IICIC, SCLDAIC)

Interrupt Control Register 1



Symbol	Address	After Reset
TB5IC	0045h	XXXX X000b
TB4IC/U1BCNIC	0046h	XXXX X000b
TB3IC/U0BCNIC	0047h	XXXX X000b
BCNIC	004Ah	XXXX X000b
DM0IC to DM3IC	004Bh, 004Ch, 0069h, 006Ah	XXXX X000b
KUPIC	004Dh	XXXX X000b
ADIC	004Eh	XXXX X000b
S0TIC to S2TIC	0051h, 0053h, 004Fh	XXXX X000b
S0RIC to S2RIC	0052h, 0054h, 0050h	XXXX X000b
TA0IC to TA4IC	0055h to 0059h	XXXX X000b
TB0IC to TB2IC	005Ah to 005Ch	XXXX X000b
U5BCNIC/CEC1IC	006Bh	XXXX X000b
S5TIC/CEC2IC	006Ch	XXXX X000b
S5RIC to S7RIC	006Dh, 0070h, 0073h	XXXX X000b
U6BCNIC/RTCTIC	006Eh	XXXX X000b
S6TIC/RTCCIC	006Fh	XXXX X000b
U7BCNIC/PMC0IC	0071h	XXXX X000b
S7TIC/PMC1IC	0072h	XXXX X000b
IICIC	007Bh	XXXX X000b
SCLDAIC	007Ch	XXXX X000b

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0: Interrupt not requested 1: Interrupt requested	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value		—

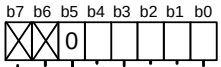
Rewrite this register at a point that does not generate an interrupt request.
When multiple interrupt sources share the register, select an interrupt source in registers IFSR2A and IFSR3A.

IR (Interrupt Request Bit) (b3)

The IR bit can only be set to 0 (do not write 1).

14.2.3 Interrupt Control Register 2 (INT7IC, INT6IC, INT3IC, S4IC/INT5IC, S3IC/INT4IC, INT0IC to INT2IC)

Interrupt Control Register 2



Symbol	Address	After Reset
INT7IC	0042h	XX00 X000b
INT6IC	0043h	XX00 X000b
INT3IC	0044h	XX00 X000b
S4IC/INT5IC	0048h	XX00 X000b
S3IC/INT4IC	0049h	XX00 X000b
INT0IC to INT2IC	005Dh to 005Fh	XX00 X000b

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0: Interrupt not requested 1: Interrupt requested	RW (1)
POL	Polarity select bit	0 : Select falling edge 1 : Select rising edge	RW
— (b5)	Reserved bit	Set to 0	RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as undefined value		—

Rewrite this register at a point that does not generate an interrupt request.
When multiple interrupt sources share the register, select an interrupt source in the IFSR register.

ILVL2-ILVL0 (Interrupt Priority Level Select Bit) (b2-b0)

In memory expansion or microprocessor mode, set bits ILVL2 to ILVL0 in registers INT6IC and INT7IC to 000b (interrupts disabled).
When the BYTE pin is low in memory expansion or microprocessor mode, set bits ILVL2 to ILVL0 in registers INT3IC, INT4IC, and INT5IC to 000b (interrupts disabled).

IR (Interrupt Request Bit) (b3)

The IR bit can only be set to 0 (do not write 1).

POL (Polarity Select Bit) (b4)

When the IFSRi bit in the IFSR register is 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge) (i = 0 to 5). Similarly, when bits IFSR30 and IFSR31 in the IFSR3A register are 1 (both edges), set the POL bit in registers INT6IC and INT7IC to 0 (falling edge).
Set the POL bit in the S3IC or S4IC register to 0 (falling edge) when the IFSR6 bit in the IFSR register is 0 (SI/O3 selected) or IFSR7 bit is 0 (SI/O4 selected), respectively.

14.2.4 Interrupt Source Select Register 3 (IFSR3A)

Interrupt Source Select Register 3

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
0			0	0	0			IFSR3A	0205h	00h

Bit Symbol	Bit Name	Function	RW
IFSR30	INT6 interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR31	INT7 interrupt polarity select bit	0 : One edge 1 : Both edges	RW
— (b2)	Reserved bit	Set to 0	RW
IFSR33	Interrupt request source select bit	0 : UART5 start/stop condition detection, bus collision detection 1 : CEC1	RW
IFSR34	Interrupt request source select bit	0 : UART5 transmission, NACK 1 : CEC2	RW
IFSR35	Interrupt request source select bit	0 : UART6 start/stop condition detection, bus collision detection 1 : Real-time clock cycle	RW
IFSR36	Interrupt request source select bit	0 : UART6 transmission, NACK 1 : Real-time clock compare match	RW
— (b7)	Reserved bit	Set to 0	RW

IFSR30 (INT6 Interrupt Polarity Select Bit) (b0)

When setting this bit to 1 (both edges), make sure the POL bit in the INT6IC register is set to 0 (falling edge).

IFSR31 (INT7 Interrupt Polarity Select Bit) (b1)

When setting this bit to 1 (both edges), make sure the POL bit in the INT7IC register is set to 0 (falling edge).

14.2.5 Interrupt Source Select Register 2 (IFSR2A)

Interrupt Source Select Register 2

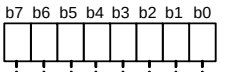
b7	b6	b5	b4	b3	b2	b1	b0
						0	0

Symbol	Address	After Reset
IFSR2A	0206h	00h

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
IFSR22	Interrupt request source select bit	0 : Not used 1 : I^2C bus interface	RW
IFSR23	Interrupt request source select bit	0 : Not used 1 : SCL/SDA	RW
IFSR24	Interrupt request source select bit	0 : UART7 start/stop condition detection, bus collision detection 1 : Remote control 0	RW
IFSR25	Interrupt request source select bit	0 : UART7 transmission, NACK 1 : Remote control 1	RW
IFSR26	Interrupt request source select bit	0 : Timer B3 1 : UART0 start/stop condition detection, bus collision detection	RW
IFSR27	Interrupt request source select bit	0 : Timer B4 1 : UART1 start/stop condition detection, bus collision detection	RW

14.2.6 Interrupt Source Select Register (IFSR)

Interrupt Source Select Register



Symbol	Address	After Reset
IFSR	0207h	00h

Bit Symbol	Bit Name	Function	RW
IFSR0	$\overline{INT0}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR1	$\overline{INT1}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR2	$\overline{INT2}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR3	$\overline{INT3}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR4	$\overline{INT4}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR5	$\overline{INT5}$ interrupt polarity select bit	0 : One edge 1 : Both edges	RW
IFSR6	Interrupt request source select bit	0 : SI/O3 1 : $\overline{INT4}$	RW
IFSR7	Interrupt request source select bit	0 : SI/O4 1 : $\overline{INT5}$	RW

IFSR5-IFSR0 ($\overline{INT5}$-$\overline{INT0}$ Interrupt Polarity Select Bit) (b5-b0)

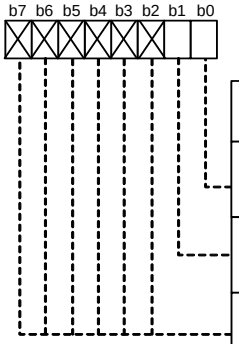
When setting this bit to 1 (both edges), make sure the POL bit in registers INT0IC to INT5IC are set to 0 (falling edge).

IFSR7, IFSR6 (Interrupt Request Source Select Bit) (b7, b6)

In memory expansion or microprocessor mode, when the data bus is 16 bits wide (BYTE pin is low), set this bit to 0 (SI/O3, SI/O4).
When setting this bit to 0 (SI/O3, SI/O4), make sure the POL bit in registers S3IC and S4IC are set to 0 (falling edge).

14.2.7 Address Match Interrupt Enable Register (AIER)

Address Match Interrupt Enable Register

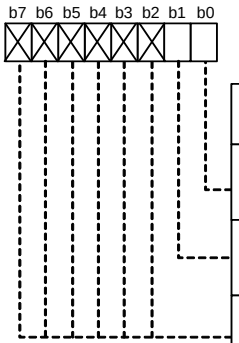


Symbol	Address	After Reset
AIER	020Eh	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
AIER0	Address match interrupt 0 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
AIER1	Address match interrupt 1 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
— (b7-b2)	No register bits. If necessary, set to 0. Read as undefined value		—

14.2.8 Address Match Interrupt Enable Register 2 (AIER2)

Address Match Interrupt Enable Register 2

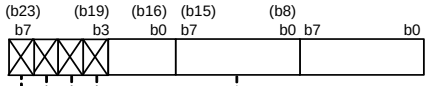


Symbol	Address	After Reset
AIER2	020Fh	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
AIER20	Address match interrupt 2 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
AIER21	Address match interrupt 3 enable bit	0 : Interrupt disabled 1 : Interrupt enabled	RW
— (b7-b2)	No register bits. If necessary, set to 0. Read as undefined value		—

14.2.9 Address Match Interrupt Register i (RMADi) (i = 0 to 3)

Address Match Interrupt Register i (i = 0 to 3)

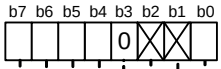


Symbol	Address	After Reset
RMAD0	0212h to 0210h	X0 0000h
RMAD1	0216h to 0214h	X0 0000h
RMAD2	021Ah to 0218h	X0 0000h
RMAD3	021Eh to 021Ch	X0 0000h

Function	Setting Range	RW
Address setting register for address match interrupt (b19 to b0)	00000h to FFFFFh	RW
No register bits. If necessary, set to 0. Read as undefined value		—

14.2.10 Port Control Register (PCR)

Port Control Register



Symbol	Address	After Reset
PCR	0366h	0000 0XX0b

Bit Symbol	Bit Name	Function	RW
PCR0	Port P1 control bit	Operation performed when the P1 register is read 0 : When the port is set to input, the input levels of pins P1_0 to P1_7 are read. When set to output, the port latch is read. 1 : The port latch is read regardless of whether the port is set to input or output.	RW
— (b2-b1)	No register bits. If necessary, set to 0. Read as undefined		—
— (b3)	Reserved bit	Set to 0	RW
PCR4	CEC output enable bit	0 : CEC output disabled 1 : CEC output enabled	RW
PCR5	$\overline{INT6}$ input enable bit	0 : Enabled 1 : Disabled	RW
PCR6	$\overline{INT7}$ input enable bit	0 : Enabled 1 : Disabled	RW
PCR7	Key input enable bit	0 : Enabled 1 : Disabled	RW

$\overline{INT6}$ Input Enable Bit (PCR5) (b5)

To use the AN2_4 pin as an analog input pin, set the PCR5 bit to 1 ($\overline{INT6}$ input disabled).

$\overline{INT7}$ Input Enable Bit (PCR5) (b5)

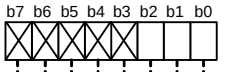
To use the AN2_5 pin as an analog input pin, set the PCR6 bit to 1 ($\overline{INT7}$ input disabled).

Key Input Enable Bit(PCR7) (b7)

To use pins AN4 to AN7 as analog input pins, set the PCR7 bit to 1 (key input disabled).

14.2.11 NMI/SD Digital Filter Register (NMIDF)

$\overline{NMI}/\overline{SD}$ Digital Filter Register



Symbol	Address	After Reset
NMIDF	0369h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
NMIDF0	$\overline{NMI}/\overline{SD}$ filter sampling clock select bit	b2 b1 b0 0 0 0 : No filter 0 0 1 : CPU clock divided by 2 0 1 0 : CPU clock divided by 4 0 1 1 : CPU clock divided by 8 1 0 0 : CPU clock divided by 16 1 0 1 : CPU clock divided by 32 1 1 0 : CPU clock divided by 64 1 1 1 : CPU clock divided by 128	RW
NMIDF1			RW
NMIDF2			RW
— (b7-b3)	No register bits. If necessary, set to 0. Read as undefined value		—

14.3 Types of Interrupt

Figure 14.1 shows Types of Interrupt.

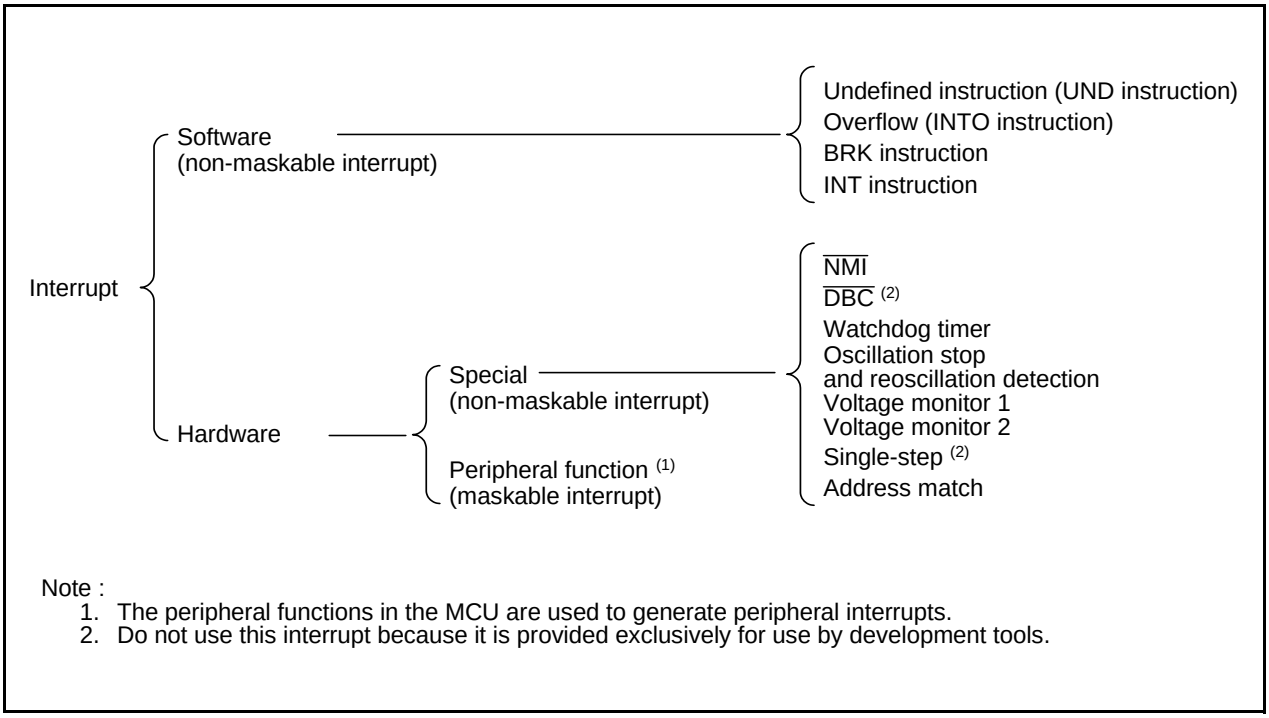


Figure 14.1 Types of Interrupt

- Maskable interrupt : The interrupt priority **can be changed** by enabling (disabling) an interrupt with the interrupt enable flag (I flag) or by using interrupt priority levels.
- Non-maskable interrupt : The interrupt priority **cannot be changed** by enabling (disabling) an interrupt with the interrupt enable flag (I flag) or by using interrupt priority levels.

14.4 Software Interrupts

A software interrupt occurs when executing instructions. Software interrupts are non-maskable interrupts.

14.4.1 Undefined Instruction Interrupt

An undefined instruction interrupt occurs when executing the UND instruction.

14.4.2 Overflow Interrupt

An overflow interrupt occurs when executing the INTO instruction with the O flag in the FLG register set to 1 (the operation resulted in an overflow). The following are instructions whose O flag changes by an arithmetic operation:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB

14.4.3 BRK Interrupt

A BRK interrupt occurs when the BRK instruction is executed.

14.4.4 INT Instruction Interrupt

An INT instruction interrupt occurs when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified for the INT instruction. Because software interrupt numbers 2 to 31, 41 to 51, 59, and 60 are assigned to peripheral function interrupts, the same interrupt routine used for peripheral function interrupts can be executed by executing the INT instruction.
For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and is cleared to 0 (ISP selected) before executing an interrupt sequence. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the SP selected at the time is used.

14.5 Hardware Interrupts

Hardware interrupts are classified into two types: special interrupts and peripheral function interrupts.

14.5.1 Special Interrupts

Special interrupts are non-maskable interrupts.

14.5.1.1 $\overline{\text{NMI}}$ Interrupt

An $\overline{\text{NMI}}$ interrupt is generated when input on the $\overline{\text{NMI}}$ pin changes state from high to low. For details about the $\overline{\text{NMI}}$ interrupt, refer to 14.9 “$\overline{\text{NMI}}$ Interrupt”.

14.5.1.2 $\overline{\text{DBC}}$ Interrupt

Do not use this interrupt because it is provided exclusively for use by development tools.

14.5.1.3 Watchdog Timer Interrupt

The interrupt is generated by the watchdog timer. Once a watchdog timer interrupt is generated, be sure to refresh the watchdog timer. For details about the watchdog timer, refer to 15. “Watchdog Timer”.

14.5.1.4 Oscillation Stop and Re-Oscillation Detection Interrupt

The interrupt is generated by the oscillation stop and re-oscillation detection function. For details about the oscillation stop and re-oscillation detection function, refer to 8. “Clock Generator”.

14.5.1.5 Voltage Monitor 1, Voltage Monitor 2

The interrupt is generated by the voltage detection circuit. For details about the voltage detection circuit, refer to 7. “Voltage Detector”.

14.5.1.6 Single-Step Interrupt

Do not use this interrupt because it is provided exclusively for use by development tools.

14.5.1.7 Address Match Interrupt

When the AIER0 or AIER1 bit in the AIER register, or the AIER20 or AIER21 bit in the AIER2 register is 1 (address match interrupt enabled), an address match interrupt is generated immediately before executing an instruction at the address indicated by the corresponding registers RMAD0 to RMAD3. For details about the address match interrupt, refer to 14.11 “Address Match Interrupt”.

14.5.2 Peripheral Function Interrupts

A peripheral function interrupt occurs when a request from a peripheral function in the MCU is acknowledged. Peripheral function interrupts are maskable interrupts. See Table 14.6 and Table 14.7 “Relocatable Vector Tables”. Refer to the descriptions of each function for details on how the corresponding peripheral function interrupt is generated.

14.6 Interrupts and Interrupt Vectors

One interrupt vector consists of 4 bytes. Set the start address of each interrupt routine in the respective interrupt vectors. When an interrupt request is accepted, the CPU branches to the address set in the corresponding interrupt vector. Figure 14.2 shows an Interrupt Vector.

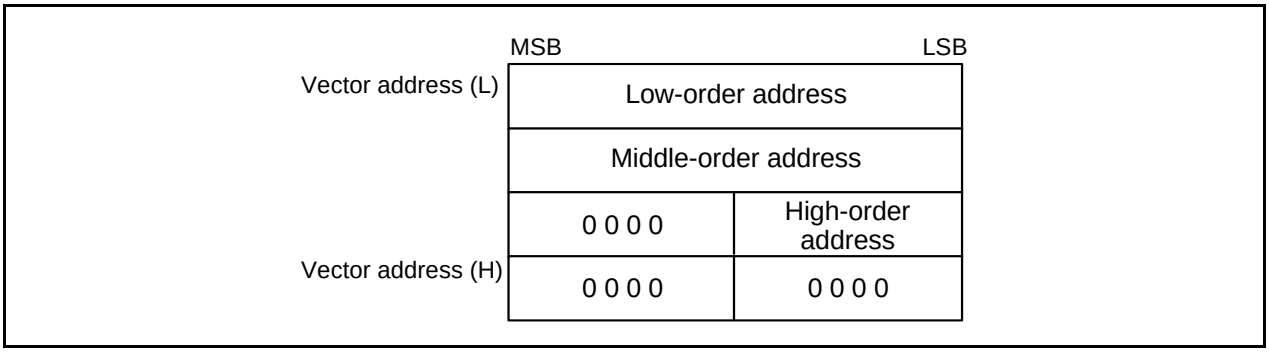


Figure 14.2 Interrupt Vector

14.6.1 Fixed Vector Tables

The fixed vector tables are allocated to addresses from FFFDCh to FFFFFh. Table 14.5 lists the Fixed Vector Tables. In the flash memory MCU version, the vector addresses (H) of fixed vectors are used for the ID code check function and OFS1 address. For details, refer to 30.5 “Flash Memory Rewrite Disable Function”.

Table 14.5 Fixed Vector Tables

Interrupt Source	Vector Table Addresses Address (L) to Address (H)	Reference
Undefined instruction (UND instruction)	FFFDCh to FFFDFh	M16C/60, M16C/20, M16C/ Tiny Series Software Manual
Overflow (INTO instruction)	FFFE0h to FFFE3h	
BRK instruction (2)	FFFE4h to FFFE7h	
Address match	FFFE8h to FFFEBh	14.11 “Address Match Interrupt”
Single-step (1)	FFFECh to FFFEFh	-
Watchdog timer, oscillation stop and re-oscillation detection, voltage monitor 1, voltage monitor 2	FFFF0h to FFFF3h	15. “Watchdog Timer” 8. “Clock Generator” 7. “Voltage Detector”
$\overline{\text{DBC}}$ (1)	FFFF4h to FFFF7h	-
$\overline{\text{NMI}}$	FFFF8h to FFFFBh	14.9 “$\overline{\text{NMI}}$ Interrupt”
Reset	FFFFCh to FFFFFh	6. “Resets”

Notes:
1. Do not use this interrupt because it is provided exclusively for use by development tools.
2. If the content of address FFFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.

14.6.2 Relocatable Vector Tables

The 256 bytes beginning with the start address set in the INTB register compose a relocatable vector table area. Table 14.6 and Table 14.7 list the Relocatable Vector Tables. Setting an even address in the INTB register results in the interrupt sequence being executed faster than setting an odd address.

Table 14.6 Relocatable Vector Tables (1/2)

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Reference
BRK instruction (5)	+0 to +3 (0000h to 0003h)	0	M16C/60, M16C/20, M16C/Tiny Series Software Manual
- (Reserved)		1	
$\overline{\text{INT7}}$	+8 to +11 (0008h to 000Bh)	2	14.8 "$\overline{\text{INT}}$ Interrupt"
$\overline{\text{INT6}}$	+12 to +15 (000Ch to 000Fh)	3	
$\overline{\text{INT3}}$	+16 to +19 (0010h to 0013h)	4	
Timer B5	+20 to +23 (0014h to 0017h)	5	18. "Timer B"
Timer B4, UART1 start/stop condition detection, bus collision detection (4)	+24 to +27 (0018h to 001Bh)	6	18. "Timer B"
Timer B3, UART0 start/stop condition detection, bus collision detection (4)	+28 to +31 (001Ch to 001Fh)	7	23. "Serial Interface UARTi (i = 0 to 2, 5 to 7)"
SI/O4, $\overline{\text{INT5}}$ (2)	+32 to +35 (0020h to 0023h)	8	14.8 "$\overline{\text{INT}}$ Interrupt"
SI/O3, $\overline{\text{INT4}}$ (2)	+36 to +39 (0024h to 0027h)	9	24. "Serial Interface SI/O3 and SI/O4"
UART2 start/stop condition detection, bus collision detection (4)	+40 to +43 (0028h to 002Bh)	10	23. "Serial Interface UARTi (i = 0 to 2, 5 to 7)"
DMA0	+44 to +47 (002Ch to 002Fh)	11	16. "DMAC"
DMA1	+48 to +51 (0030h to 0033h)	12	
Key input interrupt	+52 to +55 (0034h to 0037h)	13	14.10 "Key Input Interrupt"
A/D converter	+56 to +59 (0038h to 003Bh)	14	27. "A/D Converter"
UART2 transmit, NACK2 (3)	+60 to +63 (003Ch to 003Fh)	15	23. "Serial Interface UARTi (i = 0 to 2, 5 to 7)"
UART2 receive, ACK2 (3)	+64 to +67 (0040h to 0043h)	16	
UART0 transmit, NACK0 (3)	+68 to +71 (0044h to 0047h)	17	
UART0 receive, ACK0 (3)	+72 to +75 (0048h to 004Bh)	18	
UART1 transmit, NACK1 (3)	+76 to +79 (004Ch to 004Fh)	19	
UART1 receive, ACK1 (3)	+80 to +83 (0050h to 0053h)	20	
Timer A0	+84 to +87 (0054h to 0057h)	21	17. "Timer A"
Timer A1	+88 to +91 (0058h to 005Bh)	22	
Timer A2	+92 to +95 (005Ch to 005Fh)	23	
Timer A3	+96 to +99 (0060h to 0063h)	24	
Timer A4	+100 to +103 (0064h to 0067h)	25	
Timer B0	+104 to +107 (0068h to 006Bh)	26	18. "Timer B"
Timer B1	+108 to +111 (006Ch to 006Fh)	27	
Timer B2	+112 to +115 (0070h to 0073h)	28	

Notes:
1. Address relative to address in INTB.
2. Use bits IFSR6 and IFSR7 in the IFSR register to select a source.
3. In I^2C mode, NACK and ACK are interrupt sources.
4. Use bits IFSR26 and IFSR27 in the IFSR2A register to select a source.
5. These interrupts cannot be disabled using the I flag.

Table 14.7 Relocatable Vector Tables (2/2)

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Reference
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	14.8 "$\overline{\text{INT}}$ Interrupt"
$\overline{\text{INT1}}$	+120 to +123 (0078h to 007Bh)	30	
$\overline{\text{INT2}}$	+124 to +127 (007Ch to 007Fh)	31	
INT instruction interrupt (3)	+128 to +131 (0080h to 0083h) to +160 to +163 (00A0h to 00A3h)	32 to 40	M16C/60, M16C/20, M16C/Tiny Series Software Manuall
DMA2	+164 to +167 (00A4h to 00A7h)	41	16. "DMAC"
DMA3	+168 to +171 (00A8h to 00ABh)	42	
UART5 start/stop condition detection, bus collision detection, CEC1 (4)	+172 to +175 (00ACh to 0AFh)	43	23. "Serial Interface UARTi (i = 0 to 2, 5 to 7)" 26. "Consumer Electronics Control (CEC) Function"
UART5 transmit, NACK5, CEC2 (2), (4)	+176 to +179 (00B0h to 00B3h)	44	
UART5 receive, ACK5 (2)	+180 to +183 (00B4h to 00B7h)	45	
UART6 start/stop condition detection, bus collision detection, real-time clock cycle (5)	+184 to +187 (00B8h to 00BBh)	46	20. "Real-Time Clock" 23. "Serial Interface UARTi (i = 0 to 2, 5 to 7)"
UART6 transmit, NACK6, real-time clock compare match (2), (5)	+188 to +191 (00BCh to 00BFh)	47	
UART6 receive, ACK6 (2)	+192 to +195 (00C0h to 00C3h)	48	
UART7 start/stop condition detection, bus collision detection, remote control 0 (6)	+196 to +199 (00C4h to 00C7h)	49	22. "Remote Control Signal Receiver" 23. "Serial Interface UARTi (i = 0 to 2, 5 to 7)"
UART7 transmit, NACK7, remote control 1 (2), (6)	+200 to +203 (00C8h to 00CBh)	50	
UART7 receive, ACK7 (2)	+204 to +207 (00CCh to 00CFh)	51	
- (Reserved)		52 to 58	
I^2C-bus interface interrupt (7)	+236 to +239 (00ECh to 00EFh)	59	25. "Multi-Master I^2C-bus Interface"
SCL/SDA interrupt (7)	+240 to +243 (00F0h to 00F3h)	60	
- (Reserved)		61 to 63	

Notes:
1. Address relative to address in INTB.
2. In I^2C mode, NACK and ACK are the interrupt sources.
3. These interrupts cannot be disabled using the I flag.
4. Use bits IFSR33 and IFSR34 in the IFSR3 register to select a source.
5. Use bits IFSR35 and IFSR36 in the IFSR3 register to select a source.
6. Use bits IFSR24 and IFSR25 in the IFSR2 register to select a source.
7. Use bits IFSR22 and IFSR23 in the IFSR2 register to select a source.

14.7 Interrupt Control

14.7.1 Maskable Interrupt Control

The settings of enabling/disabling the maskable interrupts and of the acceptance priority are explained below. Note that these explanations do not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

14.7.1.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

14.7.1.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. Then, when the interrupt request is accepted, the IR bit is automatically set to 0 (interrupt not requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.

14.7.1.3 Bits ILVL2 to ILVL0 and IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 14.8 lists the Settings of Interrupt Priority Levels and Table 14.9 lists the Interrupt Priority Levels Enabled by IPL.

An interrupt request is accepted under the following conditions.

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0 and IPL are independent each other. In no case do they affect one another.

Table 14.8 Settings of Interrupt Priority Levels

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	-
001b	Level 1	Low
010b	Level 2	↓
011b	Level 3	↓
100b	Level 4	↓
101b	Level 5	↓
110b	Level 6	↓
111b	Level 7	High

Table 14.9 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Levels
000b	Level 1 and above are enabled
001b	Level 2 and above are enabled
010b	Level 3 and above are enabled
011b	Level 4 and above are enabled
100b	Level 5 and above are enabled
101b	Level 6 and above are enabled
110b	Level 7 and above are enabled
111b	All maskable interrupts are disabled

14.7.2 Interrupt Sequence

The interrupt sequence is explained here. The sequence starts when an interrupt request is accepted and ends when the interrupt routine is executed.
If an interrupt request occurs during execution of an instruction, the processor determines its priority after the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. However, if an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR, or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.
The CPU behavior during the interrupt sequence is described below. Figure 14.3 shows Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. Then, the IR bit applicable to the interrupt information is set to 0 (interrupt not requested).
(2) The FLG register, prior to the interrupt sequence, is saved to a temporary register (1) within the CPU.
(3) Flags I, D, and U in the FLG register are set as follows:
- The I flag is set to 0 (interrupt disabled)
- The D flag is set to 0 (single-step interrupt disabled).
- The U flag is set to 0 (ISP selected).
  Note that the U flag does not change states when an INT instruction for software interrupt numbers 32 to 63 is executed.

(4) The temporary register (1) within the CPU is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The start address of the relevant interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, an instruction is executed from the starting address of the interrupt routine.

Note:
1. Temporary registers cannot be modified by users.

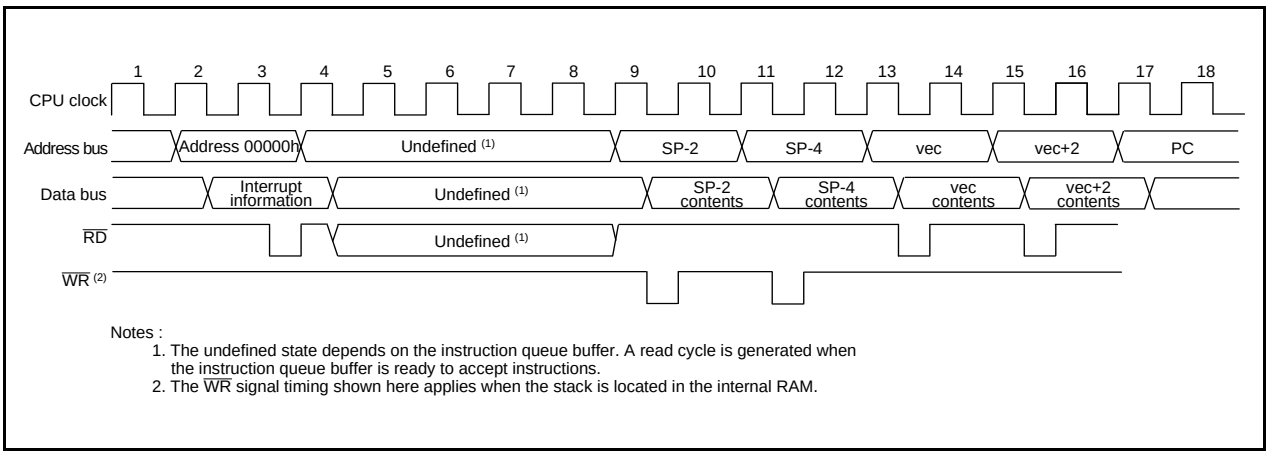
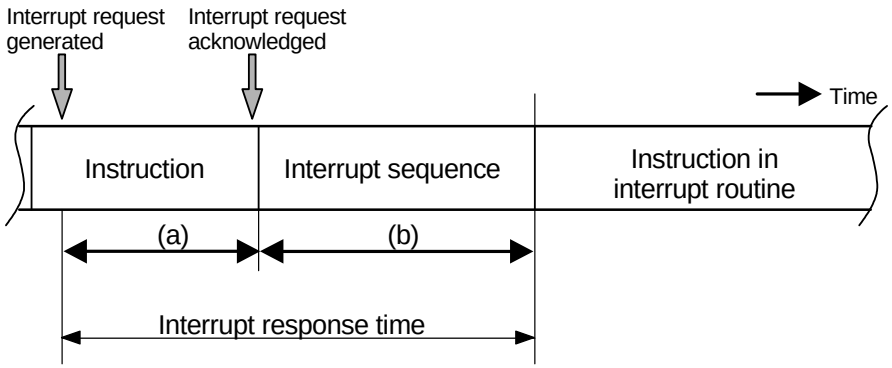


Figure 14.3 Time Required for Executing Interrupt Sequence

14.7.3 Interrupt Response Time

Figure 14.4 shows the Interrupt Response Time. The interrupt response or interrupt acknowledge time denotes the time from when an interrupt request is generated until the first instruction in the interrupt routine is executed. Specifically, it consists of the time from when an interrupt request is generated until the executing instruction is completed ((a) in Figure 14.4) and the time during which the interrupt sequence is executed ((b) in Figure 14.4).



(a) The time from when an interrupt request is generated until the instruction currently executing is completed. The length of this time varies with the instruction being executed. The DIVX instruction requires the longest time, which is equal to 30 cycles (no wait state, and when the divisor is a register).

(b) The time during which the interrupt sequence is executed. For details, see the table below. Note, however, that the values in this table must be increased by two cycles for the $\overline{\text{DBC}}$ interrupt and by one cycle for the address match and single-step interrupts.

Interrupt Vector Address	SP Value	16-Bit Bus, No Wait States	8-Bit Bus, No Wait States
Even	Even	18 cycles	20 cycles
Even	Odd	19 cycles	20 cycles
Odd	Even	19 cycles	20 cycles
Odd	Odd	20 cycles	20 cycles

Figure 14.4 Interrupt Response Time

14.7.4 Variation of IPL When Interrupt Request is Accepted

When a maskable interrupt request is accepted, the interrupt priority level of the accepted interrupt is set in the IPL.

When a software interrupt or special interrupt request is accepted, one of the interrupt priority levels listed in Table 14.10 is set in the IPL. Table 14.10 lists the IPL Level Set in IPL When Software or Special Interrupt is Accepted.

Table 14.10 IPL Level Set in IPL When Software or Special Interrupt is Accepted

Interrupt Source	Level Set in IPL
Watchdog timer, $\overline{\text{NMI}}$, oscillation stop and re-oscillation detection, voltage monitor1, voltage monitor 2	7
Software, address match, $\overline{\text{DBC}}$, single-step	Not changed

14.7.5 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
At this time, the 4 high-order bits of the PC and the 4 high-order (IPL) and 8 low-order bits in the FLG register, 16 bits in total, are saved on the stack first. Next, the 16 low-order bits of the PC are saved. Figure 14.5 shows the Stack Status Before and After Acceptance of Interrupt Request.
The other necessary registers must be saved by a program at the beginning of the interrupt routine. Use the PUSHM instruction, and all registers except SP can be saved with a single instruction.

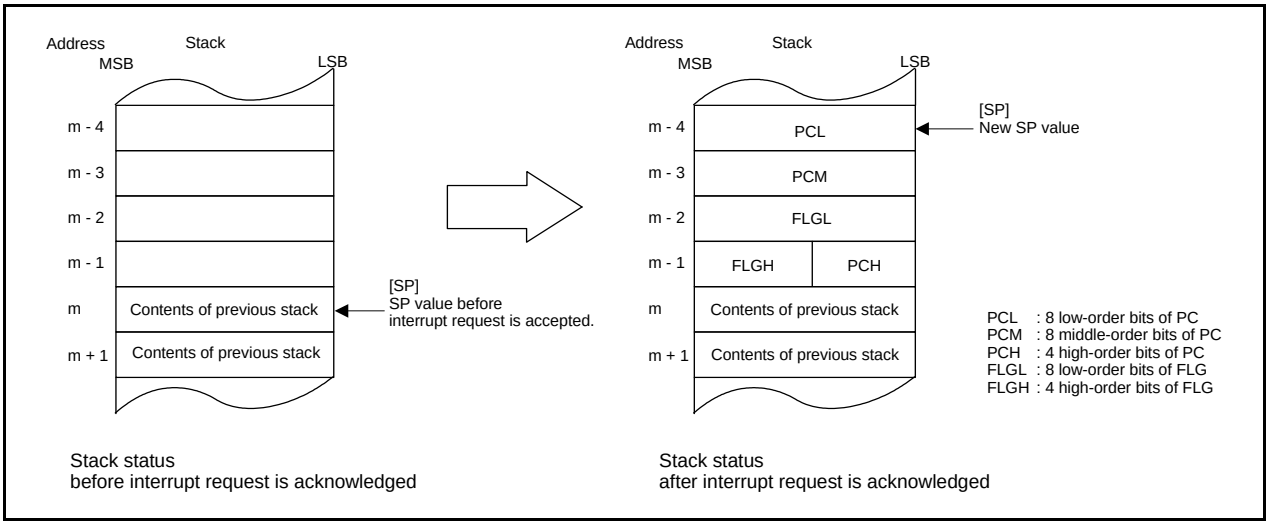


Figure 14.5 Stack Status Before and After Acceptance of Interrupt Request

The register save operation carried out in the interrupt sequence is dependent on whether the SP (1), at the time of acceptance of an interrupt request, is even or odd. If the SP (1) is even, the FLG register and the PC are saved 16 bits at a time. If odd, they are saved in two steps, 8 bits at a time. Figure 14.6 shows the Register Save Operation.

Note:
1. When an INT instruction with software numbers 32 to 63 has been executed, it is the SP indicated by the U flag. Otherwise, it is the ISP.

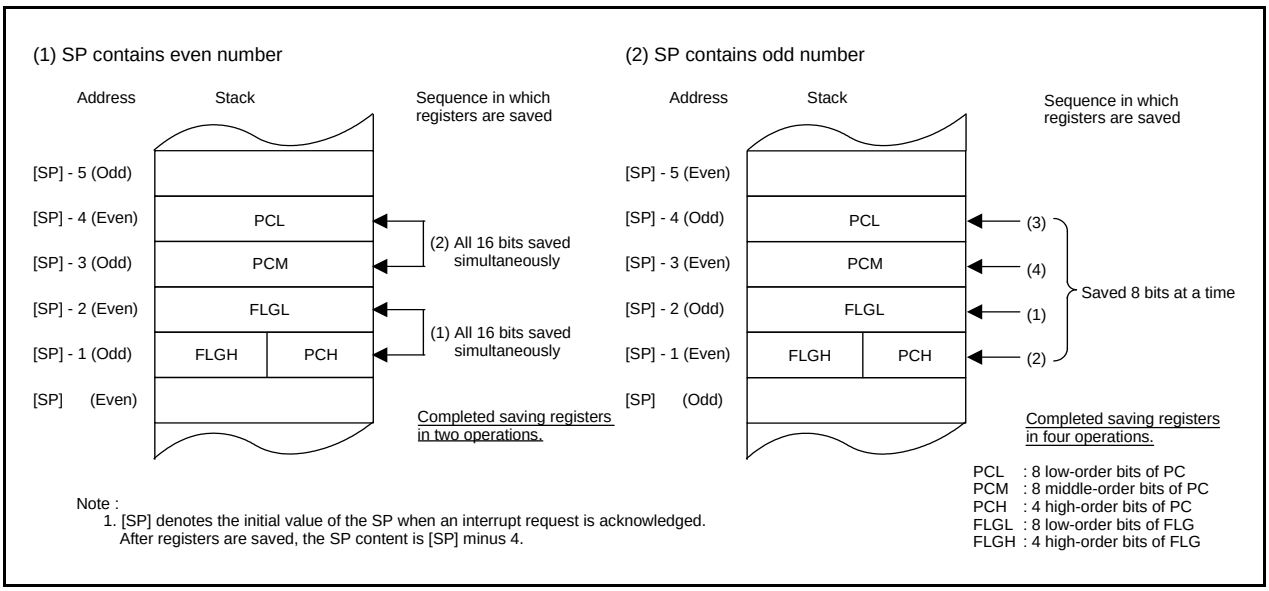


Figure 14.6 Register Save Operation

14.7.6 Returning from an Interrupt Routine

The FLG register and PC saved in the stack immediately before entering the interrupt sequence are restored from the stack by executing the REIT instruction at the end of the interrupt routine. Then, the CPU returns to the program which was being executed before the interrupt request was accepted.
Restore the other registers saved by a program within the interrupt routine using the POPM or another instruction before executing the REIT instruction.
The register bank is switched back to the bank used prior to the interrupt sequence by the REIT instruction.

14.7.7 Interrupt Priority

If two or more interrupt requests occur at the same sampling points (the point in time at which interrupt requests are detected), the interrupt with the highest priority is acknowledged.
For maskable interrupts (peripheral function interrupts), any priority level can be selected using bits ILVL2 to ILVL0. However, if two or more maskable interrupts have the same priority level, their interrupt priority is selected by hardware, with the highest priority interrupt accepted.
The watchdog timer interrupt and other special interrupts have their priority levels set in hardware. Figure 14.7 shows the Hardware Interrupt Priority.
Software interrupts are not affected by the interrupt priority. When an instruction is executed, control always branches to the interrupt routine.

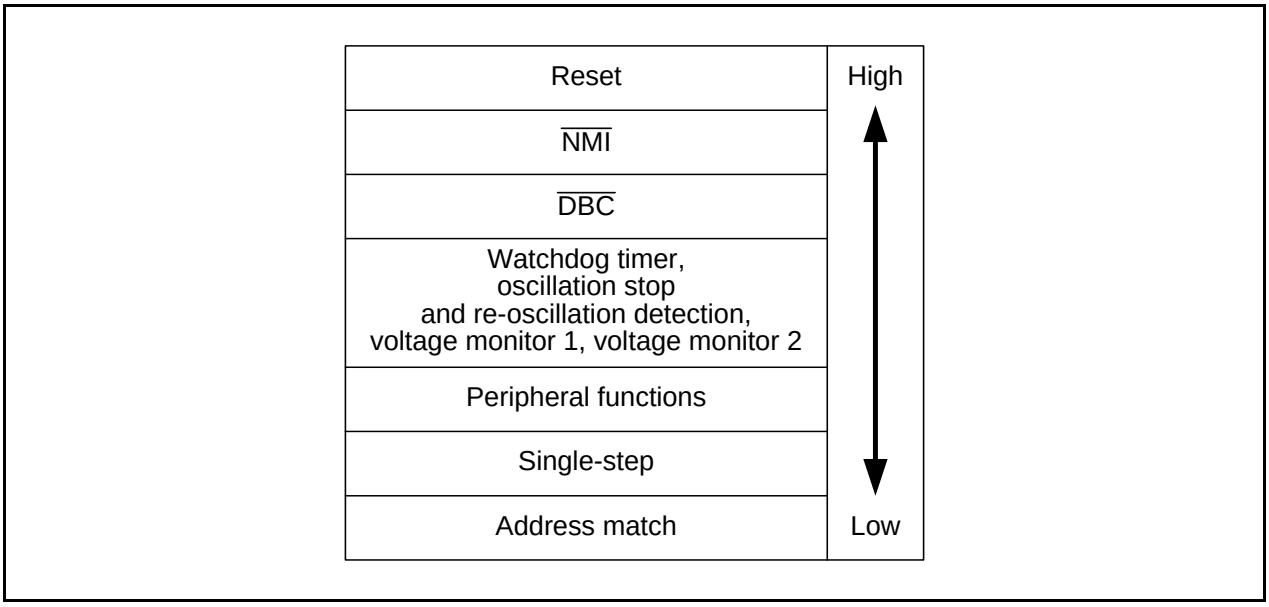


Figure 14.7 Hardware Interrupt Priority

14.7.8 Interrupt Priority Level Select Circuit

The interrupt priority level select circuit selects the highest priority interrupt among sampled interrupt requests at the same sampling point.
Figure 14.8 shows the Interrupt Priority Select Circuit 1, and Figure 14.9 shows the Interrupt Priority Select Circuit 2.

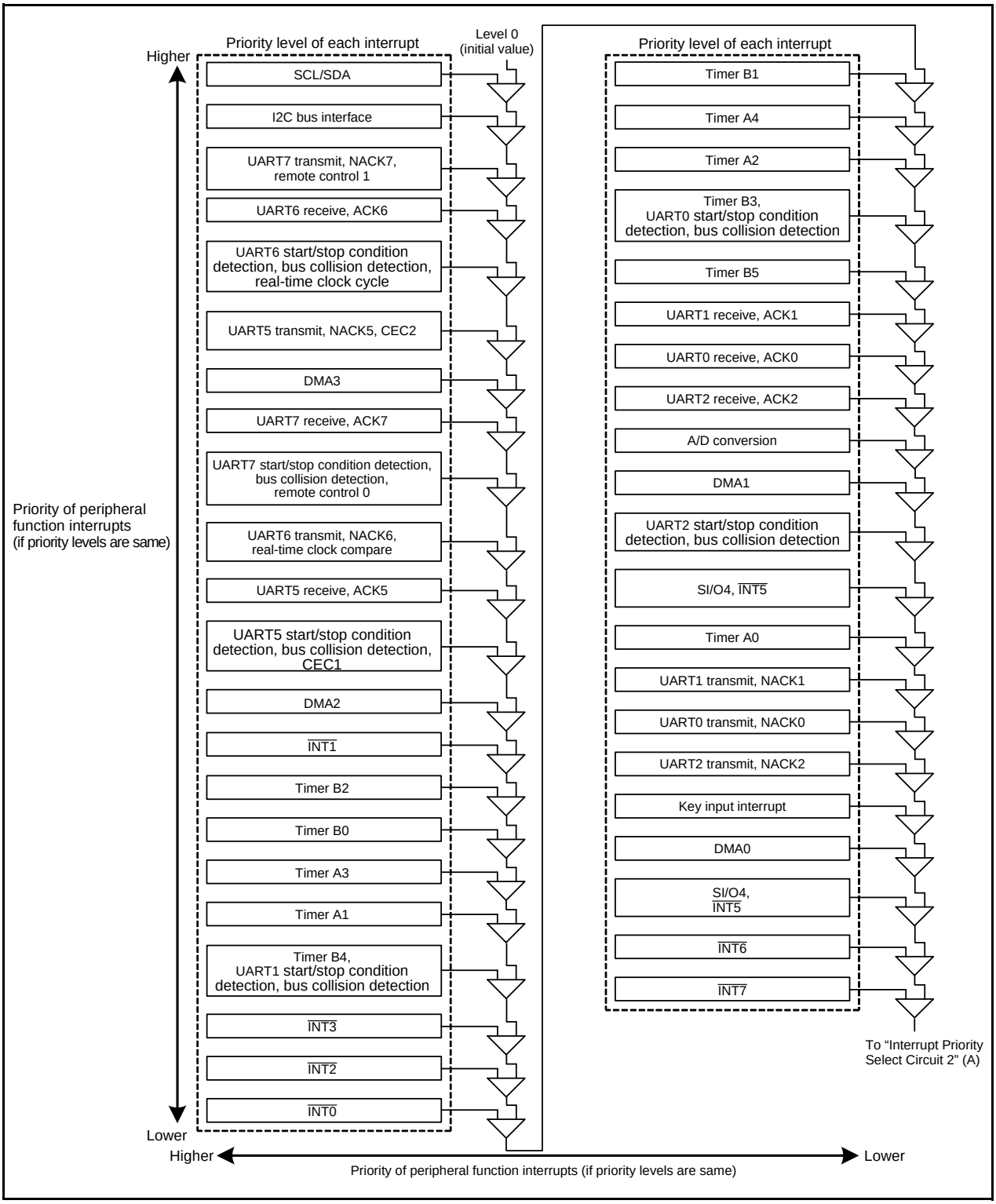


Figure 14.8 Interrupt Priority Select Circuit 1

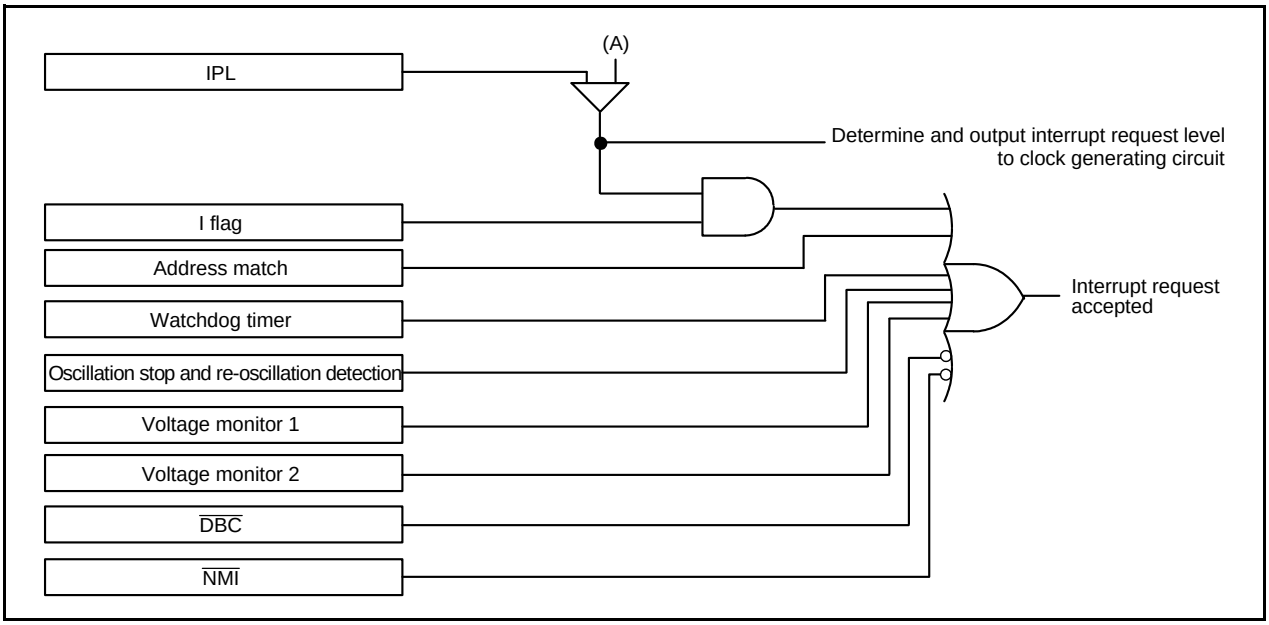


Figure 14.9 Interrupt Priority Select Circuit 2

14.7.9 Multiple Interrupts

The following shows the internal bit states when control has branched to an interrupt routine.

- I flag = 0 (interrupt disabled)
- IR bit = 0 (interrupt not requested)
- Interrupt priority level= IPL

By setting the I flag to 1 (interrupt enabled) in the interrupt routine, an interrupt request with higher priority than the IPL can be acknowledged.
The interrupt requests not acknowledged because of their low interrupt priority level are kept pending. When the IPL is restored by an REIT instruction and interrupt priority is resolved against it, the pending interrupt request is acknowledged if the following condition is met:

Interrupt priority level of pending interrupt request > Restored IP

14.8 $\overline{\text{INT}}$ Interrupt

The $\overline{\text{INTi}}$ interrupt (i = 0 to 7) is triggered by the edges of external inputs. The edge polarity is selected using the IFSRi bit in the IFSR register, or the IFSR30 or IFSR31 bit in the IFSR3A register.

The $\overline{\text{INT4}}$ and $\overline{\text{INT5}}$ each share an interrupt vector and interrupt control register with SI/O3 and SI/O4, respectively. To use the $\overline{\text{INT4}}$ interrupt, set the IFSR6 bit in the IFSR register to 1 ($\overline{\text{INT4}}$). To use the $\overline{\text{INT5}}$ interrupt, set the IFSR7 bit in the IFSR register to 1 ($\overline{\text{INT5}}$).

After modifying the IFSR6 or IFSR7 bit, set the corresponding IR bit to 0 (interrupt not requested) before enabling the interrupt.

To use the $\overline{\text{INT6}}$ interrupt, set the PCR5 bit in the PCR register to 0 ($\overline{\text{INT6}}$ input enabled). To use the $\overline{\text{INT7}}$ interrupt, set the PCR6 bit in the PCR register to 0 ($\overline{\text{INT7}}$ input enabled).

14.9 $\overline{\text{NMI}}$ Interrupt

An $\overline{\text{NMI}}$ interrupt is generated when input to the $\overline{\text{NMI}}$ pin changes state from high to low. The $\overline{\text{NMI}}$ interrupt is a non-maskable interrupt. To use the $\overline{\text{NMI}}$ interrupt, set the PM24 bit in the PM2 register to 1 ($\overline{\text{NMI}}$ function). The $\overline{\text{NMI}}$ input uses the digital filter. Refer to 13. “Programmable I/O Ports” for the digital filter. Figure 14.10 shows $\overline{\text{NMI}}$ Interrupt Block Diagram.

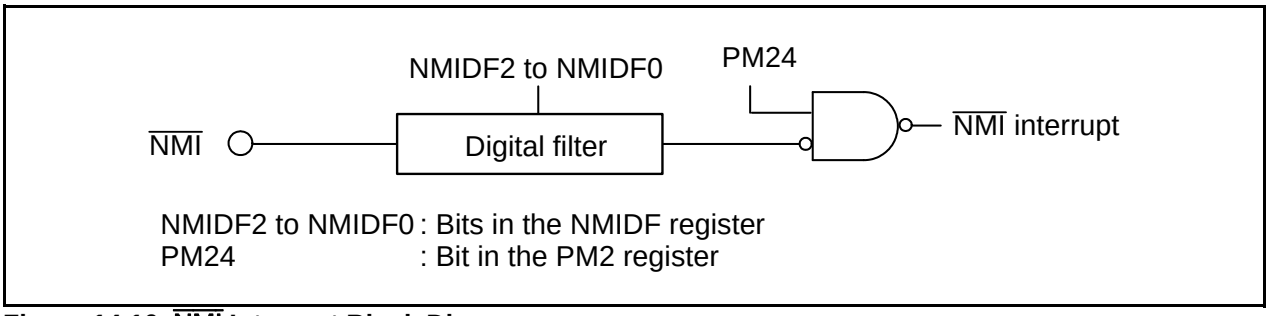


Figure 14.10 $\overline{\text{NMI}}$ Interrupt Block Diagram

14.10 Key Input Interrupt

If the PCR7 bit in the PCR register is 0 ($\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ key input enabled), set bits PD10_4 to PD10_7 in the PD10 register to 0 (input). When input to any pin from P10_4 to P10_7 becomes low, the IR bit in the KUPIC register becomes 1 (key input interrupt request). When using any pin from $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ for the key input interrupt, do not use all four pins AN4 to AN7 as analog input pins. While input to any pin from P10_4 to P10_7 is low, inputs to all other pins of the port are not detected as interrupts.

Key input interrupts can be used as a key-on wake up function for getting the MCU out of wait or stop mode.

Figure 14.11 shows Block Diagram of Key Input Interrupt.

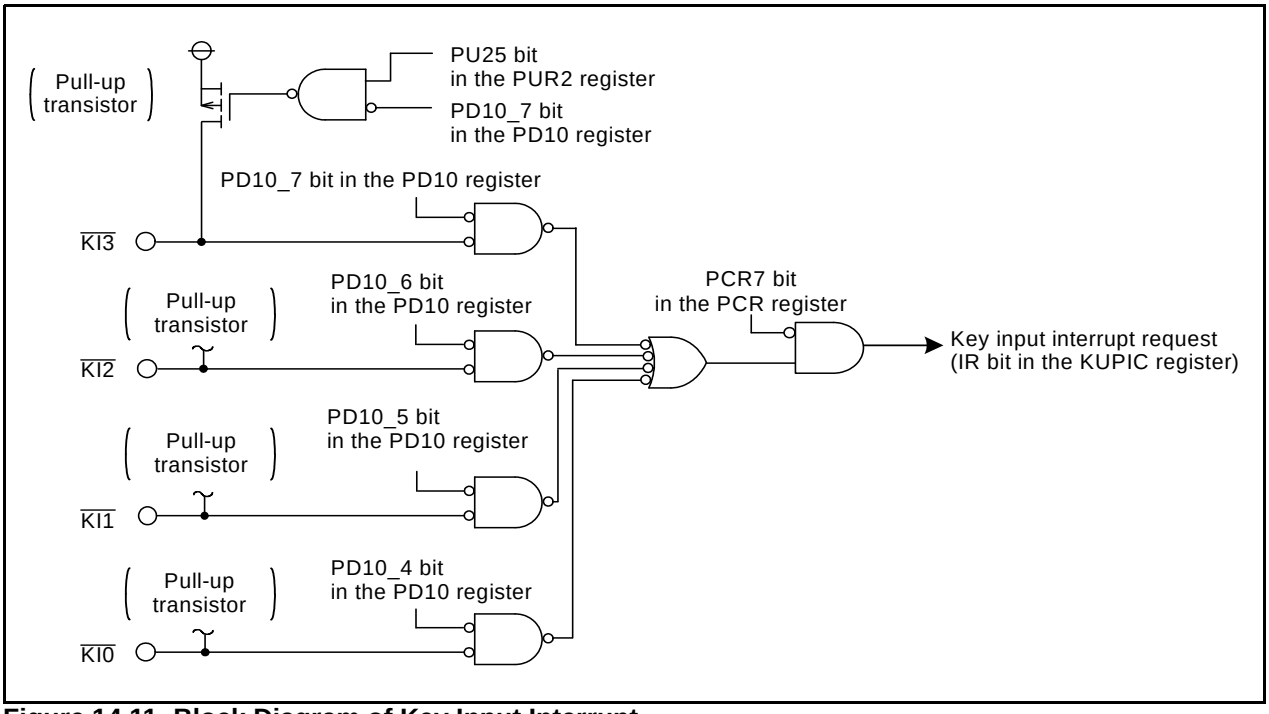


Figure 14.11 Block Diagram of Key Input Interrupt

14.11 Address Match Interrupt

An address match interrupt is generated immediately before executing the instruction at the address indicated by the RMADi register (i = 0 to 3). Set the start address of any instruction in the RMADi register. Use bits AIER0 and AIER1 in the AIER register, and bits AIER20 and AIER21 in the AIER2 register to enable or disable the interrupt. Note that the address match interrupt is unaffected by the I flag and IPL. When an address match interrupt request is acknowledged, the value of the PC that is saved to the stack area (refer to 14.7.5 “Saving Registers”) varies depending on the instruction at the address indicated by the RMADi register. (The value of the PC that is saved to the stack area is not the correct return address.) Therefore, follow one of the methods described below to return from the address match interrupt.

- Rewrite the contents of the stack and then use the REIT instruction to return.
- Restore the stack to its previous state by using the POP or other instructions before the interrupt request was accepted and then use a jump instruction to return.

Table 14.11 lists the Value of PC Saved on Stack Area When Address Match Interrupt Request Accepted. Note that when using an 8-bit external bus, no address match interrupts can be used for external areas. Refer to 14.2.7 “Address Match Interrupt Enable Register (AIER)”, 14.2.8 “Address Match Interrupt Enable Register 2 (AIER2)”, 14.2.9 “Address Match Interrupt Register i (RMADi) (i = 0 to 3)”.

Table 14.11 Value of PC Saved on Stack Area When Address Match Interrupt Request Accepted

Instruction at the Address Indicated by the RMADi Register	Value of the PC that is saved to the stack area
• 16-bit operation code instructions • Instruction shown below among 8-bit operation code instructions ADD.B:S #IMM8, dest SUB.B:S #IMM8, dest AND.B:S #IMM8, dest OR.B:S #IMM8, dest MOV.B:S #IMM8, dest STZ #IMM8, dest STNZ #IMM8, dest STZX #IMM81, #IMM82,dest CMP.B:S #IMM8, dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM, dest (However, dest = A0 or A1)	The address indicated by the RMADi register +2
Instructions other than the above	The address indicated by the RMADi register +1

Value of PC that saved on stack area: Refer to 14.7.5 “Saving Registers”.

Table 14.12 Relationship between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Sources	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER0	RMAD0
Address match interrupt 1	AIER1	RMAD1
Address match interrupt 2	AIER20	RMAD2
Address match interrupt 3	AIER21	RMAD3

14.12 Non-Maskable Interrupt Source Discrimination

The watchdog timer interrupt, oscillation stop and re-oscillation detection interrupt, voltage monitor 1 interrupt, and voltage monitor 2 interrupt share the same interrupt vector. When using some functions together, read the detect flags of the events in an interrupt processing program, and determine the interrupt source of the interrupt request. Table 14.13 lists Bits Used for Non-Maskable Interrupt Source Discrimination.

Table 14.13 Bits Used for Non-Maskable Interrupt Source Discrimination

Interrupt	Detect Flag	
	Bit Position	Function
Watchdog timer	VW2C3 bit in the VW2C register (watchdog timer underflow detected)	0: not detected 1: detected
Oscillation stop and re-oscillation detection	CM22 bit in the CM2 register (oscillation stop and re-oscillation detected)	
Voltage monitor 1	VW1C2 bit in the VW1C register (Vdet1 passage detected)	
Voltage monitor 2	VW2C2 bit in the VW2C register (Vdet2 passage detected)	

14.13 Notes on Interrupts

14.13.1 Reading Address 00000h

Do not read the address 00000h by a program. When a maskable interrupt request is accepted, the CPU reads interrupt information (interrupt number and interrupt request priority level) from address 00000h during the interrupt sequence. At this time, the IR bit of the accepted interrupt is cleared to 0.
If the address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. Thus, some problems may be caused: interrupts may be canceled, and an unexpected interrupt request may be generated.

14.13.2 SP Setting

Set a value in the SP (USP, ISP) before accepting an interrupt. The SP (USP, ISP) is set to 0000h after reset. Therefore, if an interrupt is accepted before setting a value in the SP (USP, ISP), the program may go out of control.
Especially when using the $\overline{\text{NMI}}$ interrupt, set a value in the ISP at the beginning of the program. For the first instruction after reset only, all interrupts including the $\overline{\text{NMI}}$ interrupt are disabled.

14.13.3 $\overline{\text{NMI}}$ Interrupt

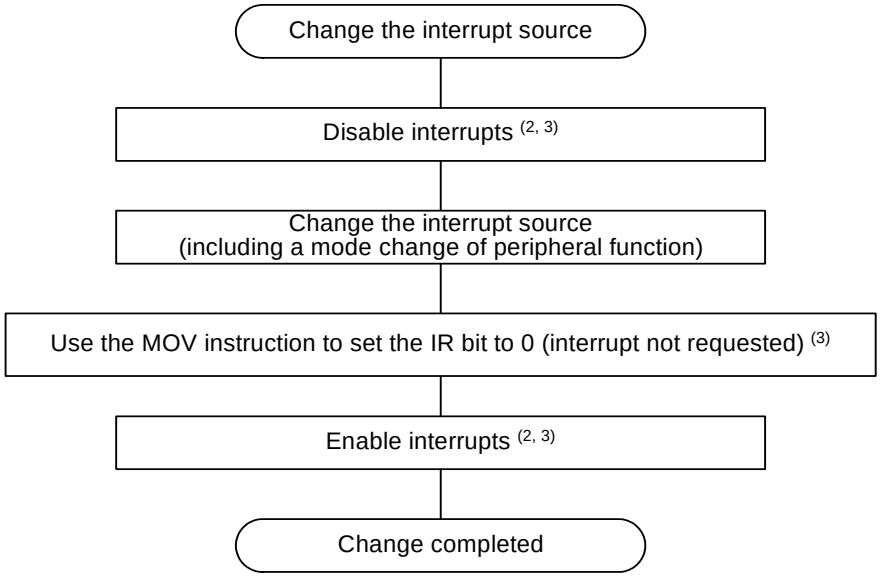
- When the $\overline{\text{NMI}}$ interrupt is not used, set the PM24 bit in the PM2 register to 0 ($\overline{\text{NMI}}$ interrupt disabled).
- Stop mode cannot be entered while the 24 bit is 1 ($\overline{\text{NMI}}$ interrupt enabled) and input on the $\overline{\text{NMI}}$ pin is low. When input on the $\overline{\text{NMI}}$ pin is low, the CM10 bit in the CM1 register is fixed to 0.
- Do not enter wait mode while the 24 bit is 1 ($\overline{\text{NMI}}$ interrupt enabled) and input on the $\overline{\text{NMI}}$ pin is low because the CPU clock remains active even though the CPU stops, and therefore, the current consumption of the chip does not drop. In this case, the normal condition is restored by the next interrupt generated.
- Set the low- and high-level durations of the input signal to the $\overline{\text{NMI}}$ pin to 2 CPU clock cycles + 300 ns or more.

14.13.4 Changing an Interrupt Source

If the interrupt source is changed, the IR bit in the interrupt control register may inadvertently be set to 1 (interrupt requested). To use an interrupt, change the interrupt source, and then set the IR bit to 0 (interrupt not requested).

In this section, the changing of an interrupt source refers to all elements (e.g. changing the mode of a peripheral function) used in changing the interrupt source, polarity, and timing assigned to each software interrupt number. When using an element to change the interrupt source, polarity, or timing, make the change before setting the IR bit to 0 (interrupt not requested). Refer to the descriptions of the individual peripheral functions for details of the peripheral function interrupts.

Figure 14.12 shows the Procedure for Changing the Interrupt Generate Factor.



IR bit: A bit in the interrupt control register for the interrupt whose interrupt source is to be changed

Notes :

1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. Use the I flag for the $\overline{\text{INTi}}$ interrupt (i = 0 to 7).
   For the interrupts from peripheral functions other than the $\overline{\text{INTi}}$ interrupt, turn off the peripheral function that is the source of the interrupt in order not to generate an interrupt request before changing the interrupt source. In this case, if the maskable interrupts can all be disabled without causing a problem, use the I flag. Otherwise, use the corresponding bits ILVL2 to ILVL0 for the interrupt whose interrupt source is to be changed.
3. Refer to the following “Rewriting the Interrupt Control Register” for details about the instructions to use and the notes to be taken for instruction execution.

Figure 14.12 Procedure for Changing the Interrupt Generate Factor

14.13.5 Rewriting the Interrupt Control Register

(a) The interrupt control register for any interrupt should be modified in places where no requests for that register may occur. If an interrupt request generation is a possibility, disable an interrupt and then rewrite the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling an interrupt, be careful with the instruction used.

- Changing bits other than the IR bit
  When interrupts corresponding to the register occur, the IR bit may not be set to 1 (interrupt requested) and the interrupts may be ignored. If this causes a problem, use one of the following instructions to change the registers.
  Instructions: AND, OR, BCLR, or BSET.
- Changing the IR bit
  Depending on the instruction used, the IR bit may not always be set to 0 (interrupt not requested). Therefore, use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample program code shown below. (Refer to (b) regarding rewriting the contents of the interrupt control registers using the sample program code.)

Examples 1 through 3 show how to prevent the I flag from being set to 1 (interrupt enabled) before the contents of the interrupt control register are rewritten, owing to the effects of the internal bus and the instruction queue buffer.

Example 1: Using the NOP instruction to pause the program until the interrupt control register is modified

```
INT_SWITCH1:
    FCLR    I           ; Disable interrupts.
    AND.B   #00h, 0055h ; Set the TA0IC register to 00h.
    NOP                 ;
    NOP
    FSET    I           ; Enable interrupts.
```

The number of the NOP instructions is as follows.
PM20 = 1 (1 wait): 2, PM20 = 0 (2 waits): 3, when using the $\overline{\text{HOLD}}$ function: 4.

Example 2: Using a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I           ; Disable interrupts.
    AND.B   #00h, 0055h ; Set the TA0IC register to 00h.
    MOV.W   MEM, R0     ; Dummy read.
    FSET    I           ; Enable interrupts.
```

Example 3: Using the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I           ; Disable interrupts.
    AND.B   #00h, 0055h ; Set the TA0IC register to 00h.
    POPC    FLG         ; Enable interrupts.
```

14.13.6 $\overline{\text{INT}}$ Interrupt

- Either a low level of at least tw (INL) width or a high level of at least tw (INH) width is necessary for the signal input to pins $\overline{\text{INT0}}$ through $\overline{\text{INT7}}$ regardless of the CPU operation clock.
- If the POL bit in registers INT0IC to INT7IC, bits IFSR7 to IFSR0 in the IFSR register, or bits IFSR31 to IFSR30 in the IFSR3A register are changed, the IR bit may inadvertently be set to 1 (interrupt requested). Be sure to set the IR bit to 0 (interrupt not requested) after changing any of these register bits.

15. Watchdog Timer

15.1 Introduction

The watchdog timer contains a 15-bit counter, and the count source protection mode (enabled/disabled) can be set.
Table 15.1 shows Watchdog Timer Specification.
Refer to 6.4.8 “Watchdog Timer Reset” for details of watchdog timer reset.
Figure 15.1 shows Watchdog Timer Block Diagram.

Table 15.1 Watchdog Timer Specification

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	fOCO-S
Count operation	Decrement	
Count start conditions	Either of the following can be selected (selected by the WDTON bit in the OFS1 address). • Count automatically starts after reset. • Count starts by writing to the WDTS register.	
Count stop condition	Stop mode, wait mode, bus hold	None
Watchdog timer counter initial value setting conditions	• Reset (Refer to 6. “Resets”) • Write 00h, and then FFh to the WDTR register. • Underflow	
Operation when the timer underflows	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Prescaler divide ratio Divide-by-16 or divide-by-128 (selected by the WDC7 bit in the WDC register) However, divide-by-2 is selected when the CM07 bit in the CM0 register is 1 (sub clock). • Count source protection mode Enabled or disabled (selected by the CSPROINI bit in the OFS1 address and the CSPRO bit in the CSPR register)	

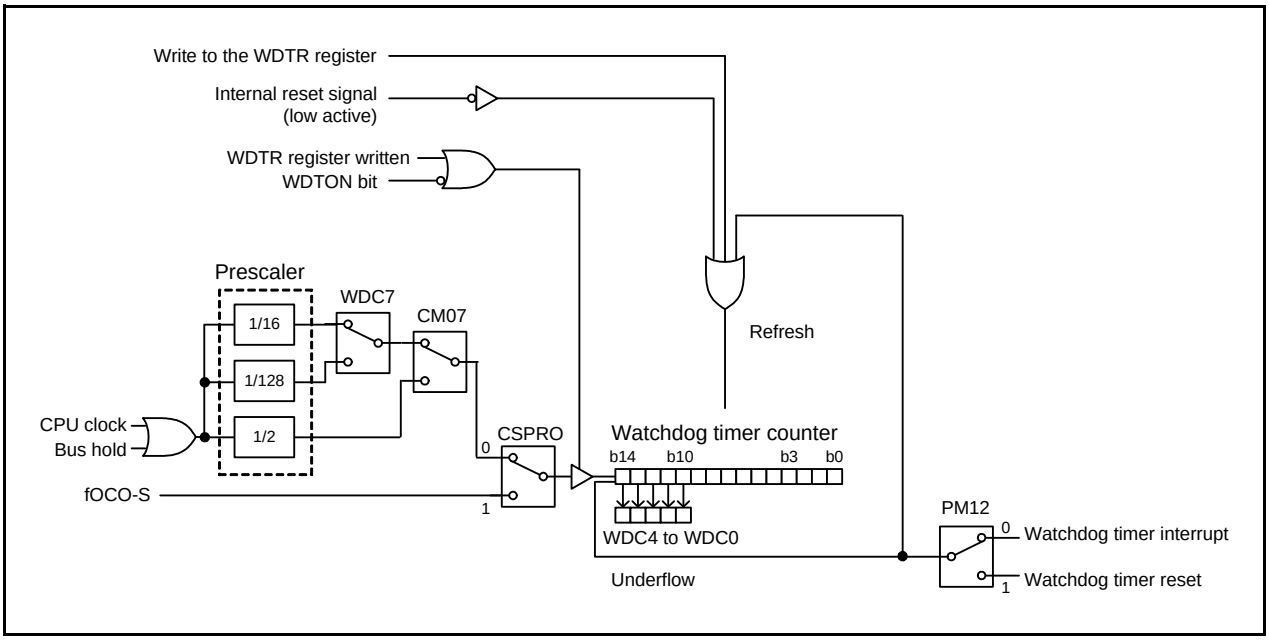


Figure 15.1 Watchdog Timer Block Diagram

15.2 Registers

Table 15.2 Register Structure

Address	Register Name	Register Symbol	After Reset
002Ch	Voltage Monitor 2 Circuit Control Register	VW2C	1000 0X10b
037Ch	Count Source Protection Mode Register	CSPR	00h (1)
037Dh	Watchdog Timer Reset Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb

Note:
1. When the CSPROINI bit in the OFS1 address is 0, the value after reset becomes 1000 0000b.

15.2.1 Voltage Monitor 2 Circuit Control Register (VW2C)

Voltage Monitor 2 Circuit Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol: VW2C
Address: 002Ch
After Reset: 1000 0X10b (hardware reset, power-on reset, voltage monitor 0 reset)

Bit Symbol	Bit Name	Function	RW
VW2C0	Voltage monitor 2 interrupt/ reset enable bit	0 : Disabled 1 : Enabled	RW
VW2C1	Voltage monitor 2 digital filter disable mode select bit	0 : Enable digital filter 1 : Disable digital filter	RW
VW2C2	Voltage change detection flag	0 : Not detected 1 : Vdet2 passage detected	RW
VW2C3	WDT detection flag	0 : Not detected 1 : Watchdog timer underflow detected	RW
VW2F0	Sampling clock select bit	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW2F1			
VW2C6	Voltage monitor 2 circuit mode select bit	0 : Voltage monitor 2 interrupt at Vdet2 passage 1 : Voltage monitor 2 reset at Vdet2 passage	RW
VW2C7	Voltage monitor 2 interrupt/ reset generation condition select bit	0 : When VCC1 reaches Vdet2 or above 1 : When VCC1 reaches Vdet2 or below	RW

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
Since rewriting the VW2C register may set the VW2C2 bit to 1, set the VW2C2 bit to 0 after rewriting the VW2C register.
Bits VW2C2 and VW2C3 do not change at voltage monitor 1 reset, voltage monitor 2 reset, oscillation stop detection reset, watchdog timer reset, or software reset.

VW2C3 (WDT Detection Flag) (b3)

Use this bit in an interrupt routine to determine the source of the interrupts from the watchdog timer, the oscillation stop/re-oscillation detection, the voltage monitor 1, and the voltage monitor 2.
Conditions to become 0:

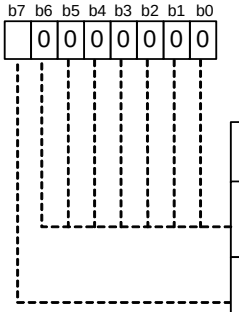
- Hardware reset, power-on reset, or voltage monitor 0 reset
- Writing 0 by a program

Condition to become 1:

- Watchdog timer underflow detected
  (This flag remains unchanged even if 1 is written by a program.)

15.2.2 Count Source Protection Mode Register (CSPR)

Count Source Protection Mode Register



Symbol	Address	After Reset
CSPR	037Ch	0000 0000b (When the CSPROINT bit in the OFS1 address is 1) 1000 0000b (When the CSPROINT bit in the OFS1 address is 0)

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Reserved bits	Set to 0	RW
CSPRO	Count source protection mode select bit	0 : Count source protection mode disabled 1 : Count source protection mode enabled	RW

CSPRO (Count Source Protection Mode Select Bit) (b7)

Select the CSPRO bit before the watchdog timer starts counting. Once counting starts, do not change the CSPRO bit.
Condition to become 0:

- Reset when the CSPROINI bit in the OFS1 address is 1.
  (This flag remains unchanged even if 0 is written by a program.)

Condition to become 1:

- When the CSPROINI bit in the OFS1 address is 0
- Write 0, and then write 1.
  Make sure no interrupts or DMA transfers will occur between setting the bit to 0 and setting it to 1.

15.2.3 Watchdog Timer Reset Register (WDTR)

Watchdog Timer Reset Register

b7	b0	Symbol	Address	After Reset
		WDTR	037Dh	Undefined

Function	RW
Setting 00h and then FFh refreshes the watchdog timer.	WO

After the watchdog timer interrupt occurs, refresh the watchdog timer by setting the WDTR register.

15.2.4 Watchdog Timer Start Register (WDTS)

Watchdog Timer Start Register

b7	b0	Symbol	Address	After Reset
		WDTS	037Eh	Undefined

Function	RW
The watchdog timer starts counting after a write instruction to this register	WO

The WDTS register is enabled when the WDTON bit in the OFS1 address is 1 (watchdog timer is in a stopped state after reset).

15.2.5 Watchdog Timer Control Register (WDC)

Watchdog Timer Control Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	X					

Symbol	Address	After Reset
WDC	037Fh	00XX XXXXb

Bit Symbol	Bit Name	Function	RW
WDC0	Higher-order bits (b14 to b10) of the watchdog timer can be read		RO
WDC1			RO
WDC2			RO
WDC3			RO
WDC4			RO
— (b5)	No register bit. If necessary, set to 0. Read as 0		—
— (b6)	Reserved bit	Set to 0	RW
WDC7	Prescaler select bit	0 : Divide-by-16 1 : Divide-by-1128	RW

WDC4-WDC0 (b4-b0)

When reading the watchdog timer value while the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), read bits WDC4 to WDC0 more than three times to determine the values.

15.3 Optional Function Select Area

15.3.1 Optional Function Select Address 1 (OFS1)

Optional Function Select Address 1

b7	b6	b5	b4	b3	b2	b1	b0
			1			1	

Symbol: OFS1 | Address: FFFFFh | Factory Setting: FFh

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Watchdog timer starts automatically after reset. 1 : Watchdog timer is in a stopped state after reset.	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect cancel bit	0 : ROM code protection cancelled. 1 : ROMCP1 bit enabled.	RW
ROMCP1	ROM code protect bit	0 : ROM code protection enabled. 1 : ROM code protection disabled.	RW
— (b4)	Reserved bit	Set to 1.	RW
VDSEL1	Vdet0 select bit 1	0 : 2.85 V (Vdet0_2) 1 : 1.90 V (Vdet0_0)	RW
LVDAS	Voltage detection 0 circuit start bit	0 : Voltage monitor 0 reset enabled after hardware reset. 1 : Voltage monitor 0 reset disabled after hardware reset.	RW
CSPROINI	After-reset count source protection mode select bit	0 : Count source protection mode enabled after reset. 1 : Count source protection mode disabled after reset.	RW

The OFS1 address exists in flash memory. Set a proper value when writing a program in flash memory. The OFS1 address is set to FFh when the block including the OFS1 address is erased.

WDTON (Watchdog Timer Start Select Bit) (b0)

Set the WDTON bit to 0 (watchdog timer starts automatically after reset) when setting the CSPROINI bit to 0 (count source protection mode enabled after reset).

CSPROINI (After-Reset Count Source Protection Mode Select Bit) (b7)

Set the WDTON bit to 0 (watchdog timer starts automatically after reset) when setting the CSPROINI bit to 0 (count source protection mode enabled after reset).

15.4 Operations

15.4.1 Count Source Protection Mode Disabled

The CPU clock is used as the watchdog timer count source when count source protection mode is disabled.
Table 15.3 lists Watchdog Timer Specifications (Count Source Protection Mode Disabled).

Table 15.3 Watchdog Timer Specifications (Count Source Protection Mode Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrement
Cycles	When the CM07 bit in the CM0 register is 0 (main clock, PLL clock, fOCO-F, fOCO-S): $\frac{\text{Prescaler divide value (n)} \times \text{watchdog timer count value (32768)}}{\text{CPU clock}}$ (1) n: 16 or 128 (selected by the WDC7 bit in the WDC register) ex.) When CPU clock frequency is 16 MHz and the prescaler division rate is 16, the watchdog timer cycle is approximately 32.8 ms. When the CM07 bit is 1 (sub clock): $\frac{\text{Prescaler divide value (2)} \times \text{watchdog timer count value (32768)}}{\text{CPU clock}}$ (1)
Watchdog timer counter initial value setting	• Reset (Refer to 6. “Resets”.) • Write 00h, and then FFh to the WDTR register. • Underflow
Count start conditions	Set the WDTON bit in the OFS1 address to select the watchdog timer operation after reset. • WDTON bit is 1 (watchdog timer is in stop state after reset) The watchdog timer and prescaler stop after reset and count starts by writing to the WDTS register. • WDTON bit is 0 (watchdog timer starts automatically after reset) The watchdog timer and prescaler start counting automatically after reset.
Count stop conditions	• Stop mode • Wait mode • Bus hold (Count resumes from the hold value after exiting.)
Operation when timer underflows	• PM12 bit in the PM1 register is 0 Watchdog timer interrupt • PM12 bit in the PM1 register is 1 Watchdog timer reset (See 6.4.8 “Watchdog Timer Reset”.)

Notes:
1. Writing 00h and then FFh to the WDTR register initializes the watchdog timer, but not the prescaler. Thus, some errors in the watchdog timer period may be caused by the prescaler. The prescaler is initialized after reset.

15.4.2 Count Source Protection Mode Enabled

The fOCO-S is used as the watchdog timer count source when the count source protection mode is enabled.
Table 15.4 lists the Watchdog Timer Specifications (Count Source Protection Mode Enabled).

Table 15.4 Watchdog Timer Specifications (Count Source Protection Mode Enabled)

Item	Specification
Count source	fOCO-S (The 125 kHz on-chip oscillator clock automatically starts oscillating.)
Count operation	Decrement
Cycle	$\frac{\text{Watchdog timer count value (4096)}}{\text{fOCO-S}}$ (The watchdog timer cycle is approximately 32.8 ms.)
Watchdog timer counter initial value setting	• Reset (Refer to 6. “Resets”.) • Write 00h, and then FFh to the WDTR register. • Underflow
Count start conditions	Set the WDTON bit in the OFS1 address to select the watchdog timer operation after reset. • WDTON bit is 1 (watchdog timer is stopped after reset) The watchdog timer and prescaler stop after reset and count starts by writing to the WDTS register. • WDTON bit is 0 (watchdog timer starts automatically after reset) The watchdog timer and prescaler start counting automatically after reset.
Count stop condition	None (Count does not stop in wait mode or by bus hold once count starts. The MCU does not enter stop mode.)
Operation when timer underflows	Watchdog timer reset (See 6.4.8 “Watchdog Timer Reset”).

When the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), the watchdog timer counter underflows every 4096 cycles because three low-order bits are not used.

Also when the CSPRO bit is set to 1 (count source protection mode enabled), the following bits change:

- The CM14 bit in the CM1 register becomes 0 (125 kHz on-chip oscillator on). It remains unchanged even if 1 is written, and the 125 kHz on-chip oscillator does not stop.
- The PM12 bit in the PM1 register becomes 1 (watchdog timer reset when watchdog timer counter underflows).
- The CM10 bit in the CM1 register remains unchanged even if 1 is written, and the MCU does not enter stop mode.

15.5 Interrupts

Watchdog timer interrupts are non-maskable interrupts.

The watchdog timer interrupt, oscillation stop and re-oscillation detection interrupt, voltage monitor 1 interrupt, and voltage monitor 2 interrupt share an vector. When using multiple functions, read the detect flag in an interrupt process program to determine which interrupt factor sends an interrupt request.

The VW2C3 bit in the VW2C register is the detect flag for the watchdog timer. After the interrupt factor is determined, set the VW2C3 bit to 0 (not detected) by a program.

15.6 Notes on Watchdog Timer

After the watchdog timer interrupt occurs, use the WDTR register to refresh the watchdog timer counter.

16. DMAC

16.1 Introduction

The direct memory access controller (DMAC) allows data to be transferred without CPU intervention. Four DMAC channels are included. Each time a DMA request occurs, the DMAC transfers one (8- or 16-bit) unit of data from the source address to the destination address. The DMAC uses the same data bus used by the CPU. Because the DMAC has higher priority for bus control than the CPU, and because it makes use of a cycle steal method, it can transfer one word (16 bits) or one byte (8 bits) of data within a very short time after a DMA request is generated. Figure 16.1 shows the DMAC Block Diagram. Table 16.1 lists DMAC Specifications, and Figure 16.1 shows DMAC Block Diagram.

Table 16.1 DMAC Specifications

Item		Specification
Number of channels		4 (cycle steal method)
Transfer memory spaces		• From a given address in the 1-Mbyte space to a fixed address • From a fixed address to a given address in the 1-Mbyte space • From a fixed address to a fixed address
Maximum number of bytes transferred		128 Kbytes (with 16-bit transfers) or 64 Kbytes (with 8-bit transfers)
DMA request factors (1)		43 factors Falling edge of $\overline{INT0}$ to $\overline{INT7}$ (8) Both edges of $\overline{INT0}$ to $\overline{INT7}$ (8) Timer A0 to timer A4 interrupt requests (5) Timer B0 to timer B5 interrupt requests (6) UART0 to 2, UART5 to 7 transmission interrupt requests (6) UART0 to 2, UART5 to 7 reception/ACK interrupt requests (6) SI/O3, SI/O4 interrupt requests (2) A/D conversion interrupt requests (1) Software triggers (1)
Channel priority		DMA0 > DMA1 > DMA2 > DMA3 (DMA0 takes precedence)
Transfers		8 bits or 16 bits
Transfer address direction		Forward or fixed (The source and destination addresses cannot both be in the forward direction.)
Transfer mode	Single transfer	Transfer is completed when the DMAi transfer counter underflows.
	Repeat transfer	When the DMAi transfer counter underflows, it is reloaded with the value of the DMAi transfer counter reload register and DMA transfer continues.
DMA interrupt request generation timing		When the DMAi transfer counter underflows
DMA transfer start		Data transfer is initiated each time a DMA request is generated when the DMAE bit in the DMAiCON register is 1 (enabled).
DMA transfer stop	Single transfer	• When the DMAE bit is set to 0 (disabled) • After the DMAi transfer counter underflows
	Repeat transfer	When the DMAE bit is set to 0 (disabled)
Reload timing for forward address pointer and DMAi transfer counter		When a data transfer is started after setting the DMAE bit to 1 (enabled), the forward address pointer is reloaded with the value of the SARi or DARi pointer whichever is specified to be in the forward direction and the DMAi transfer counter is reloaded with the value of the DMAi transfer counter reload register.
DMA transfer cycles		Minimum 3 cycles between SFR and internal RAM

i = 0 to 3

Note:

1. The selectable sources of DMA requests differ for each channel.

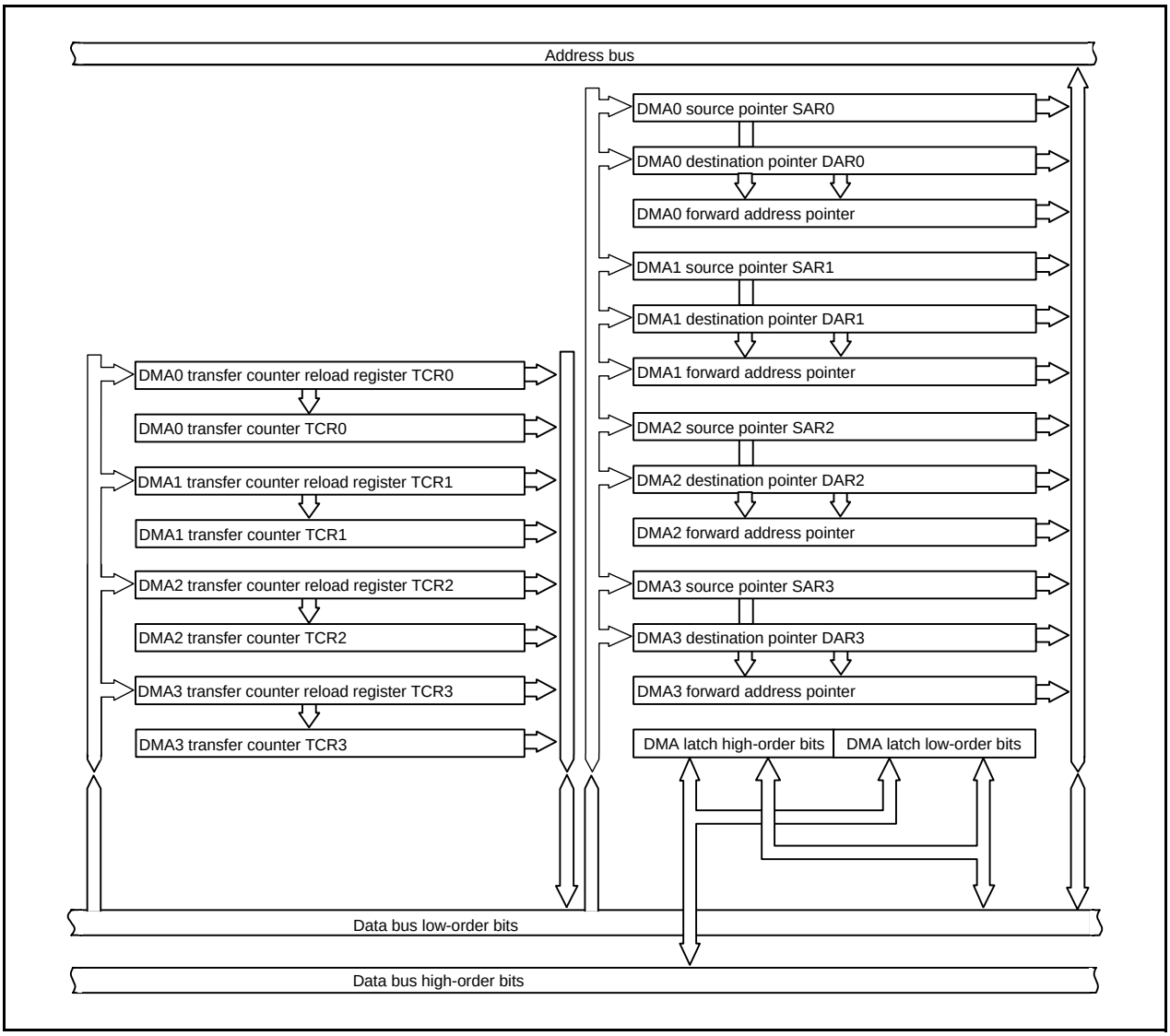


Figure 16.1 DMAC Block Diagram

16.2 Registers

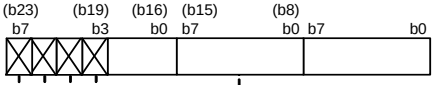
Table 16.2 lists Register Structure. Do not access these registers during DMAC operation.

Table 16.2 Register Structure

Address	Register Name	Register Symbol	After Reset
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
0390h	DMA2 Source Select Register	DM2SL	00h
0392h	DMA3 Source Select Register	DM3SL	00h
0398h	DMA0 Source Select Register	DM0SL	00h
039Ah	DMA1 Source Select Register	DM1SL	00h

16.2.1 DMAi Source Pointer (SARi) (i = 0 to 3)

DMAi Source Pointer (i = 0 to 3)



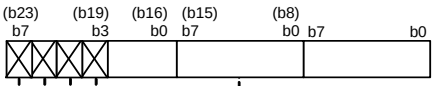
Symbol	Address	After Reset
SAR0	0182h to 0180h	0X XXXXh
SAR1	0192h to 0190h	0X XXXXh
SAR2	01A2h to 01A0h	0X XXXXh
SAR3	01B2h to 01B0h	0X XXXXh

Function	Setting Range	RW
Set the source address of transfer	00000h to FFFFFh	RW
No register bits. If necessary, set to 0. Read as 0		—

If the DSD bit in the DMiCON register is 0 (fixed), write to this register when the DMAE bit in the DMiCON register is 0 (DMA disabled).
If the DSD bit is 1 (forward direction), this register can be written to at any time.
If the DSD bit is 1 and the DMAE bit is 1 (DMA enabled), the DMAi forward address pointer can be read from this register. Otherwise, the value written to it can be read.
The forward address pointer is incremented when a DMA request is accepted.

16.2.2 DMAi Destination Pointer (DARi) (i = 0 to 3)

DMAi Destination Pointer (i = 0 to 3)



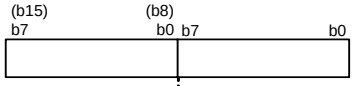
Symbol	Address	After Reset
DAR0	0186h to 0184h	0X XXXXh
DAR1	0196h to 0194h	0X XXXXh
DAR2	01A6h to 01A4h	0X XXXXh
DAR3	01B6h to 01B4h	0X XXXXh

Function	Setting Range	RW
Set the destination address of transfer	00000h to FFFFFh	RW
No register bits. If necessary, set to 0. Read as 0		—

If the DAD bit in the DMiCON register is 0 (fixed), write to this register when the DMAE bit in the DMiCON register is 0 (DMA disabled).
If the DAD bit is 1 (forward direction), this register can be written to at any time.
If the DAD bit is 1 and the DMAE bit is 1 (DMA enabled), the DMAi forward address pointer can be read from this register. Otherwise, the value written to it can be read.
The forward address pointer is incremented on accepting a DMA request.

16.2.3 DMAi Transfer Counter (TCRi) (i = 0 to 3)

DMAi Transfer Counter (i = 0 to 3)



Symbol	Address	After Reset
TCR0	0189h to 0188h	Undefined
TCR1	0199h to 0198h	Undefined
TCR2	01A9h to 01A8h	Undefined
TCR3	01B9h to 01B8h	Undefined

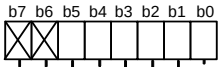
Function	Setting Range	RW
Set the transfer count minus 1.	0000h to FFFFh	RW

The written value in the TCRi register is stored in the DMAi transfer counter reload register.
The value of the DMAi transfer counter reload register is transferred to the DMAi transfer counter in either of the following cases:

- When the DMAE bit in the DMiCON register is set to 1 (DMA enabled) (single transfer mode, repeat transfer mode)
- When the DMAi transfer counter underflows (repeat transfer mode)

16.2.4 DMAi Control Register (DMiCON) (i = 0 to 3)

DMAi Control Register (i = 0 to 3)



Symbol	Address	After Reset
DM0CON	018Ch	0000 0X00b
DM1CON	019Ch	0000 0X00b
DM2CON	01ACh	0000 0X00b
DM3CON	01BCh	0000 0X00b

Bit Symbol	Bit Name	Function	RW
DMBIT	Transfer unit bit select bit	0 : 16 bits 1 : 8 bits	RW
DMASL	Repeat transfer mode select bit	0 : Single transfer 1 : Repeat transfer	RW
DMAS	DMA request bit	0 : DMA not requested 1 : DMA requested	RW
DMAE	DMA enable bit	0 : Disabled 1 : Enabled	RW
DSD	Source address direction select bit	0 : Fixed 1 : Forward	RW
DAD	Destination address direction select bit	0 : Fixed 1 : Forward	RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as 0		—

DMAS (DMA Request Bit) (b2)

Conditions to become 0:

- Set the bit to 0.
- Starting data transfer

Condition to become 1:

- Set the bit to 1.

DMAE (DMA Enable Bit) (b3)

Conditions to become 0:

- Set the bit to 0.
- The DMA transfer counter underflows (single transfer mode)

Condition to become 1:

- Set the bit to 1.

DSD (Source Address Direction Select Bit) (b4)

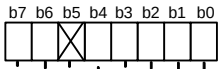
Set at least one of the DAD bit and DSD bit to 0 (address direction fixed).

DAD (Destination Address Direction Select Bit) (b5)

Set at least one of the DAD bit and DSD bit to 0 (address direction fixed).

16.2.5 DMAi Source Select Register (DMiSL) (i = 0 to 3)

DMAi Source Select Register (i = 0 to 3)



Symbol	Address	After Reset
DM0SL	0398h	00h
DM1SL	039Ah	00h
DM2SL	0390h	00h
DM3SL	0392h	00h

Bit Symbol	Bit Name	Function	RW
DSEL0	DMA request source select bit	See the bit explanation below.	RW
DSEL1			RW
DSEL2			RW
DSEL3			RW
DSEL4			RW
— (b5)	No register bit. If necessary, set to 0. Read as 0		—
DMS	DMA request source expansion select bit	0: Basic request source 1: Extended request source	RW
DSR	Software DMA request bit	A DMA request is generated by setting this bit to 1 when the DMS bit is 0 (basic source) and bits DSEL4 to DSEL0 are 00001b (software trigger). Read as 0	RW

DSEL4-DSEL0 (DMA Request Source Select Bit) (b4-b0)

The sources of DMAi requests can be selected by a combination of the DMS bit and bits DSEL4 to DSEL0 in the manner shown in Table 16.3 to Table 16.6. Table 16.3 to Table 16.6 list the sources of DMAi requests.

Table 16.3 Source of DMA Request (DMA0)

DSEL4 to DSEL0	DMS = 0 (Basic Source of Request)	DMS = 1 (Extended Source of Request)
0 0 0 0 0 b	Falling edge of INT0 pin	–
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	–
0 0 0 1 1 b	Timer A1	–
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	Both edges of INT0 pin
0 0 1 1 1 b	Timer B0	Timer B3
0 1 0 0 0 b	Timer B1	Timer B4
0 1 0 0 1 b	Timer B2	Timer B5
0 1 0 1 0 b	UART0 transmission	–
0 1 0 1 1 b	UART0 reception	–
0 1 1 0 0 b	UART2 transmission	–
0 1 1 0 1 b	UART2 reception	–
0 1 1 1 0 b	A/D conversion	–
0 1 1 1 1 b	UART1 transmission	–
1 0 0 0 0 b	UART1 reception	Falling edge of INT4 pin
1 0 0 0 1 b	UART5 transmission	Both edges of INT4 pin
1 0 0 1 0 b	UART5 reception	–
1 0 0 1 1 b	UART6 transmission	–
1 0 1 0 0 b	UART6 reception	–
1 0 1 0 1 b	UART7 transmission	–
1 0 1 1 0 b	UART7 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X indicates 0 or 1. – indicates no setting.

Table 16.4 Source of DMA Request (DMA1)

DSEL4 to DSEL0	DMS = 0 (Basic Source of Request)	DMS = 1 (Extended Source of Request)
0 0 0 0 0 b	Falling edge of INT1 pin	–
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	–
0 0 0 1 1 b	Timer A1	–
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	SI/O3
0 0 1 1 0 b	Timer A4	SI/O4
0 0 1 1 1 b	Timer B0	Both edges of INT1 pin
0 1 0 0 0 b	Timer B1	–
0 1 0 0 1 b	Timer B2	–
0 1 0 1 0 b	UART0 transmission	–
0 1 0 1 1 b	UART0 reception/ACK0	–
0 1 1 0 0 b	UART2 transmission	–
0 1 1 0 1 b	UART2 reception/ACK2	–
0 1 1 1 0 b	A/D conversion	–
0 1 1 1 1 b	UART1 reception/ACK1	–
1 0 0 0 0 b	UART1 transmission	Falling edge of INT5 pin
1 0 0 0 1 b	UART5 transmission	Both edges of INT5 pin
1 0 0 1 0 b	UART5 reception/ACK5	–
1 0 0 1 1 b	UART6 transmission	–
1 0 1 0 0 b	UART6 reception/ACK6	–
1 0 1 0 1 b	UART7 transmission	–
1 0 1 1 0 b	UART7 reception/ACK7	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X indicates 0 or 1. – indicates no setting.

Table 16.5 Source of DMA Request (DMA2)

DSEL4 to DSEL0	DMS = 0 (Basic Source of Request)	DMS = 1 (Extended Source of Request)
0 0 0 0 0 b	Falling edge of INT2 pin	–
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	–
0 0 0 1 1 b	Timer A1	–
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	–
0 0 1 1 0 b	Timer A4	Both edges of INT2 pin
0 0 1 1 1 b	Timer B0	Timer B3
0 1 0 0 0 b	Timer B1	Timer B4
0 1 0 0 1 b	Timer B2	Timer B5
0 1 0 1 0 b	UART0 transmission	–
0 1 0 1 1 b	UART0 reception	–
0 1 1 0 0 b	UART2 transmission	–
0 1 1 0 1b	UART2 reception	–
0 1 1 1 0 b	A/D conversion	–
0 1 1 1 1 b	UART1 transmission	–
1 0 0 0 0 b	UART1 reception	Falling edge of INT6 pin
1 0 0 0 1 b	UART5 transmission	Both edges of INT6 pin
1 0 0 1 0 b	UART5 reception	–
1 0 0 1 1 b	UART6 transmission	–
1 0 1 0 0 b	UART6 reception	–
1 0 1 0 1 b	UART7 transmission	–
1 0 1 1 0 b	UART7 reception	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X indicates 0 or 1. – indicates no setting.

Table 16.6 Source of DMA Request (DMA3)

DSEL4 to DSEL0	DMS = 0 (Basic Source of Request)	DMS = 1 (Extended Source of Request)
0 0 0 0 0 b	Falling edge of INT3 pin	–
0 0 0 0 1 b	Software trigger	–
0 0 0 1 0 b	Timer A0	–
0 0 0 1 1 b	Timer A1	–
0 0 1 0 0 b	Timer A2	–
0 0 1 0 1 b	Timer A3	SI/O3
0 0 1 1 0 b	Timer A4	SI/O4
0 0 1 1 1 b	Timer B0	Both edges of INT3 pin
0 1 0 0 0 b	Timer B1	–
0 1 0 0 1 b	Timer B2	–
0 1 0 1 0 b	UART0 transmission	–
0 1 0 1 1 b	UART0 reception/ACK0	–
0 1 1 0 0 b	UART2 transmission	–
0 1 1 0 1b	UART2 reception/ACK2	–
0 1 1 1 0 b	A/D conversion	–
0 1 1 1 1 b	UART1 reception/ACK1	–
1 0 0 0 0 b	UART1 transmission	Falling edge of INT7 pin
1 0 0 0 1 b	UART5 transmission	Both edges of INT7 pin
1 0 0 1 0 b	UART5 reception/ACK5	–
1 0 0 1 1 b	UART6 transmission	–
1 0 1 0 0 b	UART6 reception/ACK6	–
1 0 1 0 1 b	UART7 transmission	–
1 0 1 1 0 b	UART7 reception/ACK7	–
1 0 1 1 1 b	–	–
1 1 X X X b	–	–

X indicates 0 or 1. – indicates no setting.

16.3 Operations

16.3.1 DMA Enabled

When data transfer starts after setting the DMAE bit in the DMiCON register (i = 0 to 3) to 1 (enabled), the DMAC operates as listed below. If 1 is written to the DMAE bit when it is already set to 1, the DMAC also performs the following operation.

- The forward address pointer is reloaded with the SARi register value when the DSD bit in the DMiCON register is 1 (forward), or the DARi register value when the DAD bit in the DMiCON register is 1 (forward).
- The DMAi transfer counter is reloaded with the DMAi transfer counter reload register value.

16.3.2 DMA Request

The DMAC can generate a DMA request as triggered by the request source that is selected with the DMS bit and bits DSEL4 to DSEL0 in the DMiSL register (i = 0 to 3) on either channel. Table 16.7 lists the Timing at Which the DMAS Bit Changes State.

Whenever a DMA request is generated, the DMAS bit is set to 1 (DMA requested) regardless of whether or not the DMAE bit is set. If the DMAE bit is set to 1 (enabled) when this occurs, the DMAS bit is set to 0 (DMA not requested) immediately before a data transfer starts. This bit cannot be set to 1 by a program (writing a 1 has no effect).

If the DMAE bit is 1, the DMAS bit in almost all cases is 0 when read in a program, because a data transfer starts immediately after a DMA request is generated. Read the DMAE bit to determine whether the DMAC is enabled. When a DMA request transfer cycle is shorter than a DMA transfer cycle, the number of transfer requests and the number of transfers do not agree.

When the peripheral function is selected as a DMA source, relations with interrupts are as follows:

- DMA transfers are not affected by the I flag or interrupt control registers. DMA requests are always accepted even when interrupt requests are not accepted.
- The IR bit in the interrupt control register retains its value when a DMA transfer is accepted.

Table 16.7 Timing at Which the DMAS Bit Changes State

DMA Source	DMAS Bit in the DMiCON Register	
	Timing at Which the Bit is Set to 1	Timing at Which the Bit is Set to 0
Software trigger	When the DSR bit in the DMiSL register is set to 1	• Immediately before a data transfer starts • When set by writing a 0 by a program
External factor	When an input edge of pins $\overline{INT0}$ to $\overline{INT7}$ agrees with what is selected by bits DSEL4 to DSEL0 in the DMiSL register.	
Peripheral function	When an interrupt request of the peripheral function selected by bits DSEL4 to DSEL0 and DMS in the DMiSL register is generated. (If the IR bit in an interrupt control register is 0, the timing is when 0 is changed to 1.)	

i = 0 to 3

16.3.3 Transfer Cycles

A transfer cycle is composed of a bus cycle to read data from a source address (source read), and a bus cycle to write data to a destination address (destination write). The number of read and write bus cycles depends on the source and destination addresses.

Figure 16.2 shows Transfer Cycles for Source Read Operations. For convenience, the destination write cycle is shown as one cycle and the source read cycles for the different conditions are shown. In reality, the destination write cycle is subject to the same conditions as the source read cycle, with the transfer cycle changing accordingly. When calculating transfer cycles, take into consideration each condition for the source read and the destination write cycle. For example, when data is transferred in 16-bit units using an 8-bit bus ((2) in Figure 16.2), two source read bus cycles and two destination write bus cycles are required.

16.3.3.1 Effect of Source and Destination Addresses

When a 16-bit unit of data is transferred with a 16-bit data bus and the source address starts with an odd address, the source-read cycle is incremented by one bus cycle, compared to a source address starting with an even address.

When a 16-bit unit of data is transferred with a 16-bit data bus and the destination address starts with an odd address, the destination-write cycle is incremented by one bus cycle, compared to a destination address starting with an even address.

16.3.3.2 Effect of Software Wait

For memory or SFR accesses in which one or more software wait states are inserted, the number of bus cycles required increases by an amount equal to the number of software wait states.

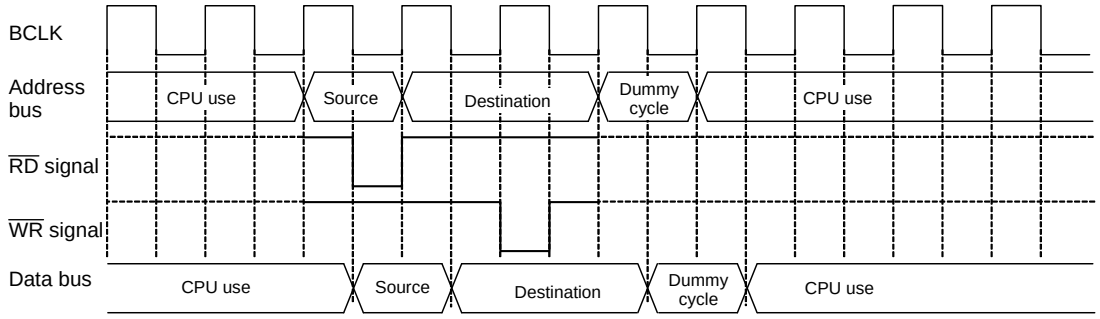
16.3.3.3 Memory Expansion Mode and Microprocessor Mode

In memory expansion or microprocessor mode, the transfer cycle is also affected by the BYTE pin level. Furthermore, the bus cycle itself is extended by a software wait or $\overline{\text{RDY}}$ signal.

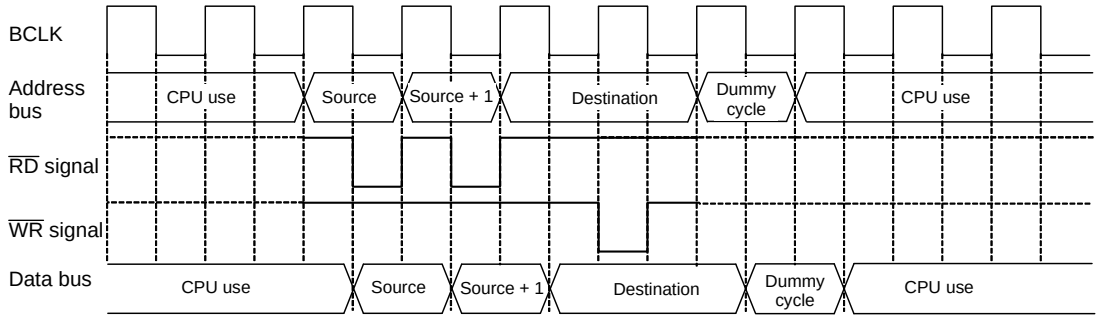
If 16 bits of data are transferred on an 8-bit data bus (input to the BYTE pin is high), the operation is accomplished by transferring 8 bits of data twice. Therefore, this operation requires two bus cycles to read data and two bus cycles to write data. Furthermore, if the DMAC accesses an internal area (internal ROM, internal RAM, or SFR), unlike in the case of the CPU, the DMAC uses the data bus width selected by the BYTE pin.

DMA transfers to and from an external area are affected by the $\overline{\text{RDY}}$ signal. Refer to 11.3.5.6 “$\overline{\text{RDY}}$ Signal” for more information.

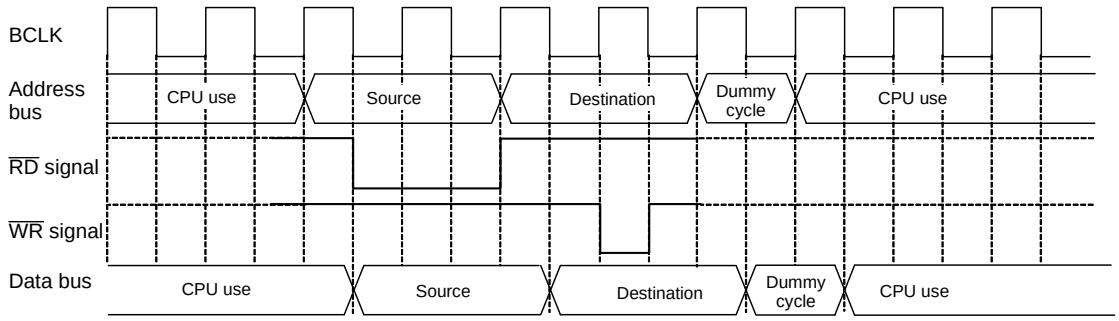
(1) Transfers are performed in 8-bit or 16-bit units, and source of transfer is an even address.



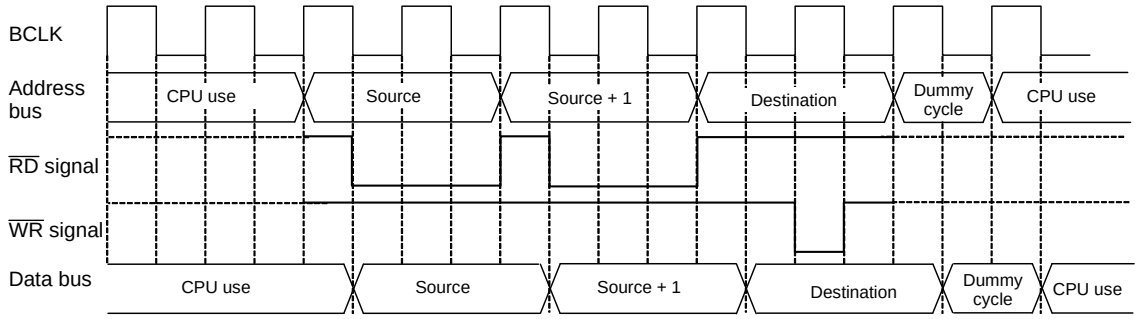
(2) Transfers are performed in 16-bit units, and the source address of transfer is an odd address.



(3) Source read cycle under condition (1) with one wait state inserted



(4) Source read cycle under condition (2) with one wait state inserted



Note :
1. The same timing changes occur with the respective conditions at the destination as at the source.

Figure 16.2 Transfer Cycles for Source Read Operations

16.3.4 DMAC Transfer Cycles

The number of DMA transfer cycles can be calculated as shown below.
Table 16.8 lists the DMAC Transfer Cycles, and Table 16.9 and Table 16.10 list coefficients j and k.

Number of transfer cycles per transfer unit = Number of read cycles × j + Number of write cycles × k

Table 16.8 DMAC Transfer Cycles

Transfer Unit	Bus Width	Access Address	Single-Chip Mode		Memory Expansion Mode Microprocessor Mode	
			No. of Read Cycles	No. of Write Cycles	No. of Read Cycles	No. of Write Cycles
8-bit transfers (DMBIT = 1)	16-bit (BYTE = low)	Even	1	1	1	1
		Odd	1	1	1	1
	8-bit (BYTE = high)	Even	N/A	N/A	1	1
		Odd	N/A	N/A	1	1
16-bit transfers (DMBIT = 0)	16-bit (BYTE = low)	Even	1	1	1	1
		Odd	2	2	2	2
	8-bit (BYTE = high)	Even	N/A	N/A	2	2
		Odd	N/A	N/A	2	2

Table 16.9 Coefficients j and k (1/2)

	Internal Area				External Area		
	Internal ROM, RAM		SFR		Multiplex bus		
	No wait states	Wait states	1 wait state (2)	2 wait states (2)	Wait states (1)		
					1 wait state	2 wait states	3 wait states
j	1	2	2	3	3	3	4
k	1	2	2	3	3	3	4

Notes:
1. Depends on the set value of the CSE register.
2. Depends on the set value of the PM20 bit in the PM2 register.

Table 16.10 Coefficients j and k (2/2)

	External Area							
	Separate bus (1)							
	No wait states	Wait states (2)						
		1wait state (1ϕ + 1ϕ)	2 wait states (1ϕ + 2ϕ)	3 wait states (1ϕ + 3ϕ)	2ϕ + 3ϕ	2ϕ + 4ϕ	3ϕ + 4ϕ	4ϕ + 5ϕ
j	1	2	3	4	5	6	7	9
k	2	2	3	4	5	6	7	9

Notes:
1. When recovery cycle inserted is selected at bits EWR1 and EWR0 in the EWR register, add the recovery cycle.
2. Depends on the set values of registers CSE and EWC.

16.3.5 Single Transfer Mode

In single transfer mode, the transfer stops when the DMAi transfer counter underflows. Figure 16.3 shows Operation Example in Single Transfer Mode.

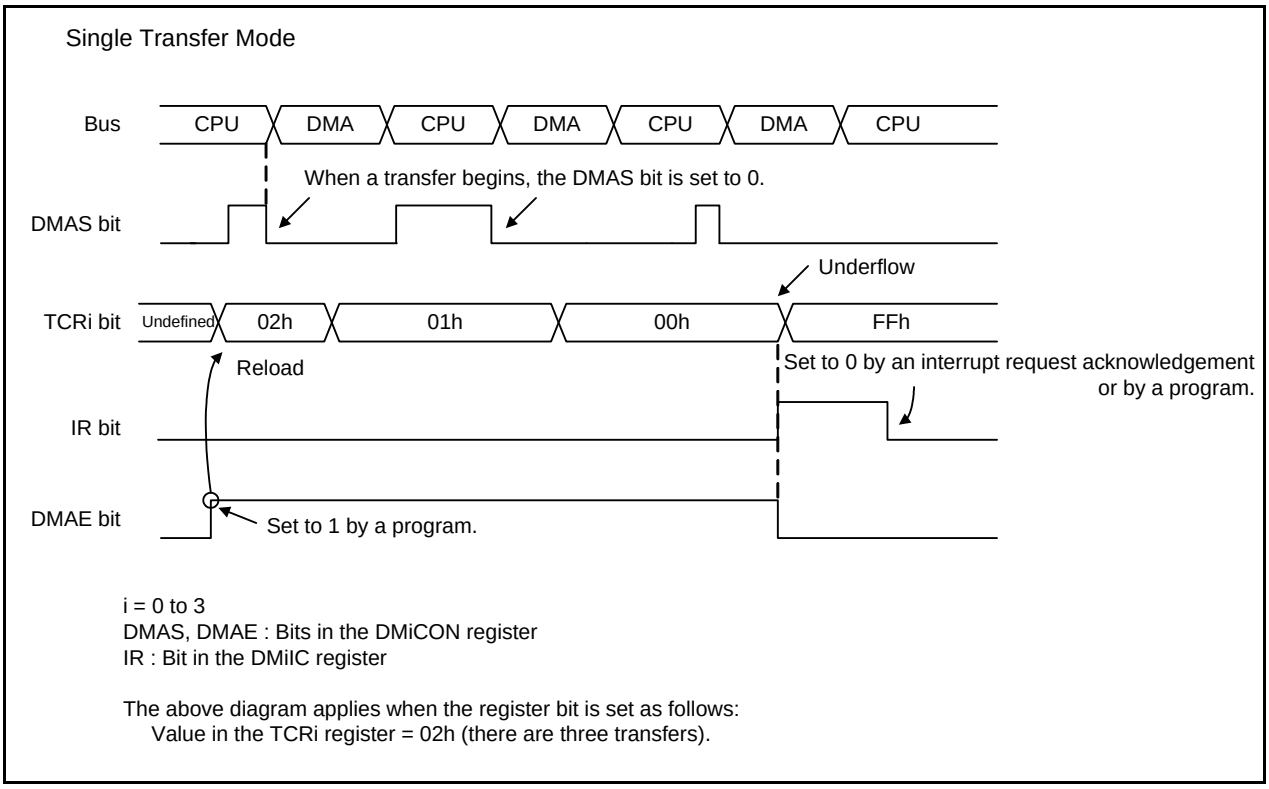


Figure 16.3 Operation Example in Single Transfer Mode

16.3.6 Repeat Transfer Mode

In repeat transfer mode, when the DMAi transfer counter underflows, it is reloaded with the value of the DMAi transfer counter reload register and DMA transfer continues. Figure 16.4 shows Operation Example in Repeat Transfer Mode.

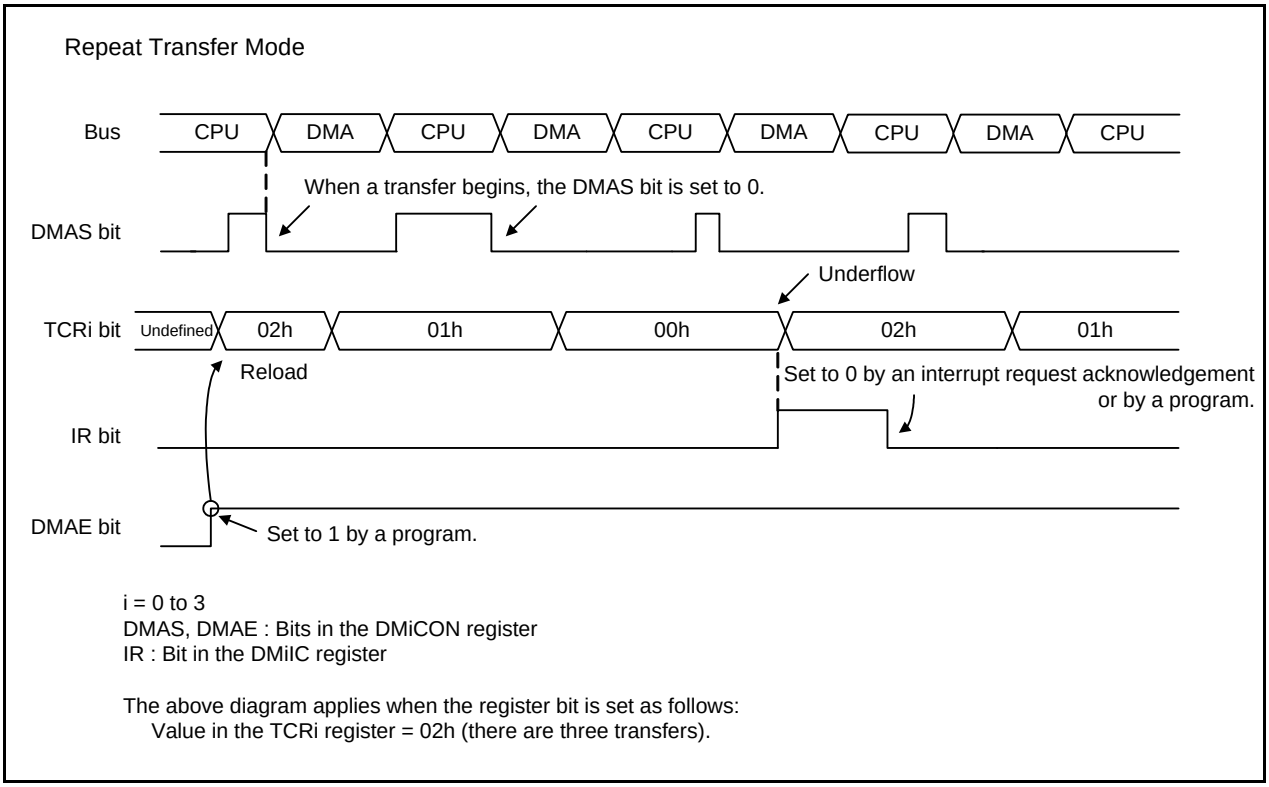


Figure 16.4 Operation Example in Repeat Transfer Mode

16.3.7 Channel Priority and DMA Transfer Timing

If multiple channels among DMA0 to DMA3 are enabled and DMA transfer request signals are detected active in the same sampling period (one period from a falling edge to the next falling edge of BCLK), the DMAS bit on each channel is set to 1 (DMA requested) at the same time. In this case, the DMA requests are arbitrated according to the following channel priority: DMA0 > DMA1 > DMA2 > DMA3. The DMAC operation when DMA0 and DMA1 requests are detected active in the same sampling period is described below. Figure 16.5 shows an example of DMA Transfer by External Sources.

In Figure 16.5, DMA0, which has a high channel priority, is received first to start a transfer when DMA0 and DMA1 requests are generated simultaneously. After one DMA0 transfer is completed, the bus access privilege is returned to the CPU. When the CPU has completed one bus access, a DMA1 transfer starts. After one DMA1 transfer is completed, the bus access privilege is again returned to the CPU.

In addition, DMA requests cannot be incremented since each channel has one DMAS bit. Therefore, when DMA requests, such as DMA1 in Figure 16.5, occur more than once, the DMAS bit is set to 0 after receiving the bus access privilege. The bus access privilege is returned to the CPU when one transfer is completed.

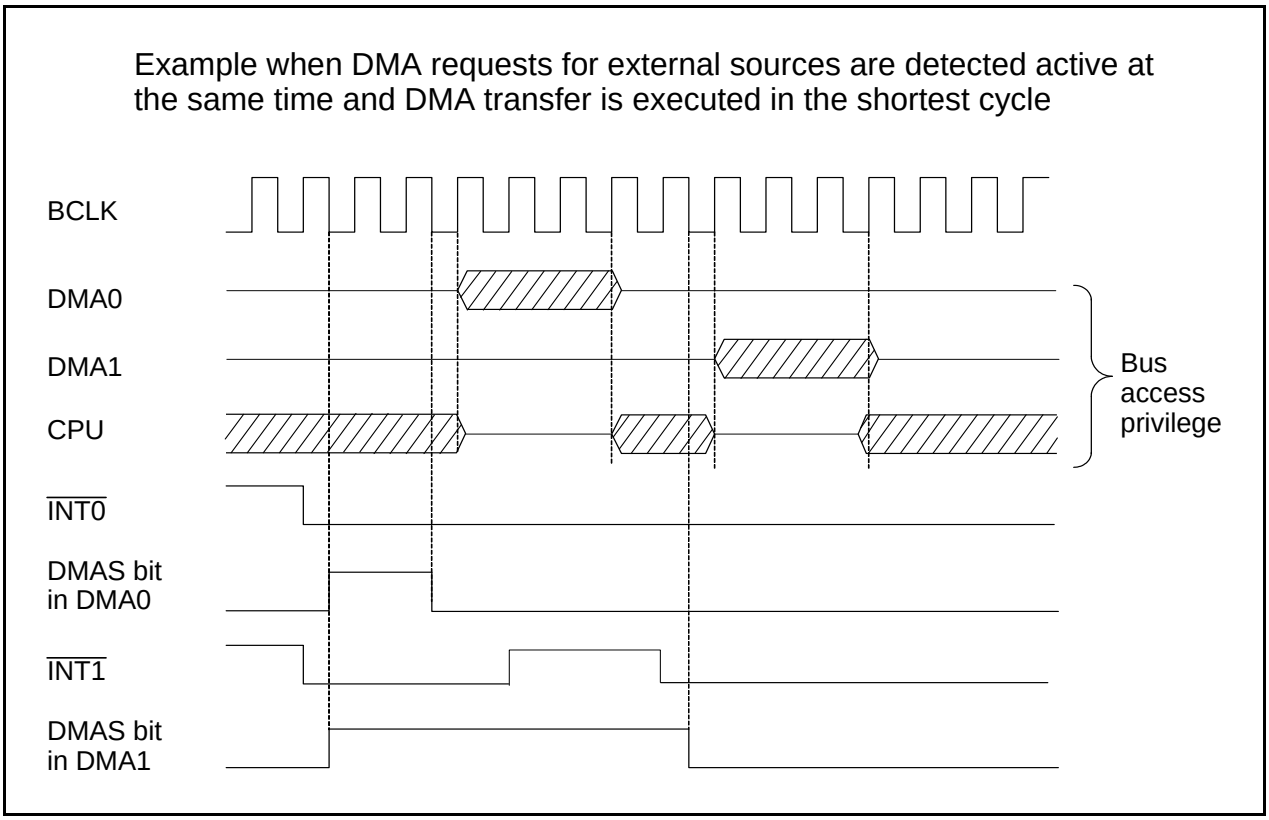


Figure 16.5 DMA Transfer by External Sources

16.4 Interrupts

Refer to operation examples for interrupt request generation timing.
For the details of interrupt control, refer to 14.7 “Interrupt Control”. Table 16.11 lists DMAC Interrupt Related Registers.

Table 16.11 DMAC Interrupt Related Registers

Address	Register Name	Register Symbol	After Reset
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b

When the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested). Therefore, set the DMAS bit to 0 (DMA not requested) after the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed. Refer to 14.13 “Notes on Interrupts”.

16.5 Notes on DMAC

16.5.1 Write to the DMAE Bit in the DMiCON Register (i = 0 to 3)

When both of following conditions are met, follow steps (1) and (2) below.

- Write a 1 (DMAi is in active state) to the DMAE bit when it is 1.
- A DMA request may occur simultaneously when the DMAE bit is being written.

Steps

(1) Write a 1 to the DMAE bit and DMAS bit in the DMiCON register simultaneously (1).
(2) Make sure that the DMAi is in an initialized state (2) in a program.
If the DMAi is not in an initialized state, repeat these two steps.

Notes:

1. The DMAS bit remains unchanged even if a 1 is written. However, if a 0 is written to this bit, it is set to 0 (DMA not requested). In order to prevent the DMAS bit from being modified to 0, 1 should be written to the DMAS bit when 1 is written to the DMAE bit. In this way, the state of the DMAS bit immediately before being written can be maintained.
Similarly, when writing to the DMAE bit with a read-modify-write instruction, write a 1 to the DMAS bit to maintain a DMA request which is generated during execution.
2. Read the TCRi register to verify whether the DMAi is in an initialized state.
If the read value is equal to a value that was written to the TCRi register before DMA transfer start, the DMAi is in an initialized state. (When a DMA request occurs after writing to the DMAE bit, the read value is a value written to the TCRi register minus one.) If the read value is a value in the middle of a transfer, the DMAi is not in an initialized state.

16.5.2 Changing DMA Request Source

When the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested). Set the DMAS bit to 0 (DMA not requested) after the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed.

17. Timer A

Note

The 80-pin package does not have pins TA1IN, TA1OUT, TA2IN and TA2OUT. Do not use functions associated with these pins.

17.1 Introduction

Timers A0 to A4 are provided for timer A. Each timer operates independently of the others. Table 17.1 lists Specifications of Timer A, Table 17.2 lists Differences in Timer A Mode, Figure 17.1 shows Timer A and B Count Sources, Figure 17.2 shows Timer A Configuration, Figure 17.3 shows Timer A Block Diagram, and Table 17.3 lists I/O Ports.

Table 17.1 Specifications of Timer A

Item	Specification
Configuration	16-bit timer × 5
Operating mode	• Timer mode The timer counts an internal count source. • Event counter mode The timer counts pulses from an external device or overflows and underflows of other timers. • One-shot timer mode The timer outputs a pulse only once before it reaches the minimum count 0000h. • Pulse width modulation (PWM) mode The timer outputs pulses of given width and cycle successively. • Programmable output mode The timer outputs a given pulse width of a high-/low- level signal (timers A1, A2, and A4).
Interrupt source	Overflow/underflow × 5

Table 17.2 Differences in Timer A Mode

Item	Timer				
	A0	A1	A2	A3	A4
Event counter mode (two-phase pulse signal processing)	No	No	Yes	Yes	Yes
Programmable output mode	No	Yes	Yes	No	Yes

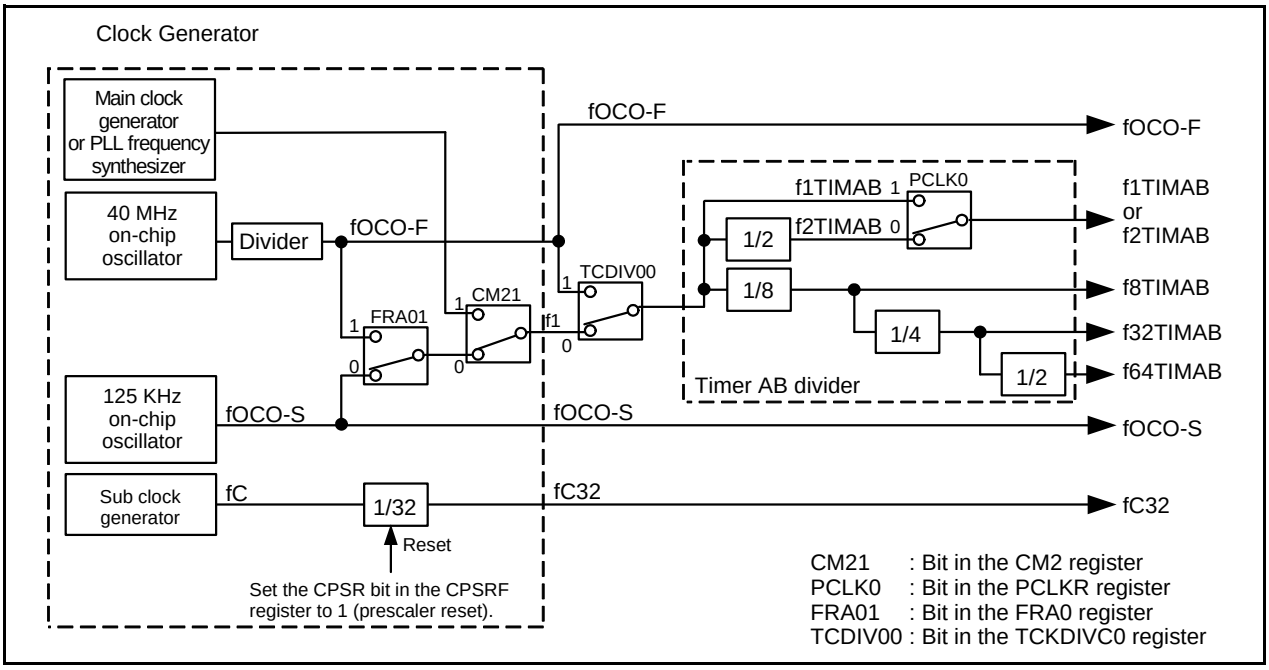


Figure 17.1 Timer A and B Count Sources

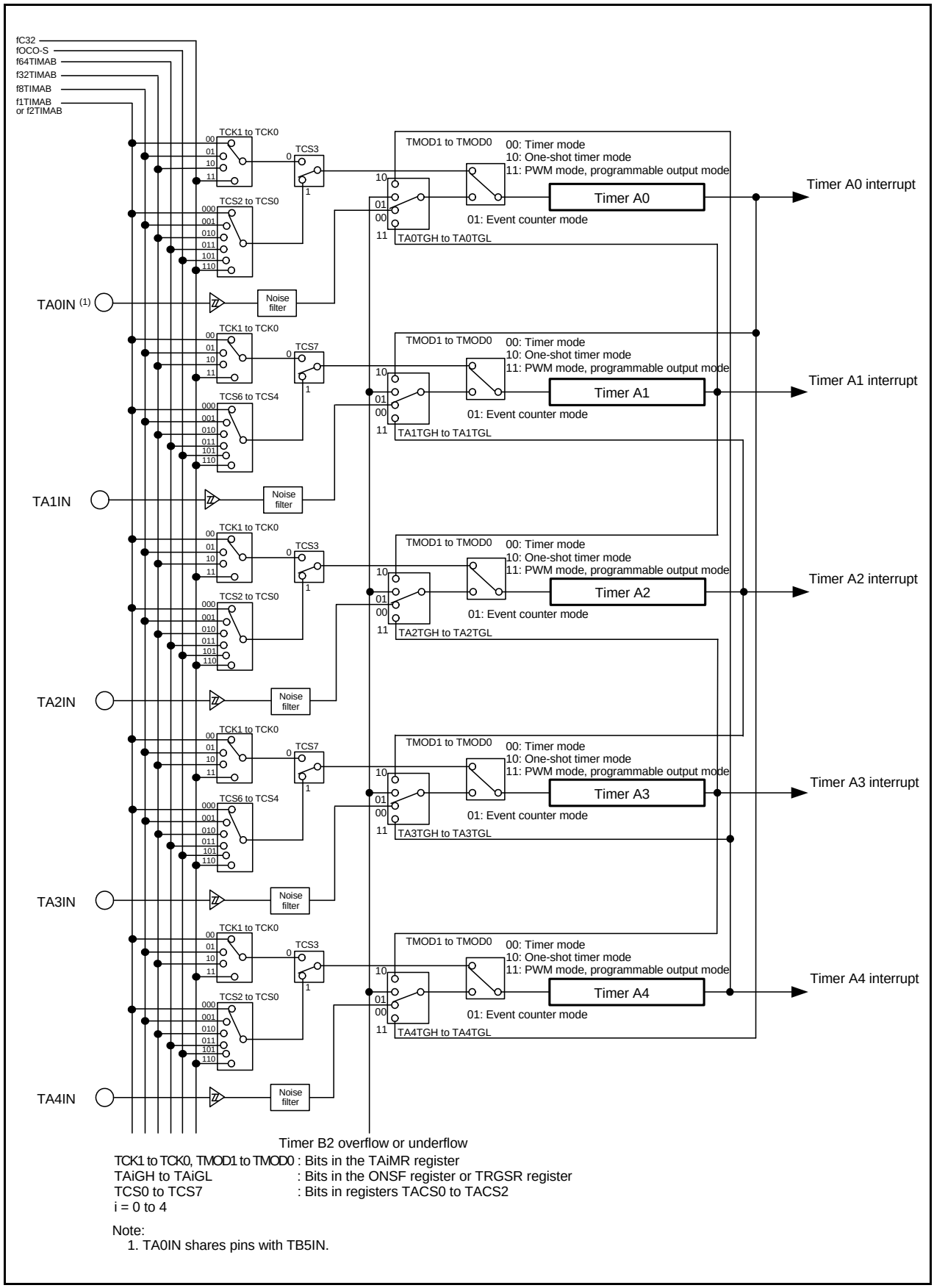
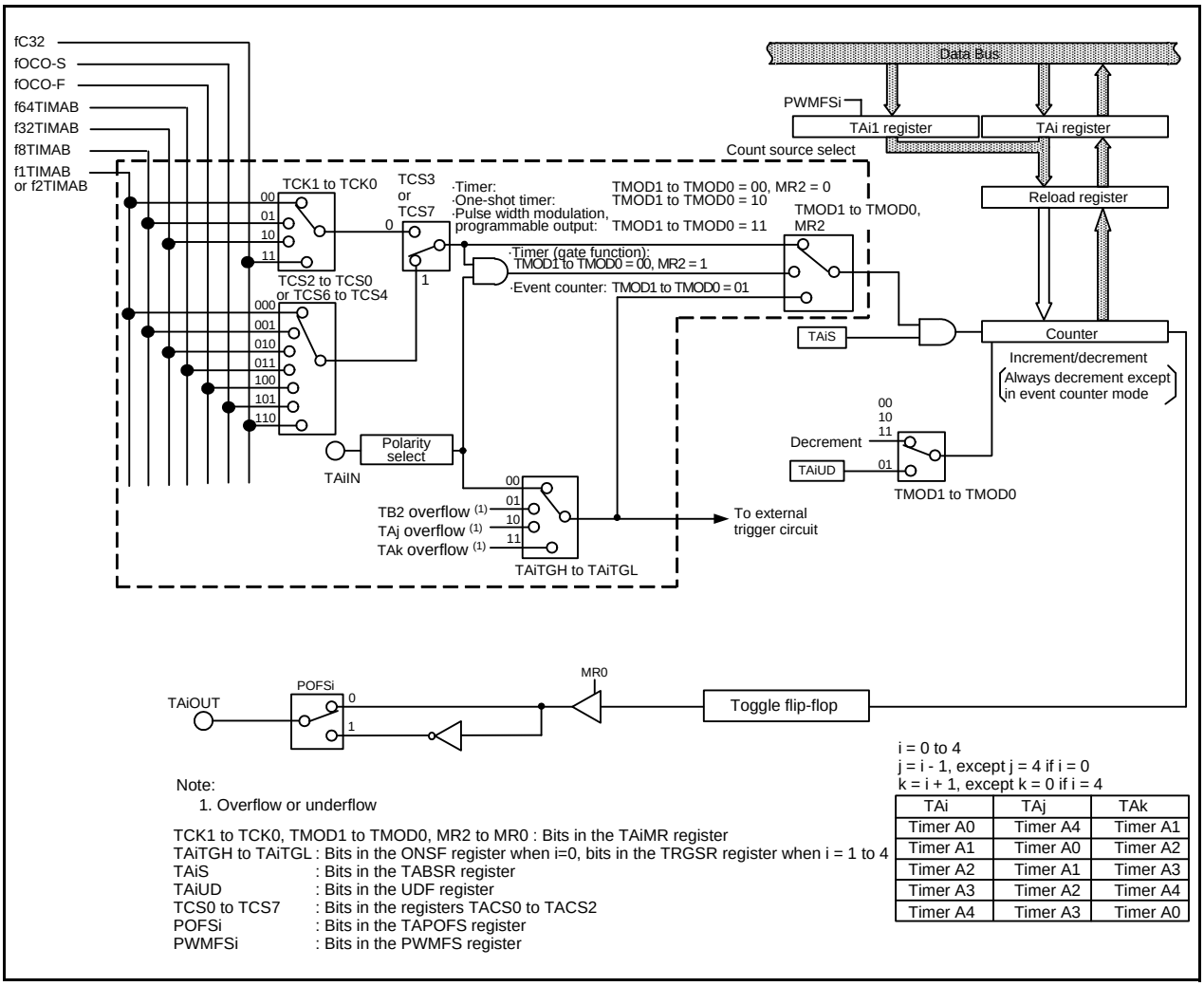


Figure 17.2 Timer A Configuration



Note:
1. Overflow or underflow

TCK1 to TCK0, TMOD1 to TMOD0, MR2 to MR0 : Bits in the TAiMR register
TAiTGH to TAiTGL : Bits in the ONSF register when i=0, bits in the TRGSR register when i = 1 to 4
TAiS : Bits in the TABSR register
TAiUD : Bits in the UDF register
TCS0 to TCS7 : Bits in the registers TACS0 to TACS2
POFSi : Bits in the TAPOFS register
PWMFSi : Bits in the PWMFS register

i = 0 to 4
j = i - 1, except j = 4 if i = 0
k = i + 1, except k = 0 if i = 4

TAi	TAj	TAk
Timer A0	Timer A4	Timer A1
Timer A1	Timer A0	Timer A2
Timer A2	Timer A1	Timer A3
Timer A3	Timer A2	Timer A4
Timer A4	Timer A3	Timer A0

Figure 17.3 Timer A Block Diagram

Table 17.3 I/O Ports

Pin Name	I/O Type	Function
TAiIN	Input (1)	Gate input (timer mode) Count source input (event counter mode) Two-phase signal input (event counter mode (two-phase pulse signal processing)) Trigger input (one-shot timer mode, PWM mode)
TAiOUT	Output (2)	Pulse output (timer mode, event counter mode, one-shot timer mode, PWM mode, and programmable output mode)
	Input (1)	Increment/decrement select input (event counter mode) Two-phase pulse input (event counter mode (two-phase pulse signal processing))
ZP	Input (1)	Z-phase (counter initialization) input (event counter mode (two-phase pulse signal processing))

i = 0 to 4; however, i = 2, 3, 4 for two-phase pulse input, and i = 1, 2, 4 in programmable output mode

Notes:
1. When using pins TAiIN, TAiOUT, and ZP for input, set the port direction bits corresponding to the pins to 0 (input mode).
2. The TA0OUT pin is an N-channel open-drain output.

17.2 Registers

Table 17.4 lists registers associated with timer A.
Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.
Refer to “registers and the setting” in each mode for registers and bit settings.

Table 17.4 Register Structure

Address	Register Name	Register Symbol	After Reset
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D4h	16-Bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
0302h 0303h	Timer A1-1 Register	TA11	XXh XXh
0304h 0305h	Timer A2-1 Register	TA21	XXh XXh
0306h 0307h	Timer A4-1 Register	TA41	XXh XXh
0320h	Count Start Flag	TABSR	00h
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Up/Down Flag	UDF	00h
0326h 0327h	Timer A0 Register	TA0	XXh XXh
0328h 0329h	Timer A1 Register	TA1	XXh XXh
032Ah 032Bh	Timer A2 Register	TA2	XXh XXh
032Ch 032Dh	Timer A3 Register	TA3	XXh XXh
032Eh 032Fh	Timer A4 Register	TA4	XXh XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h

17.2.1 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0		0	0	0		

Symbol	Address	After Reset
PCLKR	0012h	0000 0011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A and B clock select bit (clock source for timers A and B, the dead time timer, and muliti-master I^2C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART2, UART5 to UART7, SI/O3, and SI/O4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0	RW
PCLK5	Clock output function extension bit (valid in single-chip mode)	0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1	RW
— (b7-b6)	Reserved bits	Set to 0	RW

Set the PCLKR register after the PRC0 bit in the PRCR register is set to 1 (write enabled).

17.2.2 Clock Prescaler Reset Flag (CPSRF)

Clock Prescaler Reset Flag

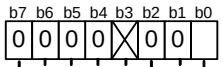
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	X	X	X

Symbol	Address	After Reset
CPSRF	0015h	0XXX XXXXb

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	No register bits. If necessary, set to 0. Read as undefined value		—
CPSR	Clock prescaler reset flag	Setting this bit to 1 initializes the prescaler for the timekeeping clock. (Read as 0)	RW

17.2.3 Timer AB Division Control Register 0 (TCKDIVC0)

Timer AB Division Control Register 0



Symbol: TCKDIVC0 | Address: 01CBh | After Reset: 0000 X000b

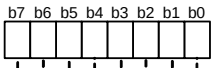
Bit Symbol	Bit Name	Function	RW
TCDIV00	Clock select prior to timer AB division bit	0 : f1 1 : fOCO-F	RW
— (b2-b1)	Reserved bits	Set to 0	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
— (b7-b4)	Reserved bits	Set to 0	RW

TCDIV00 (Clock Select Prior to Timer AB Division Bit) (b1)

Set the TCDIV00 bit while timer A and B stops.
Set the TCDIV00 bit before setting other registers associated with timer A.
After changing the TCDIV00 bit, set other registers associated with timer A again.

17.2.4 Timer A Count Source Select Register i (TACSi) (i = 0 to 2)

Timer A Count Source Select Register 0, Timer A Count Source Select Register 1

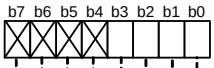


Symbol	Address	After Reset
TACS0 to TACS1	01D0h to 01D1h	00h

Bit Symbol	Bit Name	Function	RW
TCS0	TAi count source select bit	b2 b1 b0 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS1			RW
TCS2			RW
TCS3	TAi count source option specified bit	0 : TCK0, TCK1 enabled, TCS0 to TCS2 disabled 1 : TCK0, TCK1 disabled, TCS0 to TCS2 enabled	RW
TCS4	TAj count source select bit	b6 b5 b4 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS5			RW
TCS6			RW
TCS7	TAj count source option specified bit	0 : TCK0, TCK1 enabled, TCS4 to TCS6 disabled 1 : TCK0, TCK1 disabled, TCS4 to TCS6 enabled	RW

TACS0 register: i = 0, j = 1 TACS1 register: i = 2, j = 3

Timer A Count Source Select Register 2



Symbol	Address	After Reset
TACS2	01D2h	X0h

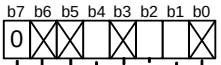
Bit Symbol	Bit Name	Function	RW
TCS0	TA4 count source select bit	b2 b1 b0 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS1			RW
TCS2			RW
TCS3	TA4 count source option specified bit	1 : TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 0 : TCK0 to TCK1 disabled, TCS0 to TCS2 enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value.		—

TCS2-TCS0 (TAi Count Source Select Bit) (b2-b0) (i = 0, 2, 4)
TCS6-TCS4 (TAj Count Source Select Bit) (b6-b4) (i = 1, 3)

Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.

17.2.5 16-Bit Pulse Width Modulation Mode Function Select Register (PWMFS)

16-Bit Pulse Width Modulation Mode Function Select Register



Symbol	Address	After Reset
PWMFS	01D4h	0XX0 X00Xb

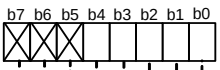
Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. Read as undefined value		—
PWMFS1	Timer A1 programmable output mode select bit	0 : PWM mode 16-bit PWM 1 : Programmable output mode	RW
PWMFS2	Timer A2 programmable output mode select bit	0 : PWM mode 16-bit PWM 1 : Programmable output mode	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
PWMFS4	Timer A4 programmable output mode select bit	0 : PWM mode 16-bit PWM 1 : Programmable output mode	RW
— (b6-b5)	No register bits. If necessary, set to 0. Read as undefined value		—
— (b7)	Reserved bit	Set to 0	RW

PWMFS1 (Timer A1 Programmable Output Mode Select Bit) (b1)
PWMFS2 (Timer A2 Programmable Output Mode Select Bit) (b2)
PWMFS4 (Timer A4 Programmable Output Mode Select Bit) (b4)

The bits are enabled when bits TMOD1 to TMOD0 in the TAiMR register are 11b (PWM mode or programmable output mode), and the MR3 bit in the TAiMR register is 0 (16-bit PWM mode).

17.2.6 Timer A Waveform Output Function Select Register (TAPOFS)

Timer A Waveform Output Function Select Register

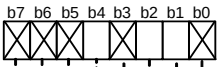


Symbol	Address	After Reset
TAPOFS	01D5h	XXX0 0000b

Bit Symbol	Bit Name	Function	RW
POFS0	TA0OUT output polar control bit	0 : Output waveform high-level active 1 : Output waveform high-level active (output reversed)	RW
POFS1	TA1OUT output polar control bit		RW
POFS2	TA2OUT output polar control bit		RW
POFS3	TA3OUT output polar control bit		RW
POFS4	TA4OUT output polar control bit		RW
— (b7-b5)	No register bits. If necessary, set to 0. Read as undefined value		—

17.2.7 Timer A Output Waveform Change Enable Register (TAOW)

Timer A Output Waveform Change Enable Register



Symbol	Address	After Reset
TAOW	01D8h	XXX0 X00Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. Read as undefined value		—
TA1OW	Timer A1 output waveform change enable bit	0 : Change disabled 1 : Change enabled	RW
TA2OW	Timer A2 output waveform change enable bit	0 : Change disabled 1 : Change enabled	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
TA4OW	Timer A4 output waveform change enable bit	0 : Change disabled 1 : Change enabled	RW
— (b7-b5)	No register bit. If necessary, set to 0. Read as undefined value		—

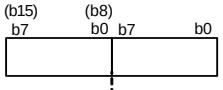
The TAOW register is enabled in programmable output mode.
To change cycles or width of the output waveform, follow the instructions below.

(1)Set the TAiOW bit to 0 (output waveform change disabled). (i = 1, 2, 4)
(2)Write to the TAi register and/or the TAi1 register.
(3)Set the TAiOW bit to 1 (output waveform change enabled).

The updated value is reloaded when the TAiOW bit is 1 (output waveform change enabled) at one cycle before the rising edge of the TAiOUT output (the falling edge when the TOFSi bit is 1). The value before the update is reloaded when the TAiOW bit is 0 (output waveform change disabled).

17.2.8 Timer Ai Register (TAi) (i = 0 to 4)

Timer Ai Register (i = 0 to 4)



Symbol	Address	After Reset
TA0	0327h to 0326h	Undefined
TA1	0329h to 0328h	Undefined
TA2	032Bh to 032Ah	Undefined
TA3	032Dh to 032Ch	Undefined
TA4	032Fh to 032Eh	Undefined

Mode	Function	Setting Range	RW
Timer mode	When n = set value, count cycle: $\frac{(n + 1)}{fj}$	0000h to FFFFh	RW
Event counter mode	When n = set value, FFFFh - n + 1 count (at increment) n + 1 count (at decrement)	0000h to FFFFh	RW
One-shot timer mode	When n = set value, pulse width: $\frac{n}{fj}$	0000h to FFFFh	WO
Pulse width modulation mode (16-bit PWM mode)	When n = set value, PWM period: $\frac{(2^{16} - 1)}{fj}$ PWM pulse width: $\frac{n}{fj}$	0000h to FFFEh	WO
Pulse width modulation mode (8-bit PWM mode)	When n = high-order address set value, m = low-order address set value, PWM period: $\frac{(2^8 - 1) \times (m + 1)}{fj}$ PWM pulse width: $\frac{(m + 1)n}{fj}$	00h to FEh (High-order address) 00h to FFh (Low-order address)	WO
Programmable output mode	When n = set value of TAi1 register, m = set value of TAi register, high-level duration: $\frac{m}{fj}$ low-level duration: $\frac{n}{fj}$	0000h to FFFFh	WO

fj : Count source frequency

Access the register in 16-bit units. Use the MOV instruction to write to the TAi register.

Event Counter Mode

The timer counts pulses from an external device, or the overflows/underflows of other timers.

One-Shot Timer Mode

If the TAi register is set to 0000h, the counter does not work and timer Ai interrupt requests are not generated. Furthermore, if pulse output is selected, no pulses are output from the TAiOUT pin.

Pulse Width Modulation Mode (16-Bit PWM Mode)

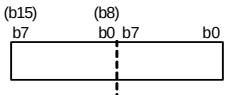
If the TAi register is set to 0000h, the counter does not work, the output level on the TAiOUT pin remains low, and timer Ai interrupt requests are not generated.

Pulse Width Modulation Mode (8-Bit PWM Mode)

This mode operates as 8-bit prescaler (eight low-order bits) and 8-bit pulse width modulator (eight high-order bits). When the eight high-order bits of the TAi register are set to 00h, the counter does not work, the output level on the TAiOUT pin remains low, and timer Ai interrupt requests are not generated.

17.2.9 Timer Ai-1 Register (TAi1) (i = 1, 2, 4)

Timer Ai-1 Register (i = 1, 2, 4)



Symbol	Address	After Reset
TA11	0303h to 0302h	Undefined
TA21	0305h to 0304h	Undefined
TA41	0307h to 0306h	Undefined

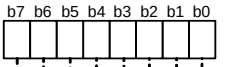
Mode	Function	Setting Range	RW
Programmable output mode	When n = set value of TAi1 register, m = set value of TAi register, high-level duration: $\frac{m}{fj}$ low-level duration: $\frac{n}{fj}$	0001h to FFFFh	WO

fj: Count source frequency

Access the register in 16-bit units. Use the MOV instruction to write to the TAi1 register.

17.2.10 Count Start Flag (TABSR)

Count Start Flag



Symbol	Address	After Reset
TABSR	0320h	00h

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0 : Stop counting 1 : Start counting	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

17.2.11 One-Shot Start Flag (ONSF)

One-Shot Start Flag

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	After Reset
	ONSF	0322h	00h

Bit Symbol	Bit Name	Function	RW
TA0OS	Timer A0 one-shot start flag	The timer starts counting by setting this bit to 1. Read as 0	RW
TA1OS	Timer A1 one-shot start flag		RW
TA2OS	Timer A2 one-shot start flag		RW
TA3OS	Timer A3 one-shot start flag		RW
TA4OS	Timer A4 one-shot start flag		RW
TAZIE	Z-phase input enable bit	0 : Z-phase input disabled 1 : Z-phase input enabled	RW
TA0TGL	Timer A0 event/trigger select bit	b7 b6 0 0 : Input on TA0IN pin selected 0 1 : Timer B2 selected 1 0 : Timer A4 selected 1 1 : Timer A1 selected	RW
TA0TGH			RW

i = 0 to 4

TAiOS (Timer Ai One-Shot Start Flag) (b4-b0) (i = 0 to 4)

This bit is enabled in one-shot timer mode. When the MR2 bit in the TAi register is 0 (TAiOS bit enabled), the timer Ai count starts by setting the TAiOS bit to 1 after setting the TAiS bit in the TABSR register to 1 (start counting).

TAZIE (Z-Phase Input Enable Bit) (b5)

This bit is used in event counter mode (two-phase pulse signal processing) of timer A3. Refer to 17.3.4.3 “Counter Initialization by Two-Phase Pulse Signal Processing” for details.

TA0TGH-TA0TGL (Timer A0 Event/Trigger Select Bit) (b7-b6)

This bit is used to select an event or a trigger of the following modes:

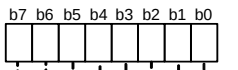
- An event in event counter mode (not using two-phase pulse signal processing)
- A trigger in one-shot timer mode or PWM mode
  The above applies when the MR2 bit in the TA0MR register is 1 (trigger selected by bits TA0TGH to TA0TGL).

The active edge of input signals can be selected by the MR1 bit in the TA0MR register when bits TA0TGH to TA0TGL are 00b.

When bits TA0TGH to TA0TGL are set to 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request of the selected timer is generated. (An event or a trigger occurs while an interrupt is disabled because bits TA0TGH to TA0TGL are not influenced by I flag, IPL, or the interrupt control registers.)

17.2.12 Trigger Select Register (TRGSR)

Trigger Select Register



Symbol	Address	After Reset
TRGSR	0323h	00h

Bit Symbol	Bit Name	Function	RW
TA1TGL	Timer A1 event/trigger select bit	b1 b0 0 0 : Input on TA1IN selected 0 1 : TB2 selected 1 0 : TA0 selected 1 1 : TA2 selected	RW
TA1TGH			RW
TA2TGL	Timer A2 event/trigger select bit	b3 b2 0 0 : Input on TA2IN selected 0 1 : TB2 selected 1 0 : TA1 selected 1 1 : TA3 selected	RW
TA2TGH			RW
TA3TGL	Timer A3 event/trigger select bit	b5 b4 0 0 : Input on TA3IN selected 0 1 : TB2 selected 1 0 : TA2 selected 1 1 : TA4 selected	RW
TA3TGH			RW
TA4TGL	Timer A4 event/trigger select bit	b7 b6 0 0 : Input on TA4IN selected 0 1 : TB2 selected 1 0 : TA3 selected 1 1 : TA0 selected	RW
TA4TGH			RW

TA1TGH-TA1TGL (Timer A1 Event/Trigger Select Bit) (b1-b0)
TA2TGH-TA2TGL (Timer A2 Event/Trigger Select Bit) (b3-b2)
TA3TGH-TA3TGL (Timer A3 Event/Trigger Select Bit) (b5-b4)
TA4TGH-TA4TGL (Timer A4 Event/Trigger Select Bit) (b7-b6)

These bits are used to select an event or a trigger of the following modes:

- Event in event counter mode (not using two-phase pulse signal processing)
- Trigger in one-shot timer mode, PWM mode, or programmable output mode
  The above applies when the MR2 bit in the TAiMR register is 1 (trigger selected by bits TAiTGH to TAiTGL).

The active edge of input signals can be selected by the MR1 bit in the TAiMR register when bits TAiTGH to TAiTGL are 00b.

When bits TAiTGH to TAiTGL are set to 01b, 10b, or 11b, an event or a trigger occurs when an interrupt request of the selected timer is generated. (An event or a trigger occurs while an interrupt is disabled because bits TAiTGH to TAiTGL are not influenced by I flag, IPL, or the interrupt control registers.)

17.2.13 Up/Down Flag (UDF)

Up/Down Flag

b7	b6	b5	b4	b3	b2	b1	b0

Symbol: UDF
Address: 0324h
After Reset: 00h

Bit Symbol	Bit Name	Function	RW
TA0UD	Timer A0 up/down flag	0 : Decrement 1 : Increment	RW
TA1UD	Timer A1 up/down flag		RW
TA2UD	Timer A2 up/down flag		RW
TA3UD	Timer A3 up/down flag		RW
TA4UD	Timer A4 up/down flag		RW
TA2P	Timer A2 two-phase pulse signal processing select bit	0 : Two-phase pulse signal processing disabled 1 : Two-phase pulse signal processing enabled	RW
TA3P	Timer A3 two-phase pulse signal processing select bit		RW
TA4P	Timer A4 two-phase pulse signal processing select bit		RW

TAiUD (Timer Ai Up/Down Flag) (bi) (i = 0 to 4)

Enabled in event counter mode (when not using two-phase pulse signal processing).

TA2P (Timer A2 Two-Phase Pulse Signal Processing Select Bit) (b5)
TA3P (Timer A3 Two-Phase Pulse Signal Processing Select Bit) (b6)
TA4P (Timer A4 Two-Phase Pulse Signal Processing Select Bit) (b7)

Set these bits to 0 when not using two-phase pulse signal processing.

17.2.14 Timer Ai Mode Register (TAiMR) (i = 0 to 4)

Timer Ai Mode Register (i= 0 to 4)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
TA0MR to TA4MR	0336h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode 0 1 : Event counter mode 1 0 : One-shot timer mode 1 1 : Pulse width modulation (PWM) mode or programmable output mode	RW
TMOD1			RW
MR0	Function varies with the operation mode		RW
MR1			RW
MR2			RW
MR3			RW
TCK0	Count source select bit		RW
TCK1			RW

17.3 Operations

17.3.1 Common Operations

17.3.1.1 Operating Clock

The count source for each timer acts as a clock, controlling such timer operations as counting and reloading.

If the conditions to start counting are met, the counter not operating starts counting at the count timing of the first count source. For this reason, a delay exists between when the count start conditions are met and the counter starts counting. Figure 17.4 shows Output Example of One-Shot Timer Mode.

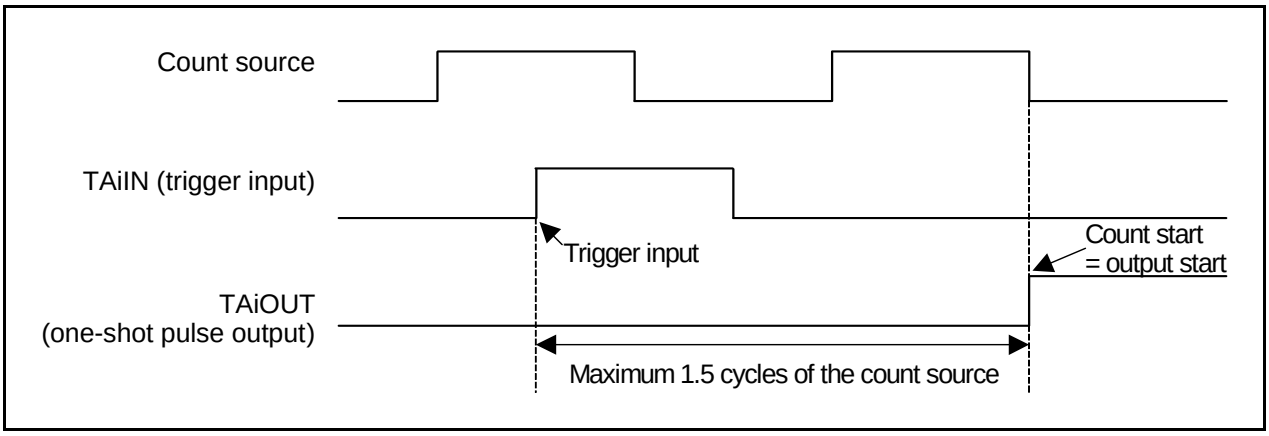


Figure 17.4 Output Example of One-Shot Timer Mode

17.3.1.2 Counter Reload Timing

Timer Ai starts counting from the value (n) set in the TAi register. The TAi register consists of a counter and a reload register. The counter starts decrementing the count source from n, reloads a value in the reload register at the next count source after the value becomes 0000h, and continues decrementing. (When incrementing, the counter reloads a value in the reload register at the next count source after the value becomes FFFFh.)

The value written in the TAi register is reflected in the counter and the reload register at the timings below.

- When the count is stopped
- Between when the count starts and the first count source is input
  A value written to the TAi register is immediately written to the counter and the reload register.

- After the count starts and the first count source is input
  A value written to the TAi register is immediately written to the reload register. The counter continues counting and reloads the value in the reload register at the next count source after the value becomes 0000h (or FFFFh).

17.3.1.3 Count Source

Internal clocks are counted in timer mode, one-shot timer mode, PWM mode, and programmable output mode. (Refer to Figure 17.1 “Timer A and B Count Sources”.) Table 17.5 lists Timer A Count Source.

Timer A, B, and multi-master I^2C-bus interface share the divider. f1 or fOCO-F can be selected before the timer AB divider.

f1 is any of the following. Select f1 by the CM21 bit in the CM2 register and the FRA01 bit in the FRA0 register. (Refer to 8. “Clock Generator”.)

- Main clock divided by 1 (no division)
- PLL clock divided by 1 (no division)
- fOCO-S divided by 1 (no division)
- fOCO-F divided by 1 (no division)

Table 17.5 Timer A Count Source

Count Source	Bit Set Value				Remarks
	PCLK0	TCS3 TCS7	TCS2 to TCS0 TCS4 to TCS6	TCK1 to TCK0	
f1TIMAB	1	0	-	00b	f1 or fOCO-F (1)
		1	000b	-	
f2TIMAB	0	0	-	00b	f1 divided by 2 or
		1	000b	-	fOCO-F divided by 2 (1)
f8TIMAB	-	0	-	01b	f1 divided by 8 or
		1	001b	-	fOCO-F divided by 8 (1)
f32TIMAB	-	0	-	10b	f1 divided by 32 or
		1	010b	-	fOCO-F divided by 32 (1)
f64TIMAB	-	1	011b	-	f1 divided by 64 or fOCO-F divided by 64 (1)
fOCO-F	-	1	100b	-	fOCO-F
fOCO-S	-	1	101b	-	fOCO-S
fC32	-	0	-	11b	fC32
		1	110b	-	

PCLK0: Bit in the PCLKR register
TCS7 to TCS0: Bits in registers TACS0 to TACS2
TCK1 to TCK0: Bits in the TAiMR register (i = 0 to 4)
Note:
1. Select f1 or fOCO-F by the TCDIV00 bit in the TCKDIVC0 register.

17.3.2 Timer Mode

In timer mode, the timer counts a count source generated internally. Table 17.6 lists Specifications of Timer Mode, Table 17.7 lists Registers and the Setting in Timer Mode, and Figure 17.5 shows Operation Example in Timer Mode.

Table 17.6 Specifications of Timer Mode

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operation	• Decrement • When the timer underflows, it reloads the reload register contents and continues counting.
Counter cycles	$\frac{(n+1)}{fj}$ n: set value of TAi register 0000h to FFFFh fj: frequency of count source
Count start condition	Set the TAiS bit in the TABSR register to 1 (start counting).
Count stop condition	Set the TAiS bit to 0 (stop counting).
Interrupt request generation timing	Timer underflow
TAiIN pin function	I/O port or gate input
TAiOUT pin function	I/O port or pulse output
Read from timer	Count value can be read by reading the TAi register.
Write to timer	• When not counting Value written to the TAi register is written to both reload register and counter. • When counting Value written to the TAi register is written to only reload register (transferred to counter when reloaded next).
Selectable functions	• Gate function Counting can be started and stopped by an input signal to the TAiIN pin. • Pulse output function Whenever the timer underflows, the output polarity of the TAiOUT pin is inverted. When the TAiS bit is set to 0 (stop counting), the pin outputs a low-level signal. • Output polarity control While the output polarity of the TAiOUT pin is inverted (the TAiS bit is set to 0 (stop counting)), the pin outputs a high-level signal.

i = 0 to 4

Table 17.7 Registers and the Setting in Timer Mode (1)

Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write a 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select a clock used prior to timer AB frequency dividing.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity when the MR0 bit in the TAiMR register is 1 (pulse output).
TAi1	7 to 0	- (does not need to be set)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TAiTGH to TAiTGL	Set to 00b.
TRGSR	TAiTGH to TAiTGL	Set to 00b.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	7 to 0	Set the counter value.
TAiMR	7 to 0	Refer to the following TAiMR register.

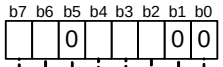
i = 0 to 4

Note:

1. This table does not describe a procedure.

Timer Mode

Timer Ai Mode Register (i = 0 to 4)

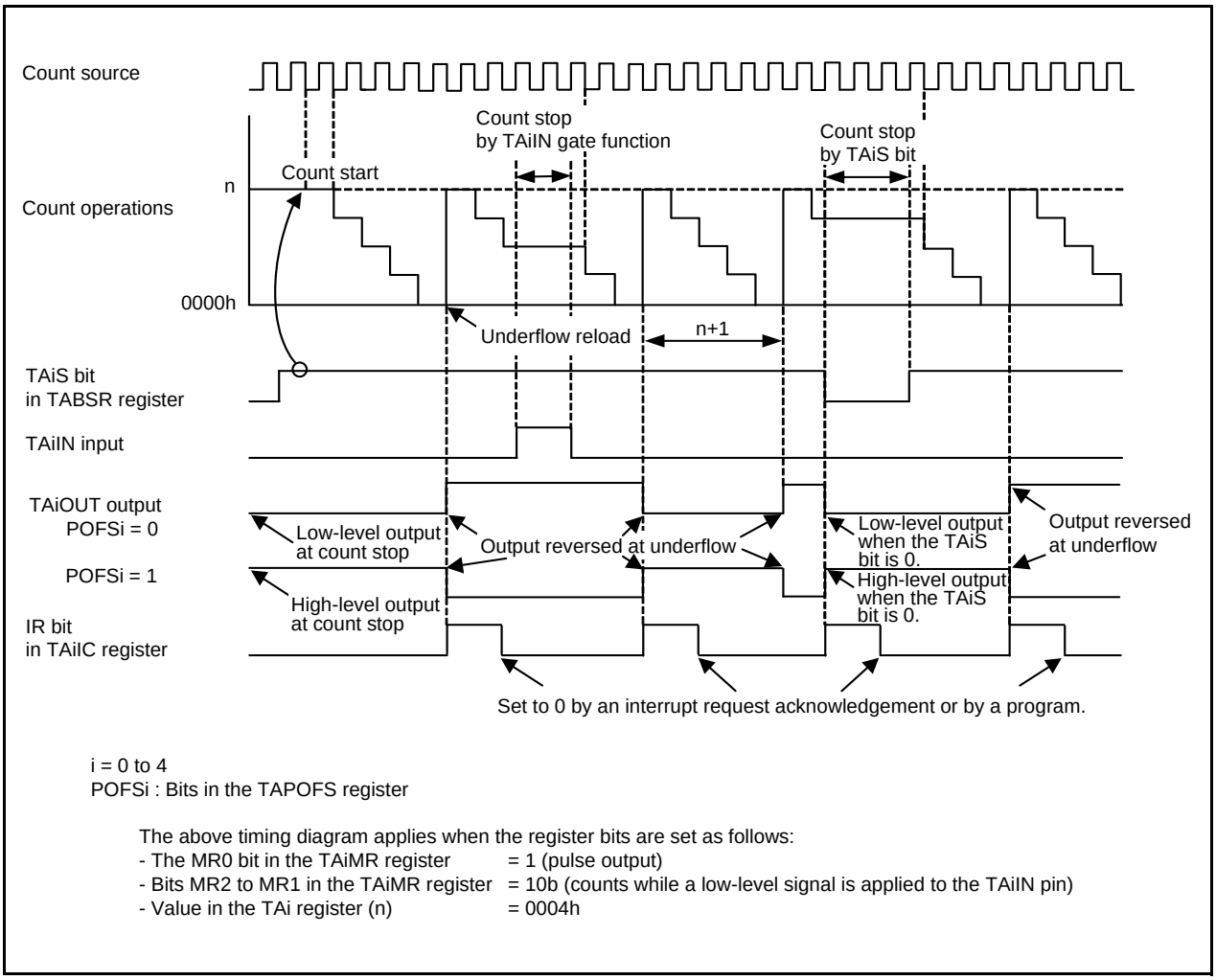


Symbol	Address	After Reset
TA0MR to TA4MR	0336h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW
MR1	Gate function select bit	b4 b3 0 0 : } Gate function not available 0 1 : } (TAiIN pin functions as I/O port) 1 0 : Counts while input on the TAiIN pin is low 1 1 : Counts while input on the TAiIN pin is high	RW
MR2			RW
MR3	Set to 0 in timer mode		RW
TCK0	Count source select bit	b1 b0 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			

TCK1-TCK0 (Count Source Select Bit) (b7-b6)

Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled).
Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.



i = 0 to 4
POFSi : Bits in the TAPOFS register

The above timing diagram applies when the register bits are set as follows:
- The MR0 bit in the TAiMR register = 1 (pulse output)
- Bits MR2 to MR1 in the TAiMR register = 10b (counts while a low-level signal is applied to the TAiIN pin)
- Value in the TAi register (n) = 0004h

Figure 17.5 Operation Example in Timer Mode

17.3.3 Event Counter Mode (When Not Processing Two-Phase Pulse Signal)

In event counter mode, the timer counts pulses from an external device, or overflows/underflows of other timers. Timers A2, A3, and A4 can count two-phase external signals (refer to 17.3.4 “Event Counter Mode (When Processing Two-Phase Pulse Signal)”). Table 17.8 lists Specifications in Event Counter Mode (When Not Processing Two-Phase Pulse Signal). Table 17.9 lists Registers and the Setting in Event Counter Mode (When Not Processing Two-Phase Pulse Signal). Figure 17.6 shows Operation Example in Event Counter Mode.

Table 17.8 Specifications in Event Counter Mode (When Not Processing Two-Phase Pulse Signal)

Item	Specification
Count source	• External signals input to the TAiIN pin (active edge can be selected by a program) • Timer B2 overflows or underflows • Timer Aj overflows or underflows (j = i - 1, except j = 4 if i = 0) • Timer Ak overflows or underflows (k = i + 1, except k=0 if i = 4)
Count operations	• Increment or decrement can be selected by a program. • When the timer overflows or underflows, it reloads the reload register contents and continues counting. When operating in free-running mode, the timer continues counting without reloading.
Number of counts	• FFFFh - n + 1 for increment • n + 1 for decrement n: set value of the TAi register 0000h to FFFFh
Count start condition	Set the TAiS bit in the TABSR register to 1 (start counting).
Count stop condition	Set the TAiS bit to 0 (stop counting).
Interrupt request generation timing	Timer overflow or underflow
TAiIN pin function	I/O port or count source input
TAiOUT pin function	I/O port or pulse output
Read from timer	Count value can be read by reading the TAi register.
Write to timer	• When not counting Value written to the TAi register is written to both reload register and counter. • When counting Value written to the TAi register is written to only reload register (transferred to counter when reloaded next).
Selectable functions	• Free-run count function Even when the timer overflows or underflows, the reload register content is not reloaded. • Pulse output function Whenever the timer underflows or underflows, the output polarity of the TAiOUT pin is inverted. When the TAiS bit is set to 0 (stop counting), the pin outputs a low-level signal. • Output polarity control While the output polarity of the TAiOUT pin is inverted (the TAiS bit is set to 0 (stop counting)), the pin outputs a high-level signal.

i = 0 to 4

Table 17.9 Registers and the Setting in Event Counter Mode (When Not Processing Two-Phase Pulse Signal) (1)

Register	Bit	Setting
PCLKR	PCLK0	Set to 1.
CPSRF	CPSR	Write a 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Set to 0.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Set to 00b.
TAPOFS	POFSi	Select the output polarity when the MR0 bit in the TAiMR register is 1 (pulse output).
TAi1	7 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TAiTGH to TAiTGL	Select a count source.
TRGSR	TAiTGH to TAiTGL	Select a count source.
UDF	TAiUD	Select a count operation.
	TAiP	Set to 0.
TAi	7 to 0	Set the counter value.
TAiMR	7 to 0	Refer to the following TAiMR register.

i = 0 to 4

Note:

1. This table does not describe a procedure.

Event Counter Mode (When Not Using Two-Phase Pulse Signal Processing)

Timer Ai Mode Register (i = 0 to 4)

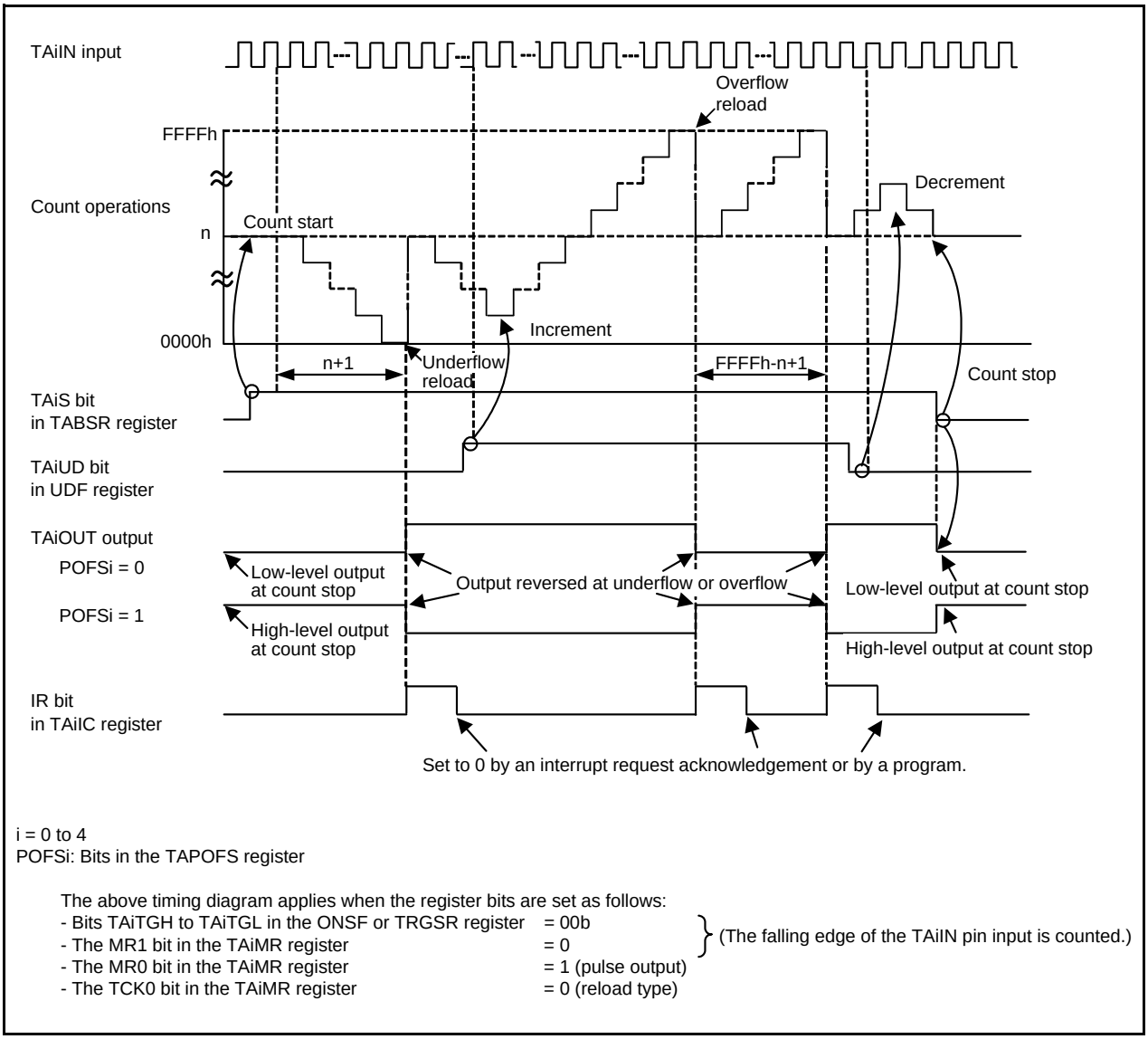
b7	b6	b5	b4	b3	b2	b1	b0
		0	0			0	1

Symbol	Address	After Reset
TA0MR to TA4MR	0336h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 1 : Event counter mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : Pulse is not output (TAiOUT pin functions as I/O port) 1 : Pulse is output (TAiOUT pin functions as pulse output pin)	RW
MR1	Count polarity select bit	0 : Counts falling edge of external signal 1 : Counts rising edge of external signal	RW
MR2	Set to 0 in event counter mode		RW
MR3	Set to 0 in event counter mode		RW
TCK0	Count operation type select bit	0 : Reload type 1 : Free-run type	RW
TCK1	Can be 0 or 1 when not using two-phase pulse signal processing		RW

MR1 (Count Polarity Select Bit) (b3)

Valid when bits TAiTGH to TAiTGL in the ONSF or TRGSR register are 00b (TAiIN pin input).



i = 0 to 4
POFSi: Bits in the TAPOFS register

The above timing diagram applies when the register bits are set as follows:
- Bits TAiTGH to TAiTGL in the ONSF or TRGSR register = 00b
- The MR1 bit in the TAiMR register = 0
- The MR0 bit in the TAiMR register = 1 (pulse output)
- The TCK0 bit in the TAiMR register = 0 (reload type)

} (The falling edge of the TAiIN pin input is counted.)

Figure 17.6 Operation Example in Event Counter Mode

17.3.4 Event Counter Mode (When Processing Two-Phase Pulse Signal)

Timers A2, A3, and A4 can be used to count two-phase pulse signals. Table 17.10 lists Specifications of Event Counter Mode (When Processing Two-Phase Pulse Signal with Timers A2, A3, and A4). Table 17.11 lists Registers and the Setting in Event Counter Mode (When Processing Two-Phase Pulse Signal).

Table 17.10 Specifications of Event Counter Mode (When Processing Two-Phase Pulse Signal with Timers A2, A3, and A4)

Item	Specification
Count source	Two-phase pulse signals input to the TAiIN or TAiOUT pin
Count operations	• Increment or decrement can be selected by a two-phase pulse signal. • When the timer overflows or underflows, it reloads the reload register contents and continues counting. When operating in free-running mode, the timer continues counting without reloading.
Number of counts	• FFFFh - n + 1 for increment • n + 1 for decrement n: set value of the TAi register 0000h to FFFFh
Count start condition	Set the TAiS bit in the TABSR register to 1 (start counting).
Count stop condition	Set the TAiS bit to 0 (stop counting).
Interrupt request generation timing	Timer overflow or underflow
TAiIN pin function	Two-phase pulse input
TAiOUT pin function	Two-phase pulse input
Read from timer	Count value can be read by reading timer A2, A3, or A4 register.
Write to timer	• When not counting Value written to the TAi register is written to both reload register and counter. • When counting Value written to the TAi register is written to only reload register (transferred to counter when reloaded next).
Selectable functions	• Select normal or multiply-by-4 processing operation (timer A3). • Counter initialization by Z-phase input (timer A3) The timer count value is initialized to 0 by Z-phase input.

i = 2 to 4

Table 17.11 Registers and the Setting in Event Counter Mode (When Processing Two-Phase Pulse Signal) (1)

Register	Bit	Setting
PCLKR	PCLK0	Set to 1.
CPSRF	CPSR	Write a 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Set to 0.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Set to 00b.
TAPOFS	POFSi	Set to 0.
TAi1	7 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 1 when using Z-phase input at timer A3.
	TAiTGH to TAiTGL	Set to 00b.
TRGSR	TAiTGH to TAiTGL	Set to 00b.
UDF	TAiUD	Set to 0.
	TAiP	Set to 1.
TAi	7 to 0	Set the counter value.
TAiMR	7 to 0	Refer to the following TAiMR register.

i = 2 to 4

Note:

1. This table does not describe a procedure.

Event Counter Mode (When Using Two-Phase Pulse Signal Processing)
Timer Ai Mode Register (i = 2 to 4)

b7	b6	b5	b4	b3	b2	b1	b0
		0	1	0	0	0	1

Symbol	Address	After Reset
TA2MR to TA4MR	0338h to 033Ah	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 1 : Event counter mode	RW
TMOD1			RW
MR0	Set to 0 to use two-phase signal processing		RW
MR1	Set to 0 to use two-phase signal processing		RW
MR2	Set to 1 to use two-phase signal processing		RW
MR3	Set to 0 to use two-phase signal processing		RW
TCK0	Count operation type select bit	0 : Reload type 1 : Free-run type	RW
TCK1	Two-phase pulse signal processing operation type select bit	0 : Normal processing operation 1 : Multiply-by-4 processing operation	RW

TCK1 (Two-Phase Pulse Signal Processing Operation Type Select Bit) (b7)

The TCK1 bit can be set only for timer A3 mode register. No matter how this bit is set, timers A2 and A4 always operate in normal processing mode and multiply-by-4 processing mode, respectively.

17.3.4.1 Normal Processing

The timer increments rising edges or decrements falling edges on the TAjIN pin when input signals on the TAjOUT (j = 2, 3) pin is high level. Figure 17.7 shows Normal Processing.

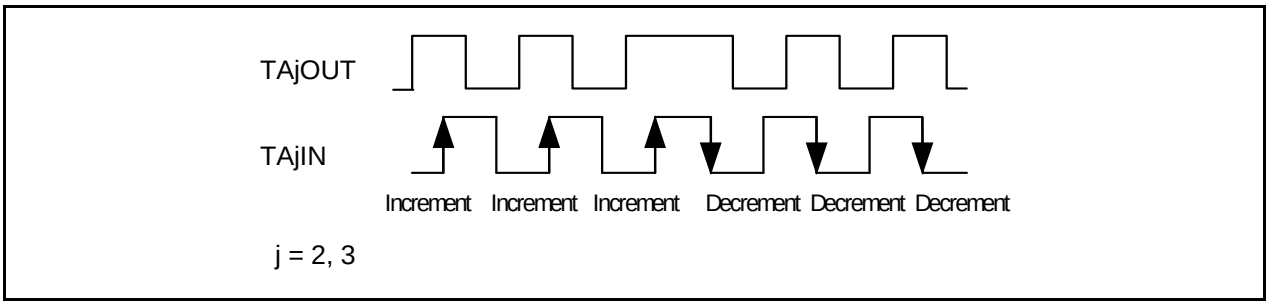


Figure 17.7 Normal Processing

17.3.4.2 Multiply-by-4 Processing

If the phase relationship is such that TAkIN pin goes high when the input signal on the TAkOUT pin (k = 3, 4) is high, the timer increments rising and falling edges on pins TAkOUT and TAkIN. If the phase relationship is such that the TAkIN pin goes low when the input signal on the TAkOUT pin is high, the timer decrements rising and falling edges on pins TAkOUT and TAkIN. Figure 17.8 shows Multiply-by-4 Processing.

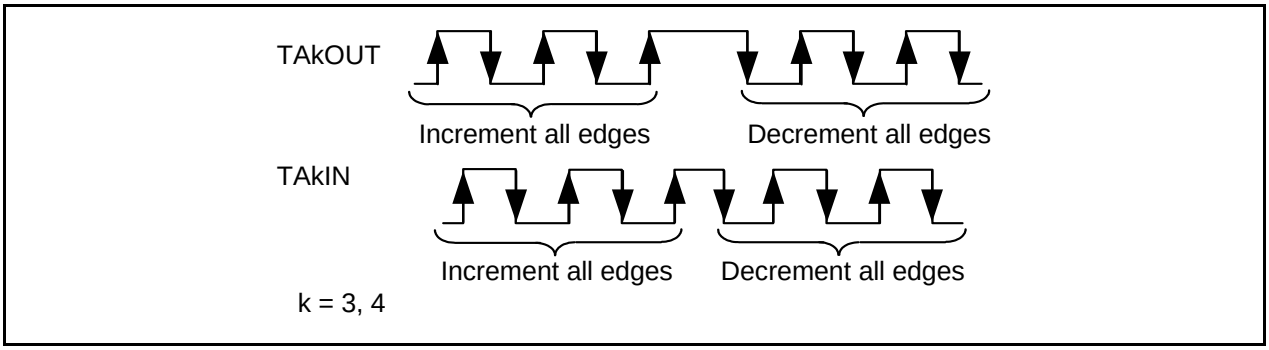


Figure 17.8 Multiply-by-4 Processing

17.3.4.3 Counter Initialization by Two-Phase Pulse Signal Processing

This function initializes the timer count value to 0000h by Z-phase (counter initialization) input during two-phase pulse signal processing.

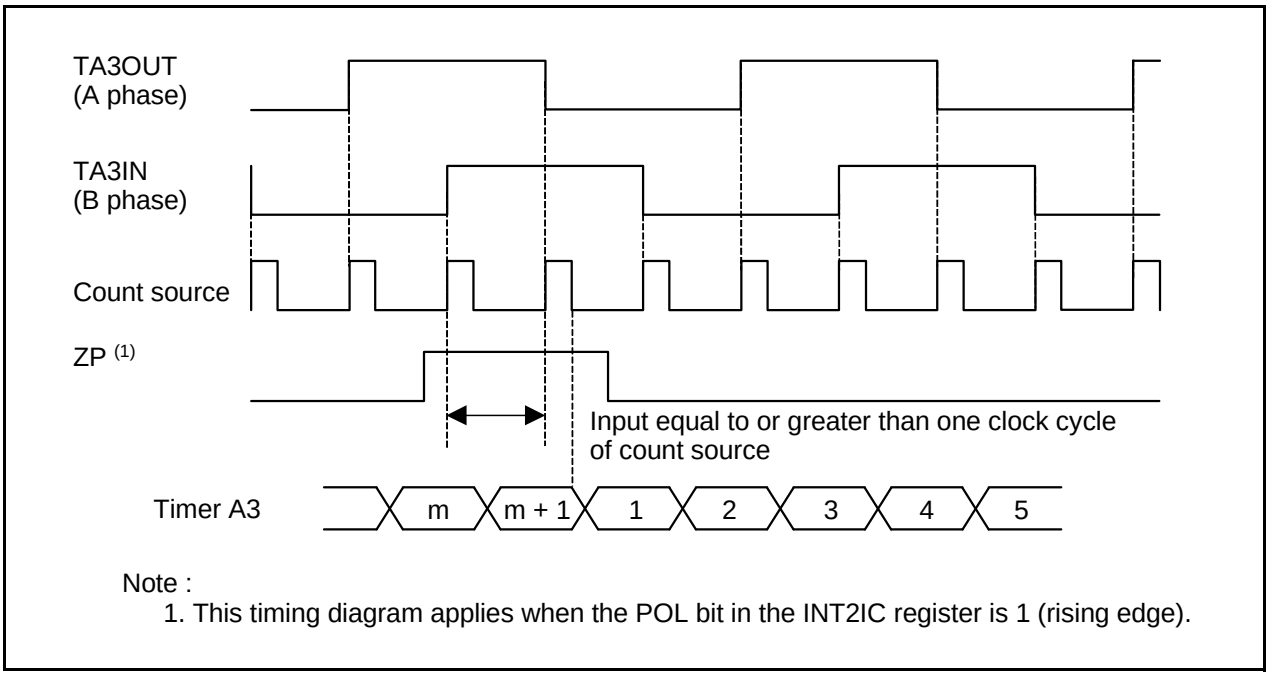
This function can only be used in timer A3 event counter mode during two-phase pulse signal processing, free-running type, multiply-by-4 processing, with Z-phase entered from the ZP pin.

Counter initialization by Z-phase input is enabled by writing 0000h to the TA3 register and setting the TAZIE bit in the ONSF register to 1 (Z-phase input enabled).

Counter initialization is accomplished by Z-phase input edge detection. The rising or falling edge can be selected as the active edge by using the POL bit in the INT2IC register. The Z-phase pulse width applied to the $\overline{ZP}$ pin must be equal to or greater than one clock cycle of timer A3 count source.

The counter is initialized at the next count timing after recognizing Z-phase input. Figure 17.9 shows the Relationship between the Two-Phase Pulse (A-Phase and B-Phase) and the Z-Phase.

If timer A3 overflow or underflow coincides with counter initialization by Z-phase input, a timer A3 interrupt request is generated twice in succession. Do not use the timer A3 interrupt when using this function.



Note :
1. This timing diagram applies when the POL bit in the INT2IC register is 1 (rising edge).

Figure 17.9 Relationship between the Two-Phase Pulse (A-Phase and B-Phase) and the Z-Phase

17.3.5 One-Shot Timer Mode

In one-shot timer mode, the timer is activated only once by one trigger. When the trigger occurs, the timer starts and continues operating for a given period. Table 17.12 lists Specifications of One-Shot Timer Mode. Table 17.13 lists Registers and the Setting in One-Shot Timer Mode. Figure 17.10 shows Operation Example in One-Shot Timer Mode.

Table 17.12 Specifications of One-Shot Timer Mode

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Decrement • When the counter reaches 0000h, it stops counting after reloading a new value. • When a trigger occurs while counting, the timer reloads a new value and restarts counting.
Pulse width	$\frac{n}{fj}$  n: set value of the TAi register 0000h to FFFFh However, the counter does not work if 0000h is set. fj: count source frequency
Count start condition	The TAiS bit in the TABSR register is 1 (start counting) and one of the following triggers occurs: • External trigger input from the TAiIN pin • Timer B2 overflow or underflow • Timer Aj overflow or underflow (j = i - 1, except j = 4 if i = 0) • Timer Ak overflow or underflow (k = i + 1, except k = 0 if i = 4) • The TAiOS bit in the ONSF register is set to 1 (timer starts).
Count stop condition	• When the counter is reloaded after reaching 0000h • The TAiS bit is set to 0 (stop counting)
Interrupt request generation timing	When the counter reaches 0000h
TAiIN pin function	I/O port or trigger input
TAiOUT pin function	I/O port or pulse output
Read from timer	An undefined value is read by reading the TAi register.
Write to timer	• When not counting and until the first count source is input after counting starts, the value written to the TAi register is written to both reload register and counter. • When counting (after first count source input), the value written to the TAi register is written to only the reload register (transferred to the counter when reloaded next).
Selectable functions	• Pulse output function The timer outputs a low-level signal when not counting and a high-level signal when counting. • Output polarity control The output polarity of TAiOUT pin is inverted. (While the TAiS bit is set to 0 (stop counting), the pin outputs a high-level signal.)

i = 0 to 4

Table 17.13 Registers and the Setting in One-Shot Timer Mode (1)

Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write a 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select a clock used prior to timer AB frequency dividing.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity when the MR0 bit in the TAiMR register is 1 (pulse output).
TAi1	7 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 1 when starting counting while the MR2 bit is 0.
	TAZIE	Set to 0.
	TAiTGH to TAiTGL	Select a count trigger.
TRGSR	TAiTGH to TAiTGL	Select a count trigger.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	7 to 0	Set a high-level pulse width. (2)
TAiMR	7 to 0	Refer to the following TAiMR register.

i = 0 to 4

Notes:
1. This table does not describe a procedure.
2. This applies when the POFSi bit in the TAPOFS register is 0.

One-Shot Timer Mode
Timer Ai Mode Register (i = 0 to 4)

b7	b6	b5	b4	b3	b2	b1	b0
		0				1	0

Symbol	Address	After Reset
TA0MR to TA4MR	0336h to 033Ah	00h

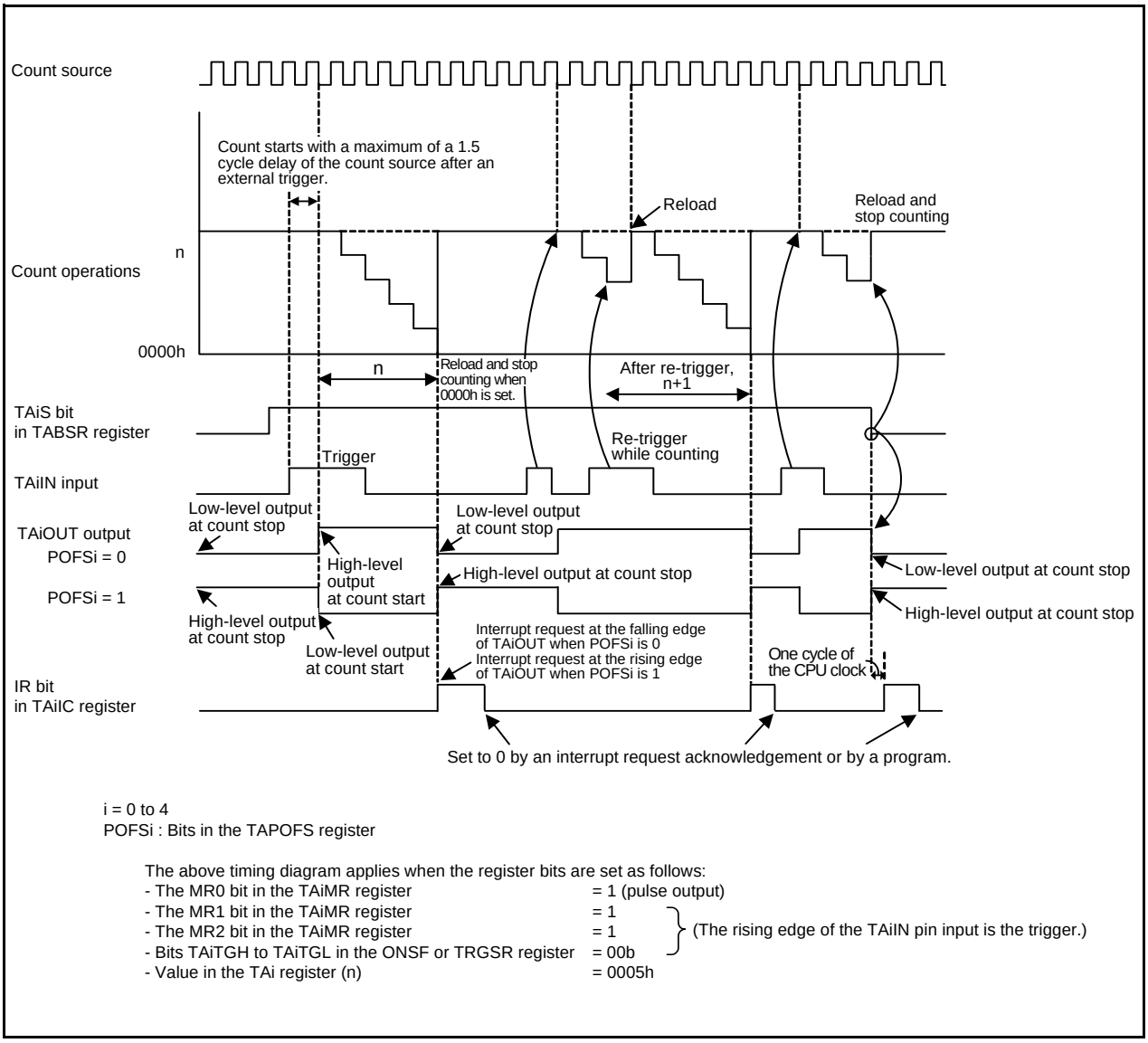
Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 0 : One-shot timer mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW
MR1	External trigger select bit	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW
MR2	Trigger select bit	0 : TAiOS bit enabled 1 : Selected by bits TAiTGH and TAiTGL	RW
MR3	Set to 0 in one-shot timer mode		RW
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			

MR1 (External Trigger Select Bit) (b3)

Valid when the MR2 bit is set to 1 and bits TAiTGH to TAiTGL in the ONSF register or TRGSR register are set to 00b (TAiIN pin input).

TCK1-TCK0 (Count Source Select Bit) (b7-b6)

Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled). Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.



i = 0 to 4
POFSi : Bits in the TAPOFS register

The above timing diagram applies when the register bits are set as follows:
- The MR0 bit in the TAiMR register = 1 (pulse output)
- The MR1 bit in the TAiMR register = 1
- The MR2 bit in the TAiMR register = 1
- Bits TAiTGH to TAiTGL in the ONSF or TRGSR register = 00b
- Value in the TAi register (n) = 0005h

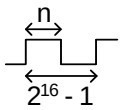
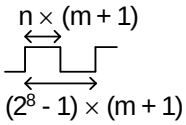
} (The rising edge of the TAiIN pin input is the trigger.)

Figure 17.10 Operation Example in One-Shot Timer Mode

17.3.6 Pulse Width Modulation (PWM) Mode

In PWM mode, the timer outputs pulses of a given width in succession. The counter functions as either 16-bit pulse width modulator or 8-bit pulse width modulator. Table 17.14 lists Specifications of PWM Mode. Table 17.15 lists Registers and the Setting in PWM Mode. Figure 17.11 and Figure 17.12 show Operation Example in 16-Bit Pulse Width Modulation Mode and Operation Example in 8-Bit Pulse Width Modulation Mode, respectively.

Table 17.14 Specifications of PWM Mode

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Decrement (operating as an 8-bit or a 16-bit pulse width modulator) • The timer reloads a new value at a rising edge of PWM pulse and continues counting. • The timer is not affected by a trigger that occurs during counting.
16-bit PWM	• Pulse width $\frac{n}{fj}$  • Cycle time $\frac{(2^{16}-1)}{fj}$ n: set value of the TAi register fj: count source frequency
8-bit PWM	• Pulse width $\frac{n \times (m+1)}{fj}$  • Cycle time $\frac{(2^8-1) \times (m+1)}{fj}$ m: set value of the TAi register low-order address n: set value of the TAi register high-order address fj: count source frequency
Count start condition	• The TAiS bit of the TABSR register is set to 1 (start counting). • The TAiS bit is 1 and external trigger input from the TAiIN pin • The TAiS bit is 1 and one of the following external triggers occurs Timer B2 overflow or underflow Timer Aj overflow or underflow (j = i - 1, except j = 4 if i = 0) Timer Ak overflow or underflow (k = i + 1, except k = 0 if i = 4)
Count stop condition	The TAiS bit is set to 0 (stop counting).
Interrupt request generation timing	On the falling edge of the PWM pulse
TAiIN pin function	I/O port or trigger input
TAiOUT pin function	Pulse output
Read from timer	An indeterminate value is read by reading the TAi register.
Write to timer	• When not counting Value written to the TAi register is written to both reload register and counter. • When counting Value written to the TAi register is written to only reload register (transferred to counter when reloaded next).
Selectable functions	• Output polarity control The output polarity of TAiOUT pin is inverted. (While the TAiS bit is set to 0 (stop counting), the pin outputs a high-level signal.)

i = 0 to 4

Table 17.15 Registers and the Setting in PWM Mode (1)

Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write a 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select a clock used prior to timer AB frequency dividing.
PWMFS	PWMFSi	Set to 0.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity.
TAi1	7 to 0	- (setting unnecessary)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TAiTGH to TAiTGL	Select a count trigger.
TRGSR	TAiTGH to TAiTGL	Select a count trigger.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	7 to 0	Select the pulse width and cycles.
TAiMR	7 to 0	Refer to the following TAiMR register.

i = 0 to 4

Note:

1. This table does not describe a procedure.

Pulse Width Modulation (PWM) Mode
Timer Ai Mode Register (i = 0 to 4)

b7	b6	b5	b4	b3	b2	b1	b0
						1	1

Symbol	Address	After Reset
TA0MR to TA4MR	0336h to 033Ah	00h

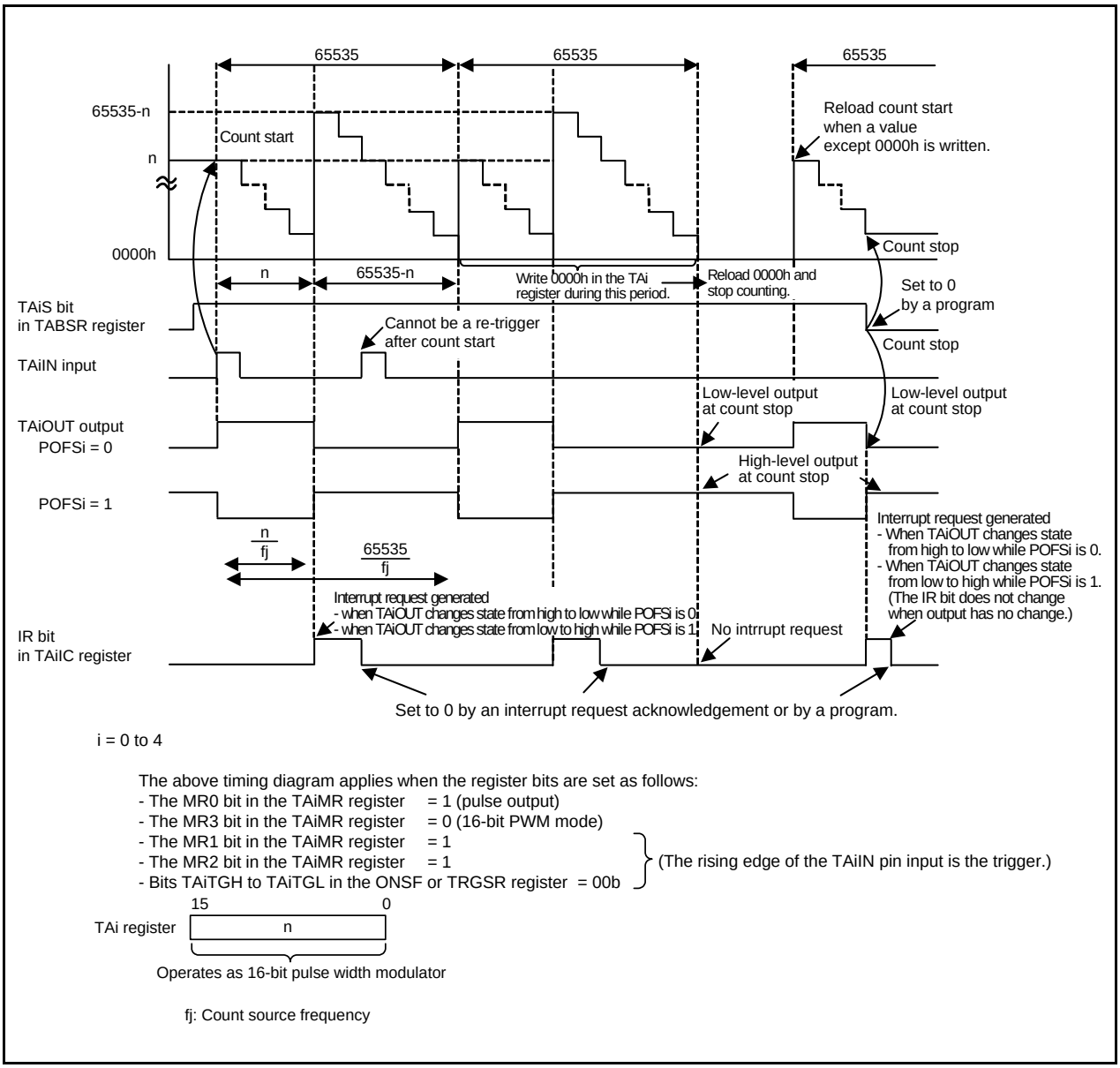
Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 1 : PWM mode or programmable output mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW
MR1	External trigger select bit	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW
MR2	Trigger select bit	0 : Write 1 to the TAiS bit in the TABSR register 1 : Selected by bits TAiTGH to TAiTGL	RW
MR3	16/8-bit PWM mode select bit	0 : 16-bit PWM mode 1 : 8-bit PWM mode	RW
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			

MR1 (External Trigger Select Bit) (b3)

Valid when the MR2 bit is set to 1 and bits TAiTGH to TAiTGL in the ONSF register or TRGSR register are set to 00b (TAiIN pin input).

TCK1-TCK0 (Count Source Select Bit) (b7-b6)

Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled). Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.



i = 0 to 4

The above timing diagram applies when the register bits are set as follows:
- The MR0 bit in the TAiMR register = 1 (pulse output)
- The MR3 bit in the TAiMR register = 0 (16-bit PWM mode)
- The MR1 bit in the TAiMR register = 1
- The MR2 bit in the TAiMR register = 1
- Bits TAiTGH to TAiTGL in the ONSF or TRGSR register = 00b

} (The rising edge of the TAiIN pin input is the trigger.)

Operates as 16-bit pulse width modulator

fj: Count source frequency

Figure 17.11 Operation Example in 16-Bit Pulse Width Modulation Mode

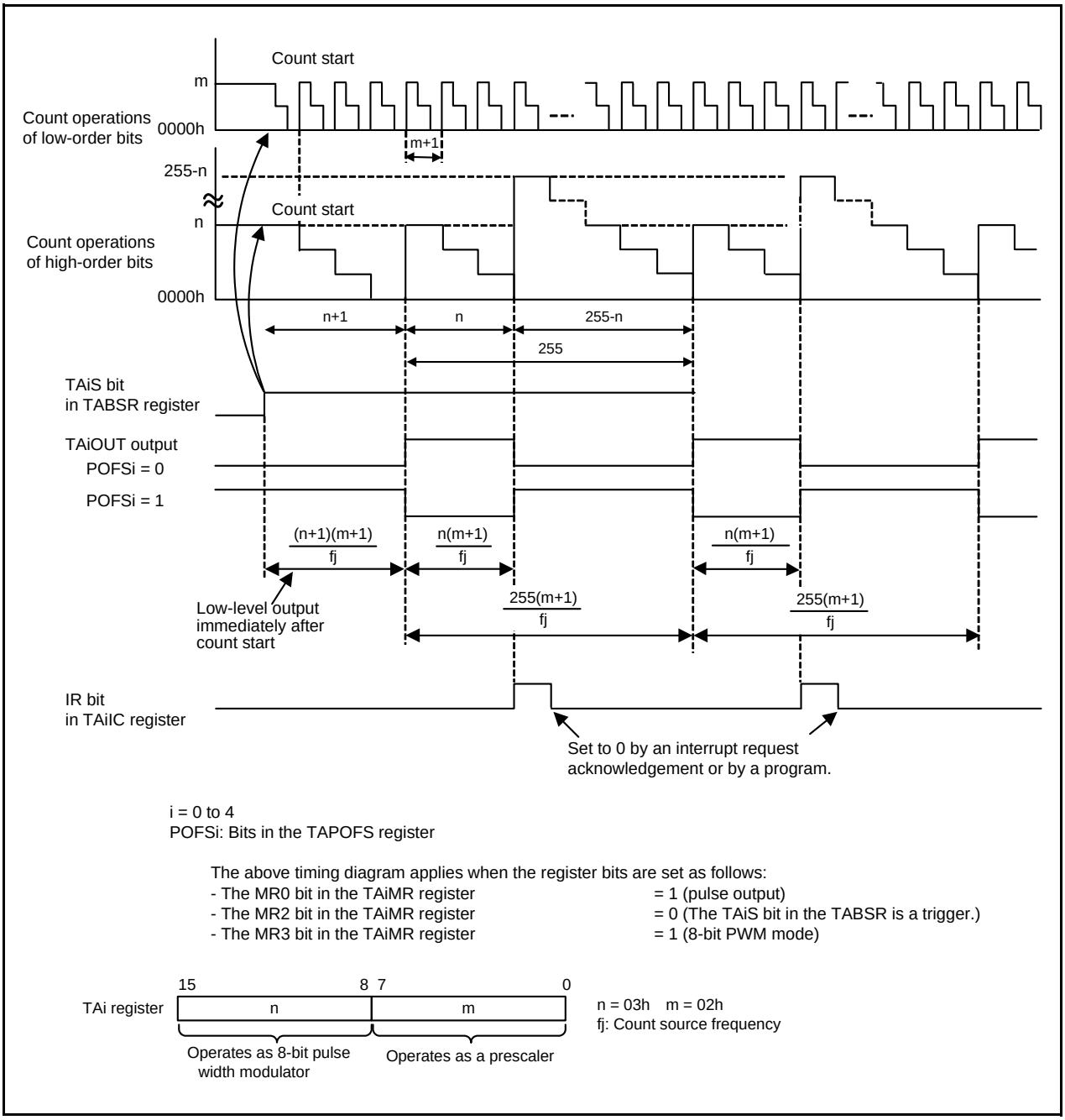
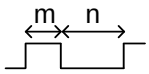


Figure 17.12 Operation Example in 8-Bit Pulse Width Modulation Mode

17.3.7 Programmable Output Mode (Timers A1, A2, and A4)

In programmable output mode, the timer outputs low- and high-levels of pulse width successively. Table 17.16 lists Specifications of Programmable Output Mode. Table 17.17 lists Registers and the Setting in Programmable Output Mode. Figure 17.13 shows Operation Example in Programmable Output Mode.

Table 17.16 Specifications of Programmable Output Mode

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Decrement • Reloads on the rising edge of pulse and continues counting • When a trigger occurs while counting, the timer reloads a new value and restarts counting.
Pulse width	• High-level pulse width $\frac{m}{fj}$  • Low-level pulse width $\frac{n}{fj}$ m: set value of the TAi register n: set value of the TAi1 register fj: count source frequency
Count start condition	• The TAiS bit of the TABSR register is set to 1 (start counting). • The TAiS bit is 1 and external trigger input from the TAiIN pin • The TAiS bit is 1 and one of the following external triggers occurs Timer B2 overflow or underflow Timer Aj overflow or underflow (j = i - 1) Timer Ak overflow or underflow (k = i + 1, except k = 0 if i = 4)
Count stop condition	The TAiS bit is set to 0 (stop counting).
Interrupt request generation timing	At the rising edge of pulse
TAiIN pin function	I/O port or trigger input
TAiOUT pin function	Pulse output
Read from timer	An undefined value is read by reading registers TAi and TAi1.
Write to timer	• When writing to registers TAi and TAi1 while not counting, the value is written to both reload register and counter. • When writing to registers TAi and TAi1 while counting, the value is written to the reload register. (transferred to the counter when reloaded next).
Selectable functions	Output polarity control The output polarity of TAiOUT pin is inverted. (While the TAiS bit is set to 0 (stop counting), the pin outputs a high-level signal.)

i = 1, 2, and 4

Table 17.17 Registers and the Setting in Programmable Output Mode (1)

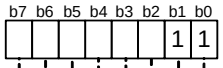
Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write a 1 to reset the clock prescaler.
TCKDIVC0	TCDIV00	Select a clock used prior to timer AB frequency dividing.
PWMFS	PWMFSi	Set to 1.
TACS0 to TACS2	7 to 0	Select the count source.
TAPOFS	POFSi	Select the output polarity.
TAi1	7 to 0	Set a low-level pulse width. (2)
TABSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
ONSF	TAiOS	Set to 0.
	TAZIE	Set to 0.
	TAiTGH to TAiTGL	Select a count trigger.
TRGSR	TAiTGH to TAiTGL	Select a count trigger.
UDF	TAiUD	Set to 0.
	TAiP	Set to 0.
TAi	7 to 0	Set a high-level pulse width. (2)
TAiMR	7 to 0	Refer to the following TAiMR register.

i = 1, 2, and 4

Notes:

1. This table does not describe a procedure.
2. This applies when the POFSi bit in the TAPOFS register is 0.

Programmable Output Mode
Timer Ai Mode Register (i = 1, 2, 4)



Symbol	Address	After Reset
TA0MR to TA4MR	0336h to 033Ah	00h

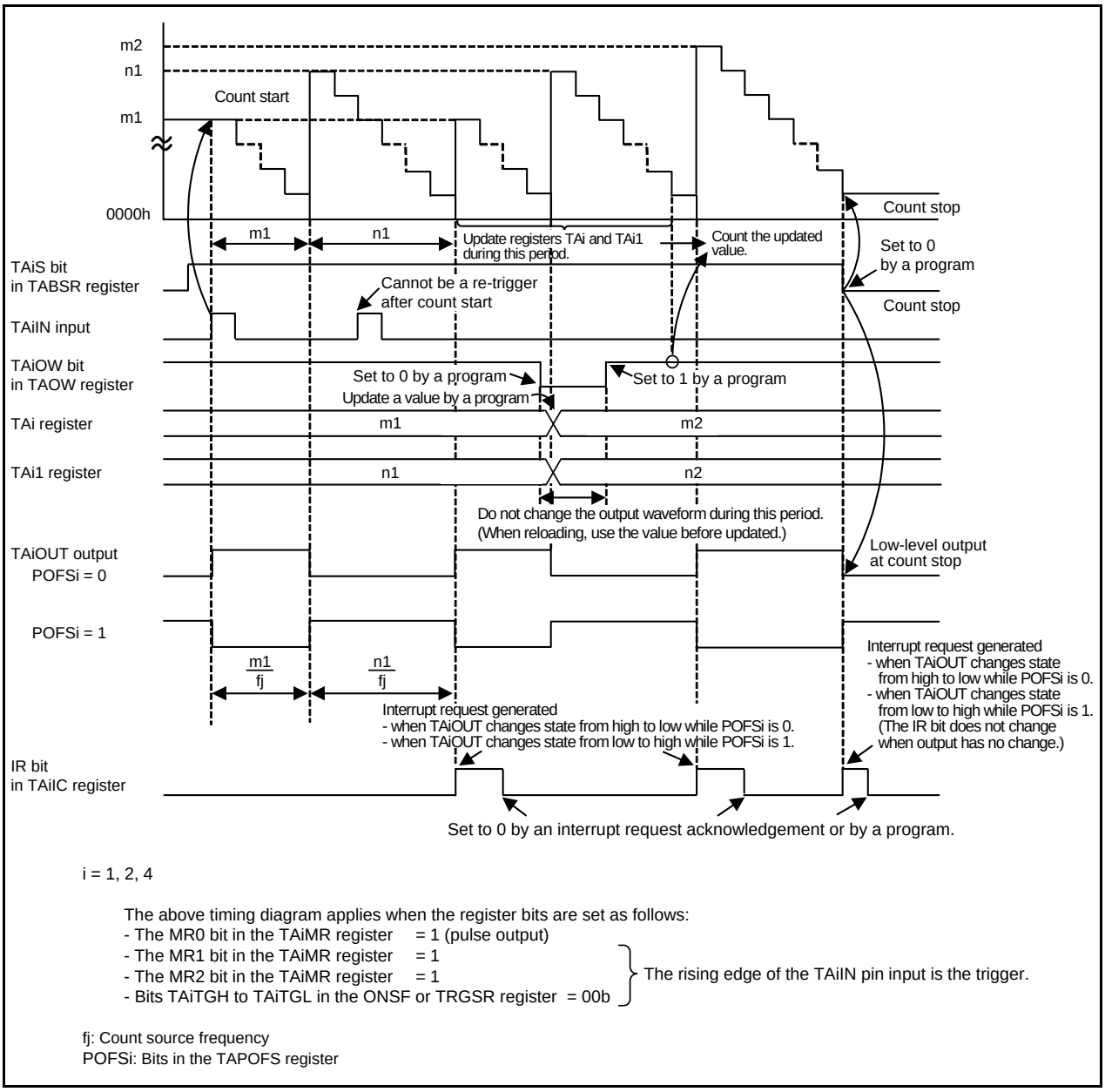
Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 1 : PWM mode or programmable output mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0 : No pulse output (TAiOUT pin functions as I/O port) 1 : Pulse output (TAiOUT pin functions as a pulse output pin)	RW
MR1	External trigger select bit	0 : Falling edge of input signal to TAiIN pin 1 : Rising edge of input signal to TAiIN pin	RW
MR2	Trigger select bit	0 : Write 1 to the TAiS bit in the TABSR register 1 : Selected by bits TAiTGH to TAiTGL	RW
MR3	Set to 0 in programmable output mode		RW
TCK0	Count source select bit	b1 b0 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			

MR1 (External Trigger Select Bit) (b3)

Valid when bits TAiTGH to TAiTGL in the ONSF register or TRGSR register are set to 00b (TAiIN pin input).

TCK1-TCK0 (Count Source Select Bit) (b7-b6)

Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0 to TCK1 enabled). Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.



i = 1, 2, 4

The above timing diagram applies when the register bits are set as follows:
- The MR0 bit in the TAiMR register = 1 (pulse output)
- The MR1 bit in the TAiMR register = 1
- The MR2 bit in the TAiMR register = 1
- Bits TAiTGH to TAiTGL in the ONSF or TRGSR register = 00b

} The rising edge of the TAiIN pin input is the trigger.

fj: Count source frequency
POFSi: Bits in the TAPOFS register

Figure 17.13 Operation Example in Programmable Output Mode

17.4 Interrupts

Refer to individual operation examples for interrupt request generating timing.
Refer to 14.7 “Interrupt Control” for details of interrupt control. Table 17.18 lists Timer A Interrupt Related Registers.

Table 17.18 Timer A Interrupt Related Registers

Address	Register Name	Register Symbol	After Reset
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b

The IR bit in the TAiIC register may become 1 (interrupt requested) when the TMOD1 bit in the TAiMR register is changed from 0 to 1 (change from timer mode or event counter mode to one-shot timer mode, PWM mode, or programmable output mode). Make sure to follow the procedure below when setting the TMOD1 bit to 1. Refer to 14.13 “Notes on Interrupts” as well.

(1) Set bits ILVL2 to ILVL0 in the TAiIC register to 000b (interrupt disabled).
(2) Set the TAiMR register.
(3) Set the IR bit in the TAiIC register to 0 (interrupt not requested).

17.5 Notes on Timer A

17.5.1 Timer A (Timer Mode)

17.5.1.1 Register Setting

The timer stops after reset. Set the mode, count source, counter value, etc., using registers TAiMR, TAi, TACS0 to TACS2, TAPOFS, TCKDIVC0, and PCLKR before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 0 to 4).

Always make sure registers TAiMR, TACS0 to TACS2, TAPOFS, TCKDIVC0, and PCLKR are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

17.5.1.2 Read from Timer

While counting is in progress, the counter value can be read at any time by reading the TAi register. However, if the counter is read at the same time as it is reloaded, the value FFFFh is read. Also, if the counter is read before it starts counting and after a value is set in the TAi register while not counting, the set value is read.

17.5.1.3 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT go to the high-impedance state.

17.5.2 Timer A (Event Counter Mode)

17.5.2.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TAiMR register, the TAi register, the UDF register, bits TAZIE, TA0TGL, and TA0TGH in the ONSF register, the TRGSR register, and the TAPOFS register before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 0 to 4).

Always make sure the TAiMR register, the UDF register, bits TAZIE, TA0TGL, and TA0TGH in the ONSF register, the TRGSR register, and the TAPOFS register are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

17.5.2.2 Read from Timer

While counting is in progress, the counter value can be read at any time by reading the TAi register. However, while reloading, FFFFh can be read in underflow, and 0000h in overflow. When the counter is read before it starts counting and after a value is set in the TAi register while not counting, the set value is read.

17.5.2.3 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT go to the high-impedance state.

17.5.3 Timer A (One-Shot Timer Mode)

17.5.3.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TAiMR register, the TAi register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, the TCKDIVC0 register, and the PCLKR register before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 0 to 4).

Always make sure the TAiMR register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, the TCKDIVC0 register, and the PCLKR register are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

17.5.3.2 Stop While Counting

When setting the TAiS bit to 0 (count stops), the following occurs:

- The counter stops counting and the contents of the reload register are reloaded.
- The TAiOUT pin outputs a low-level signal when the POFSi bit in the TAPOFS register is 0 and outputs a high-level signal when it is 1.
- After one cycle of the CPU clock, the IR bit in the TAiIC register is set to 1 (interrupt requested).

17.5.3.3 Delay between the Trigger Input and Timer Output

One-shot timer output synchronizes with a count source generated internally. When an external trigger is selected, a maximum 1.5 cycle delay of the count source occurs between the trigger input to the TAiIN pin and timer output.

17.5.3.4 Operating Mode Change

The IR bit is set to 1 when timer operating mode is set with any of the following procedures:

- Selecting one-shot timer mode after reset
- Changing the operating mode from timer mode to one-shot timer mode
- Changing the operating mode from event counter mode to one-shot timer mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 after the changes listed above are made.

17.5.3.5 Re-Trigger

When a trigger occurs while counting, the counter reloads the reload register to continue counting after generating a re-trigger and counting down once. To generate a trigger while counting, generate a re-trigger after more than one cycle of the timer count source has elapsed following the previous trigger.

When an external trigger occurs, do not generate a re-trigger for 300 ns before the count value becomes 0000h.

The one-shot timer may stop counting.

17.5.3.6 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT enter a high-impedance state.

17.5.4 Timer A (Pulse Width Modulation Mode)

17.5.4.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TAiMR register, the TAi register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, TCKDIVC0 register, the PWMFS register, and the PCLKR register before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 0 to 4).
Always make sure the TAiMR register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, TCKDIVC0 register, the PWMFS register, and the PCLKR register are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

17.5.4.2 Operating Mode Change

The IR bit is set to 1 when setting a timer operating mode with any of the following procedures:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

17.5.4.3 Stop While Counting

When setting the TAiS bit to 0 (count stops) during PWM pulse output, the following actions occur.
When the POFSi bit in the TAPOFS register is 0:

- Counting stops.
- When the TAiOUT pin is high, the output level goes low and the IR bit is set to 1.
- When the TAiOUT pin is low, both the output level and the IR bit remain unchanged.

When the POFSi bit in the TAPOFS register is 1:

- Stop counting.
- If the TAiOUT pin output is low, the output level goes high and the IR bit is set to 1.
- If the TAiOUT pin output is high, both the output level and the IR bit remain unchanged.

17.5.4.4 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT go to the high-impedance state.

17.5.5 Timer A (Programmable Output Mode)

17.5.5.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TAiMR register, the TAi register, the TRGSR register, registers TACS0 to TACS2, the TAPOF register, TCKDIVC0 register, the PWMFS register, the PCLKR register, and the TAi1 register before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 1, 2, 4).

Always make sure the TAiMR register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, TCKDIVC0 register, the PWMFS register, and the PCLKR register are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

17.5.5.2 Operating Mode Change

The IR bit is set to 1 when setting a timer operating mode with any of the following procedures:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

17.5.5.3 Stop While Counting

When setting the TAiS bit to 0 (count stops) during pulse output, the following actions occur.

When the POFSi bit in the TAPOFS register is 0:

- Counting stops.
- When the TAiOUT pin is high, the output level goes low and the IR bit is set to 1.
- When the TAiOUT pin is low, both the output level and the IR bit remain unchanged.

When the POFSi bit in the TAPOFS register is 1:

- Stop counting.
- If the TAiOUT pin output is low, the output level goes high and the IR bit is set to 1.
- If the TAiOUT pin output is high, both the output level and the IR bit remain unchanged.

17.5.5.4 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT go to the high-impedance state.

18. Timer B

Note

The 80-pin package does not have the TB1IN pin. Do not use functions associated with this pin.

18.1 Introduction

Timers B0 to B5 are provided for timer B. Each timer operates independently of the others. Table 18.1 lists Specifications of Timer B, Figure 18.1 shows Timer A and B Count Sources, Figure 18.2 shows Timer B Configuration, Figure 18.3 shows Timer B Block Diagram, and Table 18.2 lists I/O Ports.

Table 18.1 Specifications of Timer B

Item	Specification
Configuration	16-bit timer × 6
Operating mode	• Timer mode The timer counts an internal count source. • Event counter mode The timer counts pulses from an external device, or overflows and underflows of other timers. • Pulse period/pulse width measurement modes The timer measures pulse period or pulse width of an external signal.
Interrupt source	Overflow/underflow/active edge of measurement pulse × 6

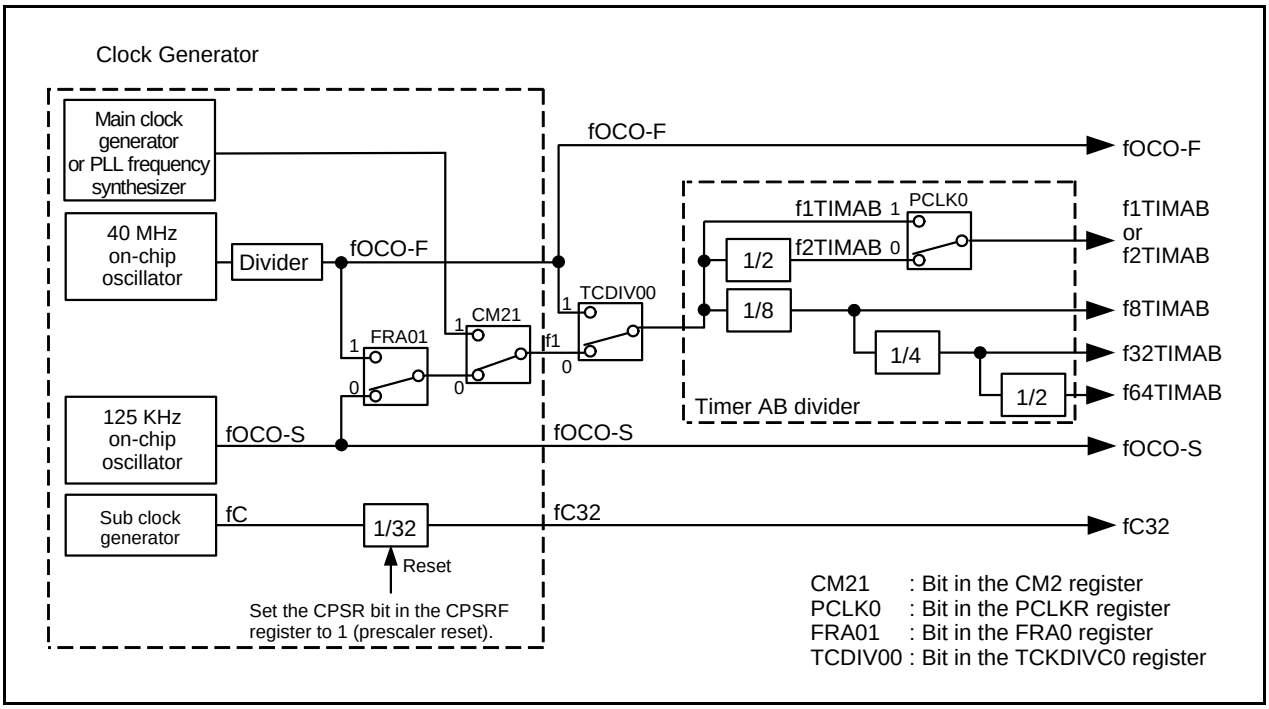


Figure 18.1 Timer A and B Count Sources

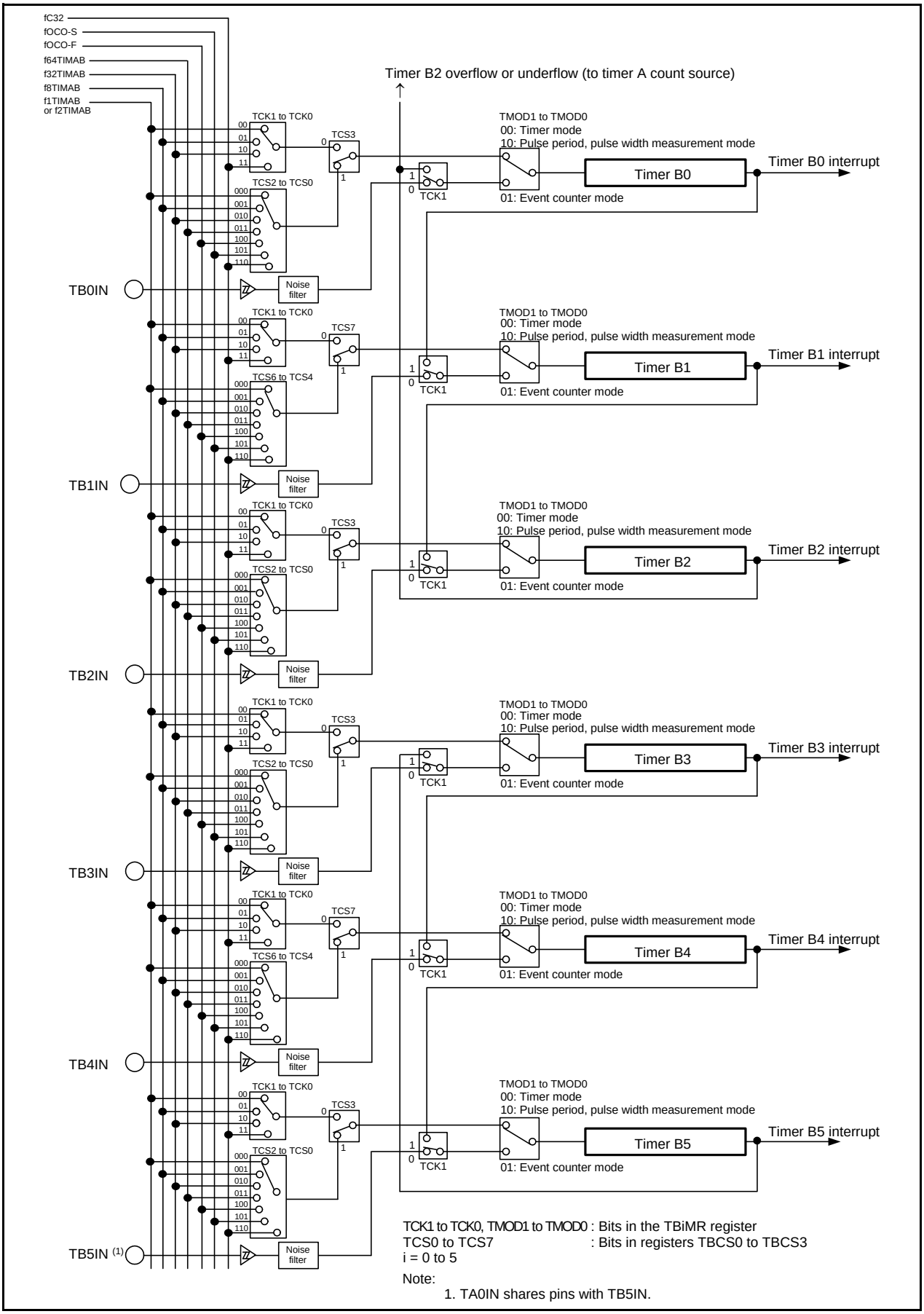


Figure 18.2 Timer B Configuration

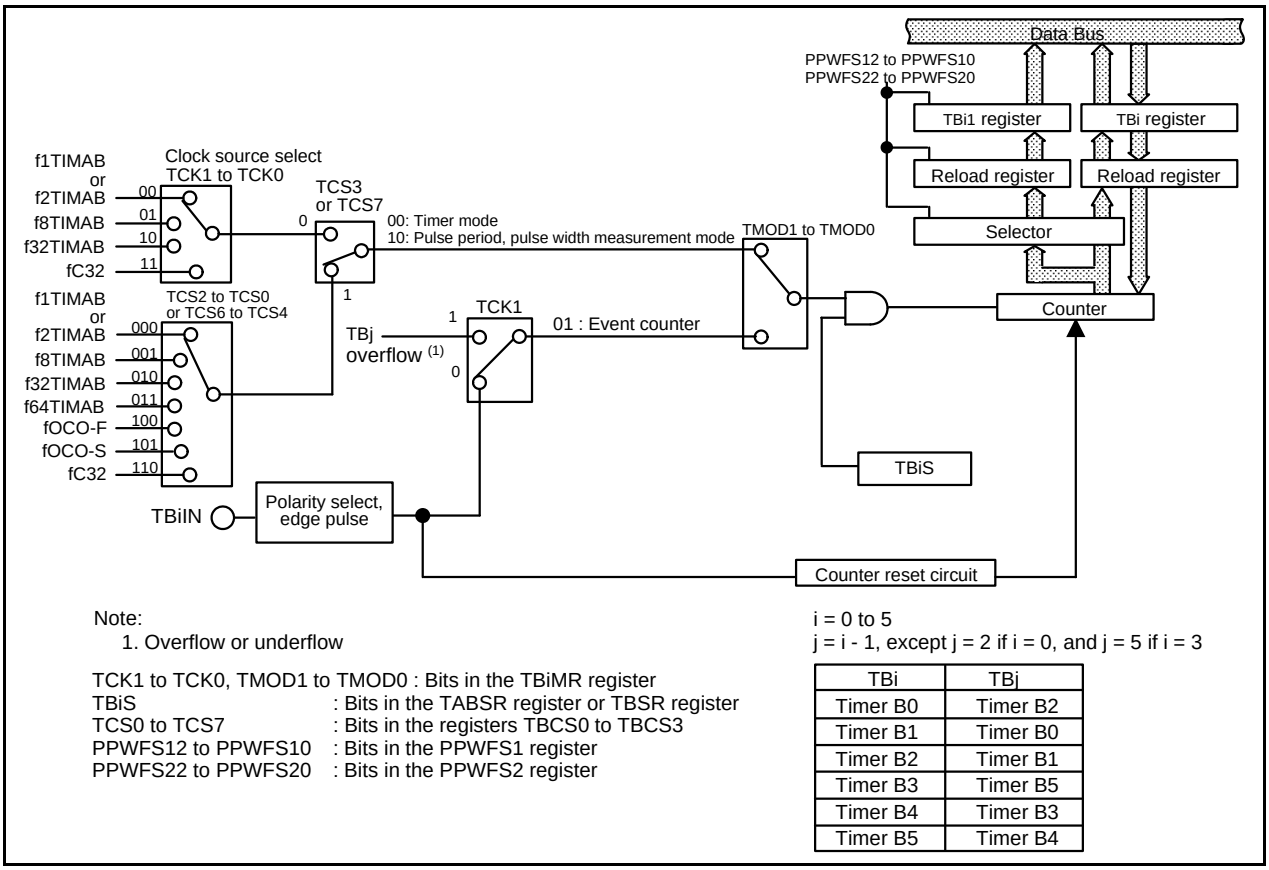


Figure 18.3 Timer B Block Diagram

Table 18.2 I/O Ports

Pin Name	I/O Type	Function
TBiIN	Input (1)	Count source input (event counter mode) Measurement pulse input (pulse period measurement mode, pulse width measurement mode)

i = 0 to 5

Note:

1. When using the TBiIN pin for input, set the port direction bit corresponding to the pin to 0 (input mode).

18.2 Registers

Table 18.3 lists registers associated with timer B.
Set the TCDIV00 bit in the TCKDIVC0 register before setting other registers associated with timer B. After changing the TCDIV00 bit, set other registers associated with timer B again.
Refer to “registers and the setting” in each mode for registers and bit settings.

Table 18.3 Register Structure

Address	Register Name	Register Symbol	After Reset
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
01C0h 01C1h	Timer B0-1 Register	TB01	XXh XXh
01C2h 01C3h	Timer B1-1 Register	TB11	XXh XXh
01C4h 01C5h	Timer B2-1 Register	TB21	XXh XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CBh	Timer AB Division Control Register 0	TCKDIVC0	0000 X000b
01E0h 01E1h	Timer B3-1 Register	TB31	XXh XXh
01E2h 01E3h	Timer B4-1 Register	TB41	XXh XXh
01E4h 01E5h	Timer B5-1 Register	TB51	XXh XXh
01E6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 2	PPWFS2	XXXX X000b
01E8h	Timer B Count Source Select Register 2	TBCS2	00h
01E9h	Timer B Count Source Select Register 3	TBCS3	X0h
0300h	Timer B3/B4/B5 Count Start Flag	TBSR	000X XXXXb
0310h 0311h	Timer B3 Register	TB3	XXh XXh
0312h 0313h	Timer B4 Register	TB4	XXh XXh
0314h 0315h	Timer B5 Register	TB5	XXh XXh
031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
0320h	Count Start Flag	TABSR	00h
0330h 0331h	Timer B0 Register	TB0	XXh XXh
0332h 0333h	Timer B1 Register	TB1	XXh XXh
0334h 0335h	Timer B2 Register	TB2	XXh XXh
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b

18.2.1 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0		0	0	0		

Symbol	Address	After Reset
PCLKR	0012h	0000 0011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A and B clock select bit (clock source for timers A and B, the dead time timer, and muliti-master I^2C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART2, UART5 to UART7, SI/O3, and SI/O4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0	RW
PCLK5	Clock output function extension bit (valid in single-chip mode)	0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1	RW
— (b7-b6)	Reserved bits	Set to 0	RW

Write to the PCLKR register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

18.2.2 Clock Prescaler Reset Flag (CPSRF)

Clock Prescaler Reset Flag

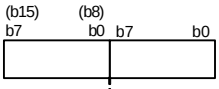
b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
CPSRF	0015h	0XXX XXXXb

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	No register bits. If necessary, set to 0. Read as undefined value		—
CPSR	Clock prescaler reset flag	Setting this bit to 1 initializes the prescaler for the timekeeping clock. (Read as 0)	RW

18.2.3 Timer Bi Register (TBi) (i = 0 to 5)

Timer Bi Register (i = 0 to 5)



Symbol	Address	After Reset
TB0	0331h to 0330h	Undefined
TB1	0333h to 0332h	Undefined
TB2	0335h to 0334h	Undefined
TB3	0311h to 0310h	Undefined
TB4	0313h to 0312h	Undefined
TB5	0315h to 0314h	Undefined

Mode	Function	Setting Range	RW
Timer mode	When n = set value, Counter cycle: $\frac{(n + 1)}{fj}$	0000h to FFFFh	RW
Event counter mode	When n = set value, n + 1 count	0000h to FFFFh	RW
Pulse period measurement mode, Pulse width measurement mode	Set an initial value. Measures a pulse period or width. Read the counter value while counting is in progress.	0000h to FFFFh	RW

fj : Count source frequency

Access this register in 16-bit units.

Event Counter Mode

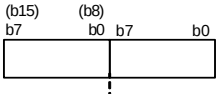
The timer counts pulses from an external device or overflows or underflows of other timers.

Pulse Period Measurement Mode, Pulse Width Measurement Mode

Set these modes when the TBiS bit in the TABSR or TBSR register is set to 0 (count stops).
Read only (RO) when the TBiS bit in the TABSR or TBSR register is set to 1 (count starts).
The counter starts counting the count source at an active edge of the measurement pulse, transfers the count value to a register at the next active edge, and continues counting.
The measurement result can be read by reading the TBi register when bits PPWFS12 to PPWFS10 in the PPWFS1 register and bits PPWFS22 to PPWFS20 in the PPWFS2 register are 0.
While counting is in progress, the counter value can be read by reading the TBi register when bits PPWFS12 to PPWFS10 and bits PPWFS22 to PPWFS20 are 1.

18.2.4 Timer Bi-1 Register (TBi1) (i = 0 to 5)

Timer Bi-1 Register (i = 0 to 5)



Symbol	Address	After Reset
TB01	01C1h to 01C0h	Undefined
TB11	01C3h to 01C2h	Undefined
TB21	01C5h to 01C4h	Undefined
TB31	01E1h to 01E0h	Undefined
TB41	01E3h to 01E2h	Undefined
TB51	01E5h to 01E4h	Undefined

Mode	Function	Setting Range	RW
Pulse period measurement mode Pulse width measurement mode	Measures a pulse period or width	0000h to FFFFh	RO

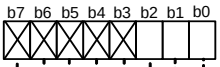
Access the register in 16-bit units.

The measurement result can be read by reading the TBi-1 register when bits PPWFS12 to PPWFS10 in the PPWFS1 register and bits PPWFS22 to PPWFS20 in the PPWFS2 register are 1.

The value in the TBi1 register is undefined when bits PPWFS12 to PPWFS10 and bits PPWFS22 to PPWFS20 are 0.

18.2.5 Pulse Period/Pulse Width Measurement Mode Function Select Register i (PPWFSi) (i = 1, 2)

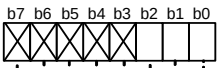
Pulse Period/Pulse Width Measurement Mode Function Select Register 1



Symbol	Address	After Reset
PPWFS1	01C6h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
PPWFS10	Timer B0 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB0 register. The TB01 register is not used 1 : The counter value is read in the TB01 register. Measurement result is stored in the TB0 register	RW
PPWFS11	Timer B1 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB1 register. The TB11 register is not used 1 : The counter value is read in the TB11 register. Measurement result is stored in the TB1 register	RW
PPWFS12	Timer B2 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB2 register. The TB21 register is not used 1 : The counter value is read in the TB21 register. Measurement result is stored in the TB2 register	RW
— (b7-b3)	No register bits. If necessary, set to 0. Read as undefined value		—

Pulse Period/Pulse Width Measurement Mode Function Select Register 2



Symbol	Address	After Reset
PPWFS2	01E6h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
PPWFS20	Timer B3 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB3 register. The TB31 register is not used 1 : The counter value is read in the TB31 register. Measurement result is stored in the TB3 register	RW
PPWFS21	Timer B4 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB4 register. The TB41 register is not used 1 : The counter value is read in the TB41 register. Measurement result is stored in the TB4 register	RW
PPWFS22	Timer B5 pulse period/pulse width measurement mode function select bit	0 : Measurement result is stored in the TB5 register. The TB51 register is not used 1 : The counter value is read in the TB51 register. Measurement result is stored in the TB5 register	RW
— (b7-b3)	No register bits. If necessary, set to 0. Read as undefined value		—

Enabled in pulse period measurement mode or pulse width measurement mode.

18.2.6 Timer B Count Source Select Register i (TBCSi) (i = 0 to 3)

Timer B Count Source Select Register 0, Timer B Count Source Select Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TBCS0	01C8h	00h
TBCS2	01E8h	00h

Bit Symbol	Bit Name	Function	RW
TCS0	TBi count source select bit	b2 b1 b0 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS1			RW
TCS2			RW
TCS3	TBi count source option specified bit	1 : TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 0 : TCK0 to TCK1 disabled, TCS0 to TCS2 enabled	RW
TCS4	TBj count source select bit	b6 b5 b4 0 0 0 : f1TIMAB or f2TIMAB 0 0 1 : f8TIMAB 0 1 0 : f32TIMAB 0 1 1 : f64TIMAB 1 0 0 : fOCO-F 1 0 1 : fOCO-S 1 1 0 : fC32 1 1 1 : Do not set	RW
TCS5			RW
TCS6			RW
TCS7	TBj count source option specified bit	1 : TCK0 to TCK1 enabled, TCS4 to TCS6 disabled 0 : TCK0 to TCK1 disabled, TCS4 to TCS6 enabled	RW

TBCS0 register: i = 0, j = 1 TBCS2 register: i = 3, j = 4

Timer B Count Source Select Register 1, Timer B Count Source Select Register 3

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TBCS1	01C9h	X0h
TBCS3	01E9h	X0h

Bit Symbol	Bit Name	Function	RW
TCS0	TBi count source select bit	b2 b1 b0 0 0 0: f1TIMAB or f2TIMAB 0 0 1: f8TIMAB 0 1 0: f32TIMAB 0 1 1: f64TIMAB 1 0 0: fOCO-F 1 0 1: fOCO-S 1 1 0: fC32 1 1 1: Do not set	RW
TCS1			RW
TCS2			RW
TCS3	TBi count source option specified bit	1: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 0: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value		—

TBCS1 register: i = 2 TBCS3 register: i = 5

TCS2-TCS0 (TBi Count Source Select Bit) (b2-b0)
TCS6-TCS4 (TBj Count Source Select Bit) (b6-b4)

Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.

18.2.7 Timer AB Division Control Register 0 (TCKDIVC0)

Timer AB Division Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	X	0	0	

Symbol: TCKDIVC0
Address: 01CBh
After Reset: 0000 X000b

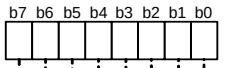
Bit Symbol	Bit Name	Function	RW
TCDIV00	Clock select prior to timer AB division bit	0 : f1 1 : fOCO-F	RW
— (b2-b1)	Reserved bits	Set to 0	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
— (b7-b4)	Reserved bits	Set to 0	RW

TCDIV00 (Clock Select Prior to Timer AB Division Bit) (b1)

Set the TCDIV00 bit while timer A and B stops.
Set the TCDIV00 bit before setting other registers associated with timer B.
After changing the TCDIV00 bit, set other registers associated with timer B again.

18.2.8 Count Start Flag (TABSR)
Timer B3/B4/B5 Count Start Flag (TBSR)

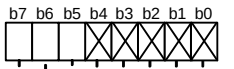
Count Start Flag



Symbol	Address	After Reset
TABSR	0320h	00h

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0 : Stop counting 1 : Start counting	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

Timer B3/B4/B5 Count Start Flag

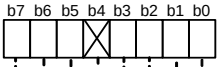


Symbol	Address	After Reset
TBSR	0300h	000X XXXXb

Bit Symbol	Bit Name	Function	RW
— (b4-b0)	No register bits. If necessary, set to 0. Read as undefined value		—
TB3S	Timer B3 count start flag	0 : Stop counting 1 : Start counting	RW
TB4S	Timer B4 count start flag		RW
TB5S	Timer B5 count start flag		RW

18.2.9 Timer Bi Mode Register (TBiMR) (i = 0 to 5)

Timer Bi Mode Register (i = 0 to 5)



Symbol	Address	After Reset
TB0MR to TB2MR	033Bh to 033Dh	00XX 0000b
TB3MR to TB5MR	031Bh to 031Dh	00XX 0000b

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode 0 1 : Event counter mode 1 0 : Pulse period measurement mode Pulse width measurement mode 1 1 : Do not set	RW
TMOD1			RW
MR0	Function varies with the operation mode		RW
MR1			RW
— (b4)	No register bit. If necessary, set to 0. Read as undefined value		—
MR3	Function varies with the operation mode		RO
TCK0	Count source select bit (Function varies with the operation mode)		RW
TCK1			RW

18.3 Operations

18.3.1 Common Operations

18.3.1.1 Operating Clock

The count source for each timer acts as a clock, controlling such timer operations as counting and reloading.

18.3.1.2 Counter Reload Timing

Timer Bi starts counting from the value (n) set in the TBi register. The TBi register consists of a counter and a reload register. The counter starts decrementing the count source from n, reloads a value in the reload register at the next count source after the value becomes 0000h, and continues decrementing. The value written in the TBi register takes effect in the counter and the reload register at the timings below.

- When the count is stopped
- Between the count starts and the first count source is input
  A value written to the TBi register is immediately written to the counter and the reload register.

- After the count starts and the first count source is input
  A value written to the TBi register is immediately written to the reload register.
  The counter continues counting and reloads the value in the reload register at the next count source after the value becomes 0000h.

18.3.1.3 Count Source

Internal clocks are counted in timer mode, pulse period measurement mode, and pulse width measurement mode. (Refer to Figure 18.1 “Timer A and B Count Sources”.) Table 18.4 lists Timer B Count Source.

Timer A, B, and multi-master I^2C-bus interface share the divider. f1 or fOCO-F can be selected before the timer AB divider.

f1 is any of the clocks listed below. Select f1 by the CM21 bit in the CM2 register and the FRA01 bit in the FRA0 register. (Refer to 8. “Clock Generator”.)

- Main clock divided by 1 (no division)
- PLL clock divided by 1 (no division)
- fOCO-S divided by 1 (no division)
- fOCO-F divided by 1 (no division)

Table 18.4 Timer B Count Source

Count Source	Bit Set Value				Remarks
	PCLK0	TCS3 TCS7	TCS2 to TCS0 TCS4 to TCS6	TCK1 to TCK0	
f1TIMAB	1	0	-	00b	f1 or fOCO-F (1)
		1	000b	-	
f2TIMAB	0	0	-	00b	f1 divided by 2 or
		1	000b	-	fOCO-F divided by 2 (1)
f8TIMAB	-	0	-	01b	f1 divided by 8 or
		1	001b	-	fOCO-F divided by 8 (1)
f32TIMAB	-	0	-	10b	f1 divided by 32 or
		1	010b	-	fOCO-F divided by 32 (1)
f64TIMAB	-	1	011b	-	f1 divided by 64 or fOCO-F divided by 64 (1)
fOCO-F	-	1	100b	-	fOCO-F
fOCO-S	-	1	101b	-	fOCO-S
fC32	-	0	-	11b	fC32
		1	110b	-	

PCLK0: Bit in the PCLKR register

TCS7 to TCS0: Bits in registers TBCS0 toTBCS3

TCK1 to TCK0: Bits in the TBiMR register (i = 0 to 5)

Note:

1. Select f1 or fOCO-F by the TCDIV00 bit in the TCKDIVC0 register.

18.3.2 Timer Mode

In timer mode, the timer counts a count source generated internally. Table 18.5 lists Specifications of Timer Mode, Table 18.6 lists Registers and the Setting in Timer Mode, and Figure 18.4 shows Operation Example in Timer Mode.

Table 18.5 Specifications of Timer Mode

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Decrement • When the timer underflows, it reloads the reload register contents and continues counting.
Counter cycles	$\frac{1}{(n+1)}$ n: set value of the TBi register 0000h to FFFFh
Count start condition	Set the TBiS bit (1) to 1 (start counting).
Count stop condition	Set the TBiS bit to 0 (stop counting).
Interrupt request generation timing	Timer underflow
TBiIN pin function	I/O port
Read from timer	Count value can be read by reading the TBi register.
Write to timer	• When not counting The value written to the TBi register is written to both the reload register and the counter. • When counting The value written to the TBi register is only written to the reload register (transferred to the counter when reloaded next).

i = 0 to 5

Note:

1. Bits TB0S to TB2S are assigned to bits 5 to 7 in the TABSR register, and bits TB3S to TB5S are assigned to bits 5 to 7 in the TBSR register.

Table 18.6 Registers and the Setting in Timer Mode (1)

Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write a 1 to reset the clock prescaler.
TBi1	7 to 0	- (setting unnecessary)
PPWFS1 to PPWFS2	PPWFS12 to PPWFS10 PPWFS22 to PPWFS20	Set to 0.
TCKDIVC0	TCDIV00	Select a clock used prior to timer AB frequency dividing.
TBCS0 to TBCS3	7 to 0	Select the count source.
TABSR TBSR	TAiS	Set to 1 when starting counting. Set to 0 when stopping counting.
TBi	7 to 0	Set the count value.
TBiMR	7 to 0	Refer to the TBiMR register below.

i = 0 to 5

Note:

1. This table does not describe a procedure.

Timer Mode

Timer Bi Mode Register (i = 0 to 5)

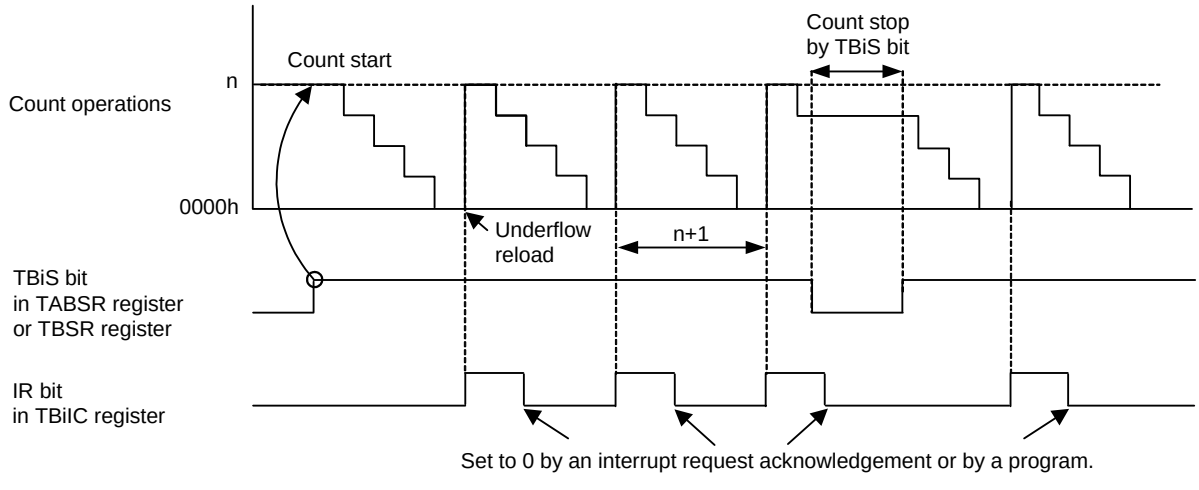
b7	b6	b5	b4	b3	b2	b1	b0
			X	0	0	0	0

Symbol	Address	After Reset
TB0MR to TB2MR TB3MR to TB5MR	033Bh to 033Dh 031Bh to 031Dh	00XX 0000b 00XX 0000b

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode	RW
TMOD1			RW
MR0	Set to 0 in timer mode		RW
MR1			RW
—	No register bit. If necessary, set to 0. Read as undefined value		—
MR3	Write 0 in timer mode. Read as undefined value in timer mode		RO
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			RW

TCK1-TCK0 (Count Source Select Bit) (b7-b6)

Enabled when the TCS3 or TCS7 bit in registers TBCS0 to TBCS3 is set to 0 (TCK0 to TCK1 enabled).
Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.



i = 0 to 5

The above timing diagram applies when the register bits are set as follows:
-Value in the TBi register (n) = 0004h

Figure 18.4 Operation Example in Timer Mode

18.3.3 Event Counter Mode

In event counter mode, the timer counts pulses from an external device or overflows and underflows of other timers. Table 18.7 lists Specifications of Event Counter Mode, Table 18.8 lists Registers and the Setting in Event Counter Mode, and Figure 18.5 shows Operation Example in Event Counter Mode.

Table 18.7 Specifications of Event Counter Mode

Item	Specification
Count source	• External signals input to TBiIN pin (active edge can be selected by a program: rising edge, falling edge, or both rising and falling edges) • Timer Bj overflow or underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register contents and continues counting.
Number of counts	$\frac{1}{(n+1)}$ n: set value of the TBi register 0000h to FFFFh
Count start condition	Set the TBiS bit (1) to 1 (start counting).
Count stop condition	Set the TBiS bit to 0 (stop counting).
Interrupt request generation timing	Timer underflow
TBiIN pin function	Count source input
Read from timer	Count value can be read by reading the TBi register.
Write to timer	• When not counting Value written to the TBi register is written to both reload register and counter. • When counting Value written to the TBi register is written to only reload register (transferred to counter when reloaded next).

i = 0 to 5 j = i - 1, except j = 2 if i = 0, j = 5 if i = 3

Note:

1. Bits TB0S to TB2S are assigned to bits 5 to 7 in the TABSR register, and bits TB3S to TB5S are assigned to bits 5 to 7 in the TBSR register.

Table 18.8 Registers and the Setting in Event Counter Mode (1)

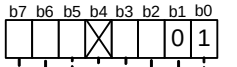
Register	Bit	Setting
PCLKR	PCLK0	Set to 1.
CPSRF	CPSR	Write a 1 to reset the clock prescaler.
TBi1	7 to 0	- (setting unnecessary)
PPWFS1 to PPWFS2	PPWFS12 to PPWFS10 PPWFS22 to PPWFS20	Set to 0.
TCKDIVC0	TCDIV00	Set to 0.
TBCS0 to TBCS3	7 to 0	Set to 00b.
TABSR TBSR	TBiS	Set to 1 when starting counting. Set to 0 when stopping counting.
TBi	7 to 0	Set the count value.
TBiMR	7 to 0	Refer to the TBiMR register below.

i = 0 to 5

Note:

1. This table does not describe a procedure.

Event Counter Mode
Timer Bi Mode Register (i = 0 to 5)

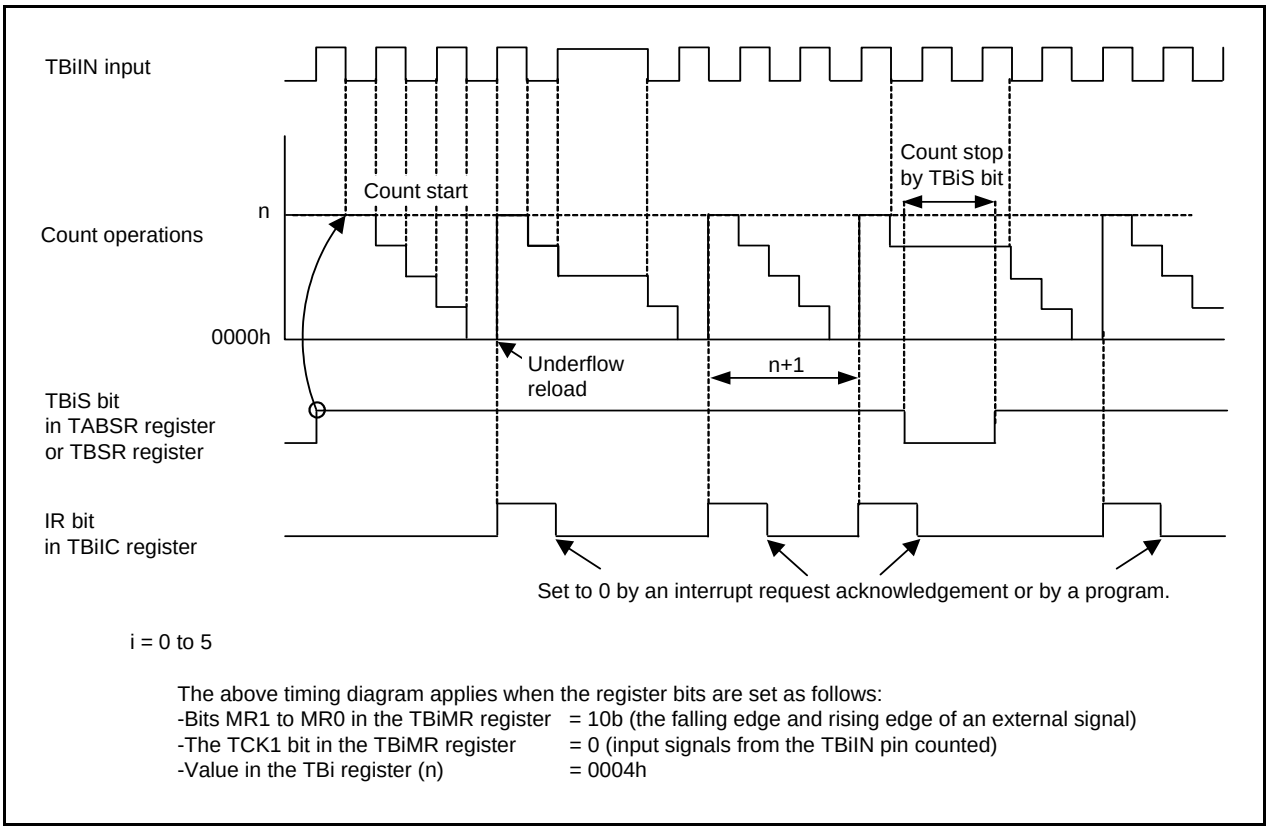


Symbol	Address	After Reset
TB0MR to TB2MR	033Bh to 033Dh	00XX 0000b
TB3MR to TB5MR	031Bh to 031Dh	00XX 0000b

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 1 : Event counter mode	RW
TMOD1			RW
MR0	Count polarity select bit	b3 b2 0 0 : Counts falling edges of external signal 0 1 : Counts rising edges of external signal 1 0 : Counts falling and rising edges of an external signal 1 1 : Do not set	RW
MR1			RW
—	No register bit. If necessary, set to 0. Read as undefined value		—
MR3	Write 0 in event counter mode. Read as undefined value in event counter mode		RO
TCK0	Invalid in event counter mode. Set 0 or 1		RW
TCK1	Event clock select	0 : Input from TBiIN pin 1 : TBj overflow or underflow (j = i – 1; however, j = 2 if i = 0, j = 5 if i = 3)	RW

MR1-MR0 (Count Polarity Select Bit) (b3-b2)

Valid when the TCK1 bit is 0 (input from TBiIN pin). If the TCK1 bit is 1 (TBj overflow or underflow), these bits can be set to 0 or 1.



The above timing diagram applies when the register bits are set as follows:
-Bits MR1 to MR0 in the TBiMR register = 10b (the falling edge and rising edge of an external signal)
-The TCK1 bit in the TBiMR register = 0 (input signals from the TBiIN pin counted)
-Value in the TBi register (n) = 0004h

Figure 18.5 Operation Example in Event Counter Mode

18.3.4 Pulse Period/Pulse Width Measurement Modes

In pulse period and pulse width measurement modes, the timer measures pulse period or pulse width of an external signal. Table 18.9 lists Specifications of Pulse Period/Pulse Width Measurement Modes, Table 18.10 lists Registers and the Setting in Pulse Period/Pulse Width Measurement Modes, Figure 18.6 shows Operation Example in Pulse Period Measurement Mode, and Figure 18.7 shows Operation Example in Pulse Width Measurement Mode.

Table 18.9 Specifications of Pulse Period/Pulse Width Measurement Modes

Item	Specification
Count source	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32
Count operations	• Increment • Counter value is transferred to reload register at an active edge of the measurement pulse. The counter value is set to 0000h to continue counting.
Count start condition	Set the TBiS bit (3) to 1 (start counting).
Count stop condition	Set the TBiS bit to 0 (stop counting).
Interrupt request generation timing	• When an active edge of measurement pulse is input (1) • Timer overflow. When an overflow occurs, the MR3 bit in the TBiMR register is set to 1 (overflowed) simultaneously.
TBiIN pin function	Measurement pulse input
Read from timer	When bits PPWFS12 to PPWFS10 and PPWFS22 to PPWFS20 in registers PPWFS1 and PPWFS2 are 0 • Contents of the reload register (measurement result) can be read by reading the TBi register (2) When bits PPWFS12 to PPWFS10 and PPWFS22 to PPWFS20 in registers PPWFS1 and PPWFS2 are 1 • Contents of the counter (counter value) can be read by reading the TBi register • Contents of the reload register (measurement result) can be read by reading the TBi1 register
Write to timer	• When not counting Value written to the TBi register is written to both reload register and counter. • When counting Value written to the TBi register is written to only reload register (transferred to counter when reloaded next).

i = 0 to 5

Notes:

1. No Interrupt request is generated when the first active edge is input after the timer starts counting.
2. Value read from the TBi register is undefined until the second active edge is input after the timer starts counting.
3. Bits TB0S to TB2S are assigned to bits 5 to 7 in the TABSR register, and bits TB3S to TB5S are assigned to bits 5 to 7 in the TBSR register.

Table 18.10 Registers and the Setting in Pulse Period/Pulse Width Measurement Modes (1)

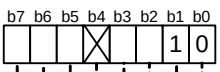
Register	Bit	Setting
PCLKR	PCLK0	Select the count source.
CPSRF	CPSR	Write a 1 to reset the clock prescaler.
TBi1	7 to 0	Measurement result can be read when the bits in the PPWFS1 or PPWFS2 register corresponding to timer Bi are 1.
PPWFS1 to PPWFS2	PPWFS12 to PPWFS10 PPWFS22 to PPWFS20	Set to 1 to read the counter value while counting.
TCKDIVC0	TCDIV00	Select a clock used prior to timer AB frequency dividing.
TBCS0 to TBCS3	7 to 0	Select the count source.
TABSR TBSR	TBiS	Set to 1 when starting counting. Set to 0 when stopping counting.
TBi	7 to 0	Set the initial value. The measurement result can be read when the bits in the PPWFS1 or PPWFS register corresponding to timer Bi are 0. The counter value can be read when the bits in the PPWFS1 or PPWFS2 register corresponding to timer Bi are 1.
TBiMR	7 to 0	Refer to the following TBiMR register.

i = 0 to 5

Note:

1. This table does not describe a procedure.

Pulse Period/Pulse Width Measurement Modes
Timer Bi Mode Register (i = 0 to 5)



Symbol	Address	After Reset
TB0MR to TB2MR	033Bh to 033Dh	00XX 0000b
TB3MR to TB5MR	031Bh to 031Dh	00XX 0000b

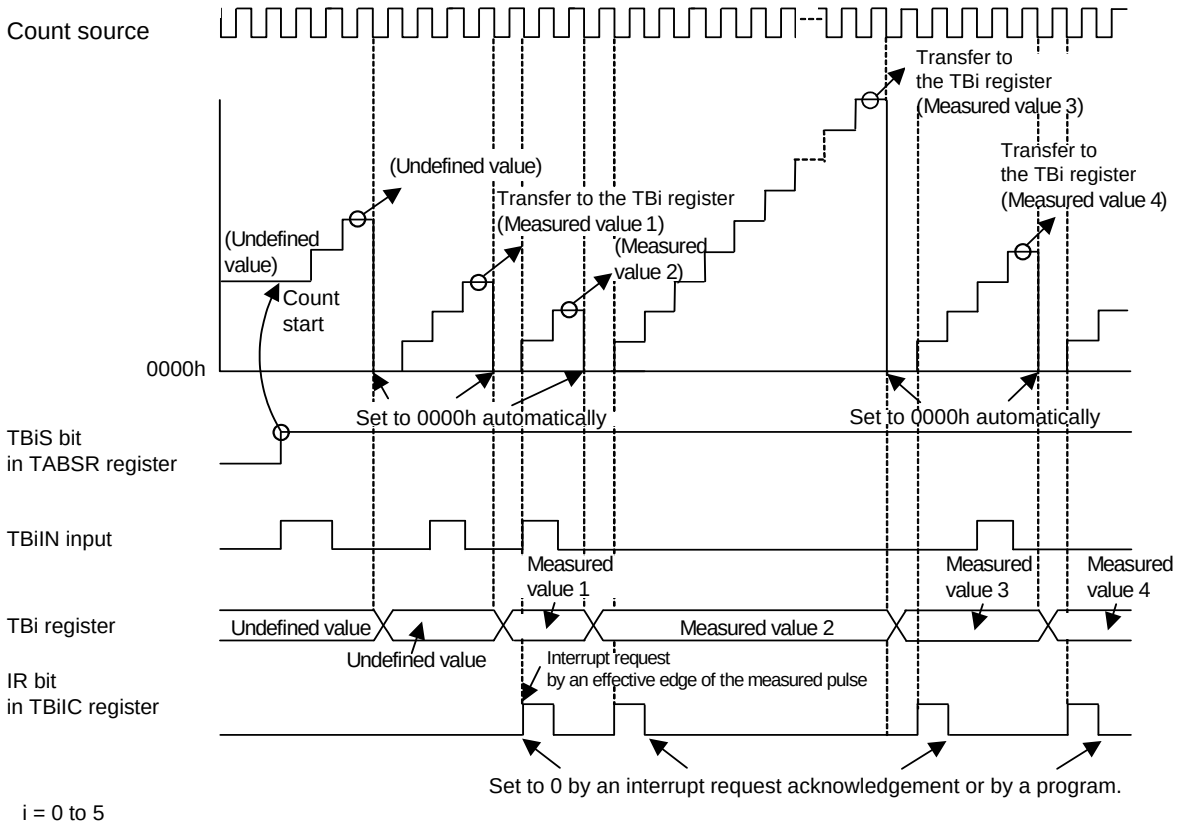
Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 1 0 : Pulse period/pulse width measurement modes	RW
TMOD1			RW
MR0	Measurement mode select bit	b3 b2 0 0 : Pulse period measurement (Measurement between a falling edge and the next falling edge of measured pulse) 0 1 : Pulse period measurement (Measurement between a rising edge and the next rising edge of measured pulse) 1 0 : Pulse width measurement (Measurement between a falling edge and the next rising edge of measured pulse and between a rising edge and the next falling edge) 1 1 : Do not set	RW
MR1			RW
—	No register bit. If necessary, set to 0. Read as undefined value		—
MR3	Timer Bi overflow flag	0 : No overflow 1 : Overflow	RO
TCK0	Count source select bit	b7 b6 0 0 : f1TIMAB or f2TIMAB 0 1 : f8TIMAB 1 0 : f32TIMAB 1 1 : fC32	RW
TCK1			RW

MR3 (Timer Bi Overflow Flag) (b5)

This flag is undefined after reset. The MR3 bit is cleared to 0 (no overflow) by writing to the TBiMR register. The MR3 bit cannot be set to 1 by a program.

TCK1-TCK0 (Count Source Select Bit) (b7-b6)

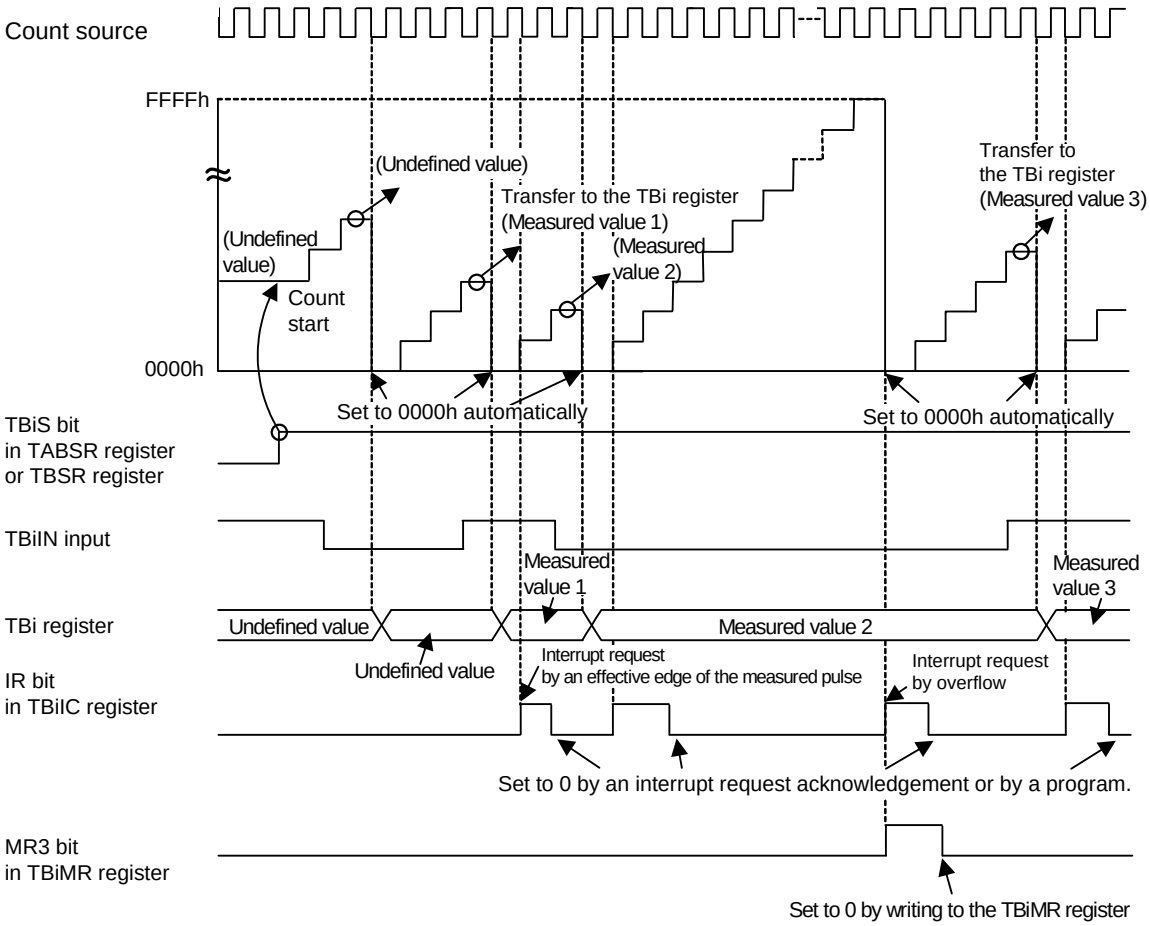
Enabled when the TCS3 bit or TCS7 bit in registers TBCS0 to TBCS3 is set to 0 (TCK0, TCK1 enabled).
Select f1TIMAB or f2TIMAB by the PCLK0 bit in the PCLKR register.



i = 0 to 5

The above timing diagram applies when the register bits are set as follows:
-Bits MR1 to MR0 in the TBiMR register = 00b (measurement between a falling edge and the next falling edge of measured pulse)
-Bits PPWFS12 to PPWFS10 and PPWFS22 to PPWFS20 in registers PPWFS1 and PPWFS2 = 0 (measurement result stored in the TBi register)
-No initial value is set while timer Bi is stopped.

Figure 18.6 Operation Example in Pulse Period Measurement Mode



i = 0 to 5

The above timing diagram applies when the register bits are set as follows:
-Bits MR1 to MR0 in the TBiMR register = 10b (measure pulse width)
-Bits PPWFS12 to PPWFS10 and PPWFS22 to PPWFS20 in registers PPWFS1 and PPWFS2 = 0 (measurement result stored in the TBi register)
-No initial value is set while timer Bi is stopped.

Figure 18.7 Operation Example in Pulse Width Measurement Mode

18.4 Interrupts

Refer to individual operation examples for interrupt request generating timing.
Refer to 14.7 “Interrupt Control” for details of interrupt control. Table 18.11 lists Timer B Interrupt Related Registers.

Table 18.11 Timer B Interrupt Related Registers

Address	Register Name	Register Symbol	After Reset
0045h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
0046h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
0047h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
0206h	Interrupt Source Select Register 2	IFSR2A	00h

Timers B3 and B4 share interrupt vectors and interrupt control registers with other peripheral functions. When using the timer B3 interrupt, set the IFSR26 bit in the IFSR2A register to 0 (timer B3). When using the timer B4 interrupt, set the IFSR27 bit in the IFSR2A register to 0 (timer B4).

18.5 Notes on Timer B

18.5.1 Timer B (Timer Mode)

18.5.1.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using registers TBiMR, TBi, TBCS0 to TBCS3, TCKDIVC0, and PCLKR before setting the TBiS bit in the TABSR or the TBSR register to 1 (count starts) (i = 0 to 5).

Always make sure registers TBiMR, TBCS0 to TBCS3, TCKDIVC0, and PCLKR are modified while the TBiS bit is 0 (count stops), regardless of whether after reset or not.

18.5.1.2 Read from Timer

The value of the counter while counting can be read from the TBi register at any time. FFFFh is read while reloading. If the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

18.5.2 Timer B (Event Counter Mode)

18.5.2.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TBiMR register and TBi register before setting the TBiS bit in the TABSR or the TBSR register to 1 (count starts) (i = 0 to 5).

Always make sure the TBiMR register is modified while the TBiS bit is 0 (count stops), regardless of whether after reset or not.

18.5.2.2 Read from Timer

While counting is in progress, the counter value can be read out at any time by reading the TBi register. However, if this register is read at the same time the counter is reloaded, the read value is always FFFFh. If the TBi register is read after setting a value in it while not counting but before the counter starts counting, the read value is the value set in the register.

18.5.3 Timer B (Pulse Period/Pulse Width Measurement Modes)

18.5.3.1 Register Setting

The timer is stopped after reset. Set the mode, count source, etc., using registers TBiMR, TBCS0 to TBCS3, TBi, TCKDIVC0, PCLKR, PPWFS1, and PPWFS2 before setting the TBiS bit in the TABSR or TBSR register to 1 (count starts) (i = 0 to 5).

Always make sure registers TBiMR, TBCS0 to TBCS3, TCKDIVC0, PCLKR, PPWFS1, and PPWFS2 are modified while the TBiS bit is 0 (count stops), regardless of whether after reset or not. To clear the MR3 bit to 0 by writing to the TBiMR register while the TBiS bit is 1 (count starts), be sure to write the same value as previously written to bits TMOD0, TMOD1, MR0, MR1, TCK0, and TCK1 and a 0 to bit 4.

18.5.3.2 Interrupts

The IR bit in the TBiIC register is set to 1 (interrupt requested) when an active edge of a measurement pulse is input or timer Bi overflows (i = 0 to 5). The source of an interrupt request can be determined by using the MR3 bit in the TBiMR register within the interrupt routine.

Use the IR bit in the TBiIC register to detect overflows only. Use the MR3 bit only to determine the interrupt source.

18.5.3.3 Operations between Count Start and the First Measurement

When a count is started and the first active edge is input, an undefined value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.

The value of the counter is undefined after reset. If count is started in this state, the MR3 bit may be set to 1 and timer Bi interrupt request may be generated after count start before an effective edge is input. When a value is set in the TBi register while the TBiS bit is 0 (count stops), the same value is written to the counter.

18.5.3.4 Pulse Period Measurement Mode

When an overflow occurs at an active edge, an input is not recognized at the effective edge because an interrupt request is generated only once. Use this mode where an overflow does not occur, or use pulse width measurement.

18.5.3.5 Pulse Width Measurement Mode

In pulse width measurement, pulse widths are measured successively. Use a program to check whether the measurement result is a high-level width or a low-level width.

When an interrupt request is generated, read the TBiIN pin level inside the interrupt routine, and check whether it is the edge of an input pulse or an overflow. The TBiIN level can be read from bits in the P9 register of corresponding ports.

19. Three-Phase Motor Control Timer Function

Note

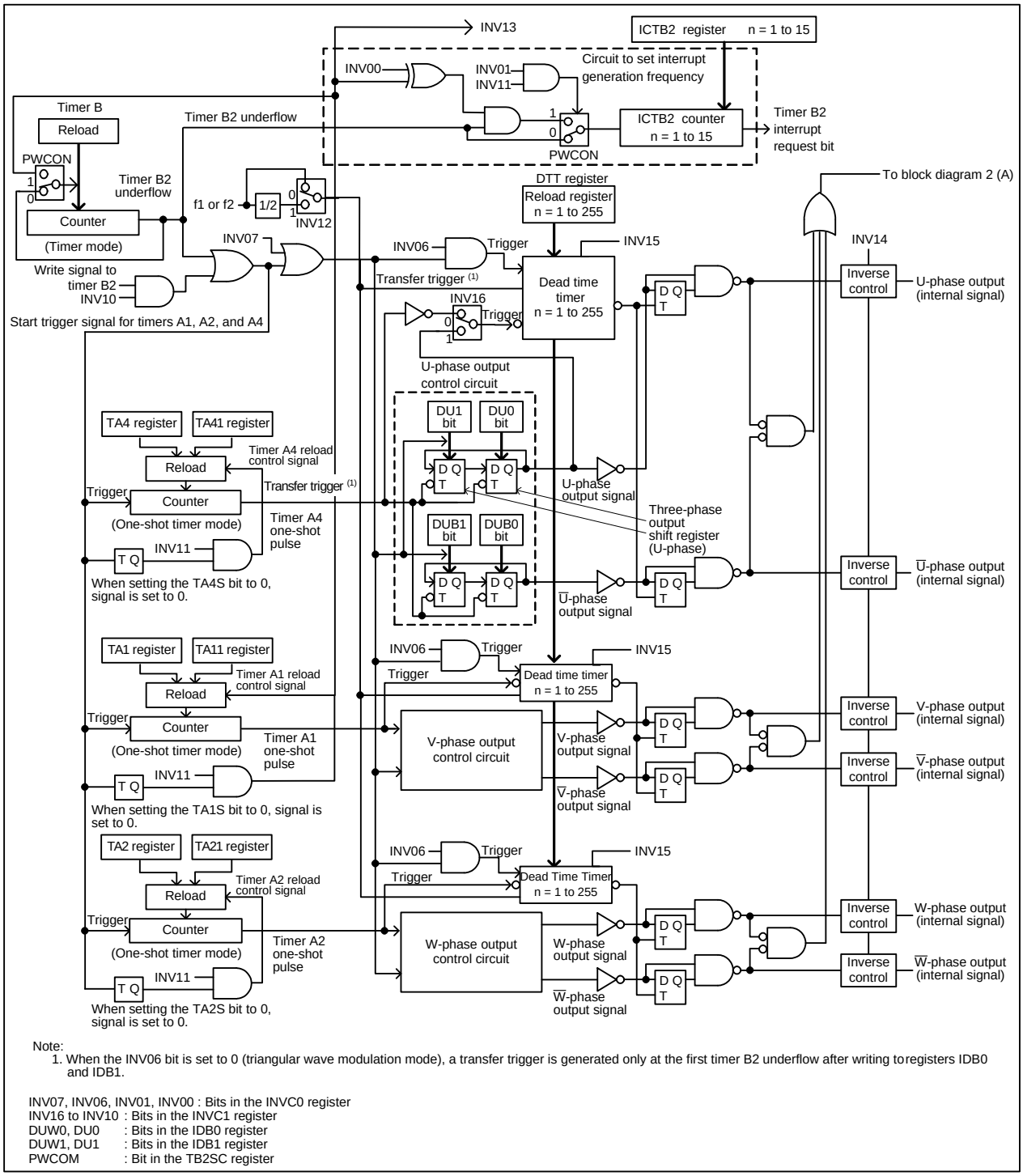
Do not use this function for the 80-pin package.

19.1 Introduction

Timers A1, A2, A4, and B2 can be used to output three-phase motor drive waveforms.
Table 19.1 lists Three-Phase Motor Control Timer Functions Specifications. Three-Phase Motor Control Timer Function Block Diagrams are shown in Figure 19.1 and Figure 19.2. Table 19.2 lists I/O Ports.

Table 19.1 Three-Phase Motor Control Timer Functions Specifications

Item	Specification
Operation modes	• Triangular wave modulation three-phase mode 0 Three-phase PWM waveform of triangular wave modulation is output. Output data is updated every half cycle of the carrier wave, and output waveform is generated. • Triangular wave modulation three-phase mode 1 Three-phase PWM waveform of triangular wave modulation is output. Output data is updated every cycle of the carrier wave, and output waveform is generated. • Sawtooth wave modulation mode Three-phase PWM waveform of sawtooth wave modulation is output.
Three-phase waveform output pin	Six pins (U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$)
Forced cutoff input	Input a low-level signal to the $\overline{SD}$ pin
Used timers	Timers A4, A1, A2 (used in one-shot timer mode) Timer A4: U-/$\overline{U}$-phase waveform control Timer A1: V-/$\overline{V}$-phase waveform control Timer A2: W-/$\overline{W}$-phase waveform control Timer B2 (used in timer mode) Carrier wave cycle control Dead time timer (three eight-bit timers and shared reload register) Dead time control
Output waveform	Triangular wave modulation, sawtooth wave modulation • All high or low outputs for one cycle supported • Output logic of high- and low-side turn-on signals can be set separately.
Carrier wave cycle	Triangular wave modulation : $\frac{(m+1)\times 2}{fi}$ Sawtooth wave modulation : $\frac{m+1}{fi}$ m: Setting value of the TB2 register, 0000h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width	Triangular wave modulation : $\frac{n\times 2}{fi}$ Sawtooth wave modulation : $\frac{n}{fi}$ n: Setting value of registers TA4, TA1, and TA2 (of registers TA4, TA41, TA1, TA11, TA2, and TA21 when setting the INV11 bit to 1), 0001h to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Dead time (width)	$\frac{p}{fi}$ or no dead time p: Setting value of the DTT register, 01h to FFh fi: Count source frequency (f1TIMAB, f2TIMAB, f1TIMAB divided by 2, f2TIMAB divided by 2)
Active level	Selectable either active high or active low
Simultaneous conduction prevention function	Simultaneous conduction prevention Simultaneous conduction detection
Interrupt frequency	Timer B2 interrupt is generated every carrier wave cycle to every 15 carrier wave cycles.



Note:
1. When the INV06 bit is set to 0 (triangular wave modulation mode), a transfer trigger is generated only at the first timer B2 underflow after writing to registers IDB0 and IDB1.

INV07, INV06, INV01, INV00 : Bits in the INVC0 register
INV16 to INV10 : Bits in the INVC1 register
DUW0, DU0 : Bits in the IDB0 register
DUW1, DU1 : Bits in the IDB1 register
PWCOM : Bit in the TB2SC register

Figure 19.1 Three-Phase Motor Control Timer Function Block Diagram 1

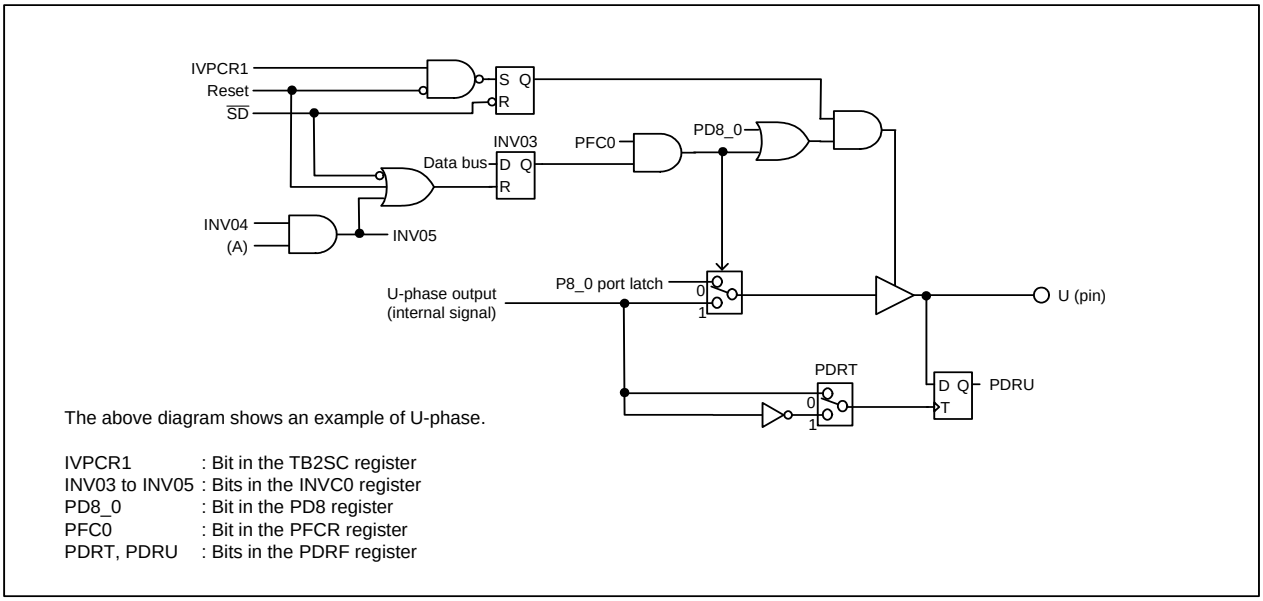


Figure 19.2 Three-Phase Motor Control Timer Function Block Diagram 2

Table 19.2 I/O Ports

Pin Name	I/O Type	Function
U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	Output	Three-phase PWM waveform output
$\overline{SD}$	Input (1)	Forced cutoff input
IDU, IDV, IDW	Input (2)	Position-data-retain function input

Notes:
1. Set the port direction bits which share pins to 0 (input mode). When not using the three-phase output forced cutoff function, input a high-level signal to the $\overline{SD}$ pin.
2. Set the port direction bits which share pins to 0 (input mode).

19.2 Registers

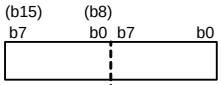
Refer to “registers used and settings” in each mode for register and bit settings.
Three-phase motor control timer function uses timers A1, A2, A4, and B2. For other registers related to A1, A2, A4, and B2, refer to 17. “Timer A” and 18. “Timer B”.

Table 19.3 Register Structure

Address	Register Name	Register Symbol	After Reset
01DAh	Three-Phase Protect Control Register	TPRC	00h
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
0318h	Port Function Control Register	PFCR	0011 1111b
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
033Eh	Timer B2 Special Mode Register	TB2SC	XXXX XX00b

19.2.1 Timer B2 Register (TB2)

Timer B2 Register



Symbol	Address	After Reset
TB2	0335h to 0334h	Undefined

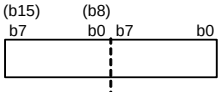
Function	Setting Range	RW
If setting value is n, counter frequency is $\frac{n+1}{fj}$ Timers A1, A2, and A4 start every time an underflow occurs.	0000h to FFFFh	RW

fj : Count source frequency

Read and write in 16-bit units.
Carrier wave cycle is determined by this counter. Timer B underflow is a one-shot trigger of timers A1, A2, and A4.
In three-phase mode 1, the reload timing of the TB2 register can be selected by the PWCON bit in the TB2SC register.

19.2.2 Timer Ai, Ai-1 Register (TAi, TAi1) (i = 1, 2, 4)

Timer Ai, Ai-1 Register (i = 1, 2, 4)



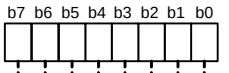
Symbol	Address	After Reset
TA1, TA2, TA4	0329h to 0328h, 032Bh to 032Ah, 032Fh to 032Eh	Undefined
TA11, TA21, TA41	0303h to 0302h, 0305h to 0304h, 0307h to 0306h	Undefined

Function	Setting Range	RW
If the setting value is n, the timer stops when the nth count source is counted after a start trigger is generated. Output signals of each phase change when timers A1, A2, and A4 stop.	0000h to FFFFh	WO

Write to this register in 16-bit units. Use the MOV instruction to set registers TAi and TAi1. If the TAi or TAi1 register is set to 0000h, no counters start and no timer Ai interrupt is generated.
The TAi or TAi1 register is used to determine waveforms of U-, V-, and W-phases. It is triggered by timer B underflow, and operates in one-shot timer mode.
Registers TA1, TA2, and TA4 are used in sawtooth wave modulation mode and three-phase mode 0 of triangular wave modulation mode.
Registers TA1, TA2, TA4, TA11, TA21, and TA41 are used in three-phase mode 1 of triangular wave modulation mode.
When the INV15 bit in the INVC1 register is set to 0 (dead time enabled), some high- and low-side turn-on signals, whose output level changes from inactive to active, switch the output level when the dead time timer stops.
In three-phase mode 1, the value of the TAi1 register is first counted. Then the values of registers TAi and TAi1 are counted alternately.

19.2.3 Three-Phase PWM Control Register 0 (INVC0)

Three-Phase PWM Control Register 0



Symbol: INVC0 | Address: 0308h | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
INV00	ICTB2 count condition select bit	b1 b0 0 0 } : Timer B2 underflow 0 1 } 1 0 : Timer B2 underflow when timer A1 reload control signal is 0 1 1 : Timer B2 underflow when timer A1 reload control signal is 1	RW
INV01			RW
INV02	Three-phase motor control timer function enable bit	0 : Three-phase motor control timer function not used 1 : Three-phase motor control timer function used	RW
INV03	Three-phase motor control timer output control bit	0 : Three-phase motor control timer output disabled 1 : Three-phase motor control timer output enabled	RW
INV04	High- and low-side simultaneous turn-on disable bit	0 : Simultaneous turn-on enabled 1 : Simultaneous turn-on disabled	RW
INV05	High- and low-side simultaneous turn-on detect flag	0 : Not detected 1 : Detected	RW
INV06	Modulation mode select bit	0 : Triangular wave modulation mode 1 : Sawtooth wave modulation mode	RW
INV07	Software trigger select bit	Transfer trigger is generated when the INV07 bit is set to 1. Trigger to the dead time timer is also generated when setting the INV06 bit to 1. Read as 0.	RW

Set the INVC0 register after the PRC1 bit in the PRCR register is set to 1 (write enabled). Rewrite bits INV00 to INV02, INV04, and INV06 when timers A1, A2, A4, and B2 are stopped.

INV01-INV00 (ICTB Count Condition Select Bit) (b1-b0)

Bits INV00 and INV01 are enabled only when the INV11 bit is set to 1 (three-phase mode 1).
To set the INV01 bit to 1, set the value of the ICTB2 register first, and then set the INV01 bit to 1. Set the TAIS bit in the TABSR register (timer A1 count start flag) to 1 prior to the first timer B2 underflow.
When the INV11 bit is 0 (three-phase mode 0), the timer B2 underflow is counted regardless of the values of bits INV01 and INV00.

INV02 (Three-Phase Motor Control Timer Function Enable Bit) (b2)

Set the INV02 bit to 1 to operate the dead time timer, U-, V- and, W-phase output control circuits and ICTB2 counter.

INV03 (Three-Phase Motor Control Timer Output Control Bit) (b3)

Conditions to become 0:

- Reset
- The INV04 bit is 1 (simultaneous turn-on disabled) and the INV05 bit is 1 (simultaneous turn-on detected).
- The INV03 bit is set to 0 by a program.
- A signal applied to the $\overline{SD}$ pin is low.

INV05 (High- and Low-Side Simultaneous Turn-On Detect Flag) (b5)

The INV05 bit cannot be set to 1 by a program. Set the INV04 bit to 0 as well when setting the INV05 bit to 0.

INV06 (Modulation Mode Select Bit) (b6)

The following table describes the influence the INV06 bit.

Table 19.4 INV06 Bit

Item	INV06 = 0	INV06 = 1
Mode	Triangular wave modulation mode	Sawtooth wave modulation mode
Transfer timing from registers IDB0 and IDB1 to three-phase output shift register	Transferred once by generating a transfer trigger after setting registers IDB0 and IDB1	Transferred every time a transfer trigger is generated
Trigger timing of the dead time timer when the INV16 bit is 0	Falling edge of a one-shot pulse of the timers A1, A2, or A4	• Falling edge of a one-shot pulse of the timer A1, A2, or A4 • Transfer trigger
INV13 bit	Enabled when the INV11 bit is 1 and the INV06 bit is 0	Disabled

One of the following conditions must be met to trigger a transfer:

- Timer B2 underflows and a value is written to the INV07 bit
- A value is written to the TB2 register when the INV10 bit is 1

19.2.4 Three-Phase PWM Control Register 1 (INVC1)

Three-Phase PWM Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	After Reset
0	INVC1	0309h	00h

Bit Symbol	Bit Name	Function	RW
INV10	Timer A1, A2 and A4 start trigger select bit	0 : Timer B2 underflow 1 : Timer B2 underflow and write to timer B2	RW
INV11	Timer A1-1, A2-1 and A4-1 control bit	0 : Three-phase mode 0 1 : Three-phase mode 1	RW
INV12	Dead time timer count source select bit	0 : f1TIMAB or f2TIMAB 1 : f1TIMAB divided by 2 or f2TIMAB divided by 2	RW
INV13	Carrier wave rise/fall detect flag	0 : Timer A1 reload control signal is 0. 1 : Timer A1 reload control signal is 1.	RO
INV14	Active level control bit	0 : Active low 1 : Active high	RW
INV15	Dead time disable bit	0 : Dead time enabled 1 : Dead time disabled	RW
INV16	Dead time timer trigger select bit	0 : Falling edge of one-shot pulse of timer (A4, A1 and A2) 1 : Rising edge of the three-phase output shift register (U-, V-, W-phase) output	RW
— (b7)	Reserved bit	Set to 0	RW

Rewrite the INVC1 register after the PRC1 bit in the PRCR register is set to 1 (write enabled).
Rewrite the INVC1 register while timers A1, A2, A4, and B2 are stopped.

INV11 (Timer A1, A2 and A4 Start Trigger Select Bit) (b1)

The following table lists items influenced by the INV11 bit.

Table 19.5 INV11 Bit

Item	INV11 = 0	INV11 = 1
Mode	Three-phase mode 0	Three-phase mode 1
Registers TA11, TA21 and TA41	Not used	Used
Bits INV00 and INV01 in the INVC0 register	Disabled The ICTB2 counter is decremented whenever timer B2 underflows	Enabled
INV13 bit	Disabled	Enabled when INV11 is 1 and INV06 is 0

When the INV06 bit is set to 1 (sawtooth wave modulation mode), set the INV11 bit to 0 (three-phase mode 0). Also, when the INV11 bit is set to 0, set the PWCON bit in the TB2SC register to 0 (timer B2 is reloaded when timer B2 underflows).

INV13 (Carrier Wave Rise/Fall Detect Flag) (b3)

The INV13 bit is enabled only when the INV06 bit is set to 0 (triangular wave modulation mode) and the INV11 bit to 1 (three-phase mode 1).

INV16 (Dead Time Timer Trigger Select Bit) (b6)

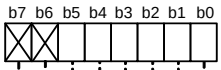
If both of the following conditions are met, set the INV16 bit to 1 (rising edge of the three-phase output shift register output).

- The INV15 bit is set to 0 (dead time timer enabled)
- The Dij bit and DiBj bit always have different values when the INV03 bit is set to 1 (three-phase control timer output enabled). (The high- and low-side signals always output opposite level signals at any time except dead time.) (i = U, V or W; j = 0, 1).

If either of the above conditions is not met, set the INV16 bit to 0 (dead time timer is triggered on the falling edge of a one-shot pulse of timers).

19.2.5 Three-Phase Output Buffer Register i (IDBi) (i = 0, 1)

Three-Phase Output Buffer Register i (i = 0, 1)



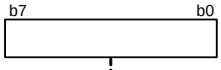
Symbol	Address	After Reset
IDB0	030Ah	XX11 1111b
IDB1	030Bh	XX11 1111b

Bit Symbol	Bit Name	Function	RW
DUi	U-phase output buffer i	Set the output logical value of the three-phase output shift registers. The set value is reflected in each turn-on signal as follows: 0 : Active (on) 1 : Inactive (off) When read, the contents of the three-phase output shift registers are read.	RW
DUBi	$\overline{U}$-phase output buffer i		RW
DVi	V-phase output buffer i		RW
DVBi	$\overline{V}$-phase output buffer i		RW
DWi	W-phase output buffer i		RW
DWBi	$\overline{W}$-phase output buffer i		RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as undefined value		—

Values of registers IDB0 and IDB1 are transferred to the three-phase output shift register in response to a transfer trigger. After the transfer trigger occurs, the values written in the IDB0 register determine each phase output signal (internal signal) first. Then, the value written in the IDB1 register on the falling edge of timers A1, A2, and A4 one-shot pulse determines each phase output signal (internal signal). Reading registers IDB0 and IDB1 returns each phase output signal (internal signal). Therefore, the same value is returned regardless of which register is read.

19.2.6 Dead Time Timer (DTT)

Dead Time Timer



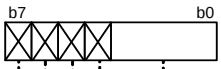
Symbol	Address	After Reset
DTT	030Ch	Undefined

Function	Setting Range	RW
If a setting value is n, the count source is counted n times after the start trigger occurs, and then the timer stops.	1 to 255	WO

Use the MOV instruction to set the DTT register.
The DTT register acts as a one-shot timer which delays the timing for a turn-on signal to be switched to its active level in order to prevent the upper and lower transistors from being turned on simultaneously.
The DTT register is enabled when the INV15 bit in the INVC1 register is set to 0 (dead time enabled). No dead time can be set when the INV15 bit is set to 1 (dead time disabled).
Select a trigger by the INV16 bit in the INVC1 register, and a count source by the INV12 bit in the INVC1 register.

19.2.7 Timer B2 Interrupt Generation Frequency Set Counter (ICTB2)

Timer B2 Interrupt Generation Frequency Set Counter



Symbol	Address	After Reset
ICTB2	030Dh	Undefined

Function	Setting Range	RW
When a setting value is n, timer B2 interrupt is generated every nth count timer B2 underflow meets the condition selected by bits INV01 and INV00.	1 to 15	WO
No register bits. If necessary, set to 0		—

Use the MOV instruction to set the ICTB2 register.
If the INV01 bit in the INVC0 register is set to 1, set the ICTB2 register when the TB2S bit in the TABSR register is set to 0 (timer B2 counter stopped). If the INV01 bit is set to 0 and the TB2S bit to 1 (timer B2 counter start), do not set the ICTB2 register when timer B2 underflows.
When bits INV01 and INV00 are 11b, the first interrupt is generated when timer B2 underflows n-1 times if a setting value in the ICTB2 counter is n. Subsequent interrupts are generated every n times timer B2 underflows.

19.2.8 Timer B2 Special Mode Register (TB2SC)

Timer B2 Special Mode Register

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	After Reset
	TB2SC	033Eh	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
PWCON	Timer B2 reload timing switch bit	0 : Timer B2 underflow 1 : Timer A output at odd-numbered occurrences	RW
IVPCR1	Three-phase output port $\overline{SD}$ control bit 1	0 : Three-phase output forced cutoff by $\overline{SD}$ input (high-impedance) disabled 1 : Three-phase output forced cutoff by $\overline{SD}$ input (high-impedance) enabled	RW
— (b6-b2)	Reserved bits	Set to 0	RW
— (b7)	No register bits. If necessary, set to 0. Read as 0		—

Write to this register after the PRC1 bit in the PRCR register is set to 1 (write enabled).

PWCON (Timer B2 Reload Timing Switch Bit) (b0)

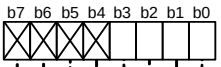
If the INV11 bit is 0 (three-phase mode 0) or the INV06 bit is 1 (sawtooth wave modulation mode), set the PWCON bit to 0 (timer B2 underflow).

IVPCR1 (Three-Phase Output Port SD Control Bit 1) (b1)

Related pins are U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$.
If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit is 1, three-phase motor control timer output is disabled (INV03 = 0). Then, the target pins go to a high-impedance state regardless of which functions of those pins are being used.
After forced cutoff, input a high-level signal to the $\overline{SD}$ pin and set the IVPCR1 bit to 0 to cancel forced cutoff.

19.2.9 Position-Data-Retain Function Control Register (PDRF)

Position-Data-Retain Function Control Register



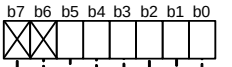
Symbol	Address	After Reset
PDRF	030Eh	XXXX 0000b

Bit Symbol	Bit Name	Function	RW
PDRW	W-phase position data retain bit	Input level at IDW pin is retained. 0: Low level 1: High level	RO
PDRV	V-phase position data retain bit	Input level at IDV pin is retained. 0: Low level 1: High level	RO
PDRU	U-phase position data retain bit	Input level at IDU pin is retained. 0: Low level 1: High level	RO
PDRT	Retain-trigger polarity select bit	Select polarity of a retain-trigger 0: Rising edge of high-side output signal 1: Falling edge of high-side output signal	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value		RW

This register is valid in three-phase mode only.

19.2.10 Port Function Control Register (PFCR)

Port Function Control Register



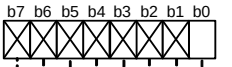
Symbol	Address	After Reset
PFCR	0318h	0011 1111b

Bit Symbol	Bit Name	Function	RW
PFC0	Port P8_0 output function select bit	0: Input/output port P8_0 1: Three-phase PWM output (U-phase output)	RW
PFC1	Port P8_1 output function select bit	0: Input/output port P8_1 1: Three-phase PWM output ($\overline{U}$-phase output)	RW
PFC2	Port P7_2 output function select bit	0: Input/output port P7_2 1: Three-phase PWM output (V-phase output)	RW
PFC3	Port P7_3 output function select bit	0: Input/output port P7_3 1: Three-phase PWM output ($\overline{V}$-phase output)	RW
PFC4	Port P7_4 output function select bit	0: Input/output port P7_4 1: Three-phase PWM output (W-phase output)	RW
PFC5	Port P7_5 output function select bit	0: Input/output port P7_5 1: Three-phase PWM output ($\overline{W}$-phase output)	RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as 0		—

This register is valid only when the INV03 bit in the INVC0 register is set to 1 (three-phase motor control timer output enabled). Write to this register after the TPRC0 bit in the TPRC register is set to 1 (write enabled).

19.2.11 Three-Phase Protect Control Register (TPRC)

Three-Phase Protect Control Register



Symbol	Address	After Reset
TPRC	01DAh	00h

Bit Symbol	Bit Name	Funtion	RW
TPRC0	Three-phase protect control bit	Enable write to the PFCR register 0: Write disabled 1: Write enabled	RW
— (b7-b1)	No register bits. If necessary, set to 0. Read as 0		—

Once the TPRC0 bit is set to 1 (write enabled) by a program, the set value 1 is retained. To change the registers protected by this bit, follow the steps below.

(1) Set the TPRC0 bit to 1.
(2) Set values in the PFCR register.
(3) Set the TPRC0 bit to 0 (write disabled).

19.3 Operations

19.3.1 Common Operations in Multiple Modes

19.3.1.1 Carrier Wave Cycle Control

Timer B2 controls the cycle of the carrier wave. In triangular wave modulation mode, the cycle of the carrier wave is double the cycle of timer B2 underflow. In sawtooth wave modulation mode, the cycle of carrier wave equals to the cycle of timer B2 underflow. Figure 19.3 shows Relationship between Carrier Wave Cycle and Timer B2.

Timer B2 underflow is a start trigger for timers A1, A2, and A4, which control the three-phase PWM waveform. However, when the INV10 bit in the INVC1 register is 1, writing to the TB2 register also generates a trigger for timers A1, A2, and A4.

The frequency of timer B2 interrupt requests can be selected for three-phase motor control timers.

In triangular wave modulation three-phase mode 0 and sawtooth wave modulation mode, when a setting value in the ICTB2 register is n, the timer B2 interrupt request is generated every nth count of timer B2 underflow.

In triangular wave modulation three-phase mode 1, when a setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth time of the timing selected by bits INV01 and INV00 in the INVC1 register. However, when bits INV01 and INV00 are 11b, the first interrupt is generated at the n-1th time of timer B2 underflow.

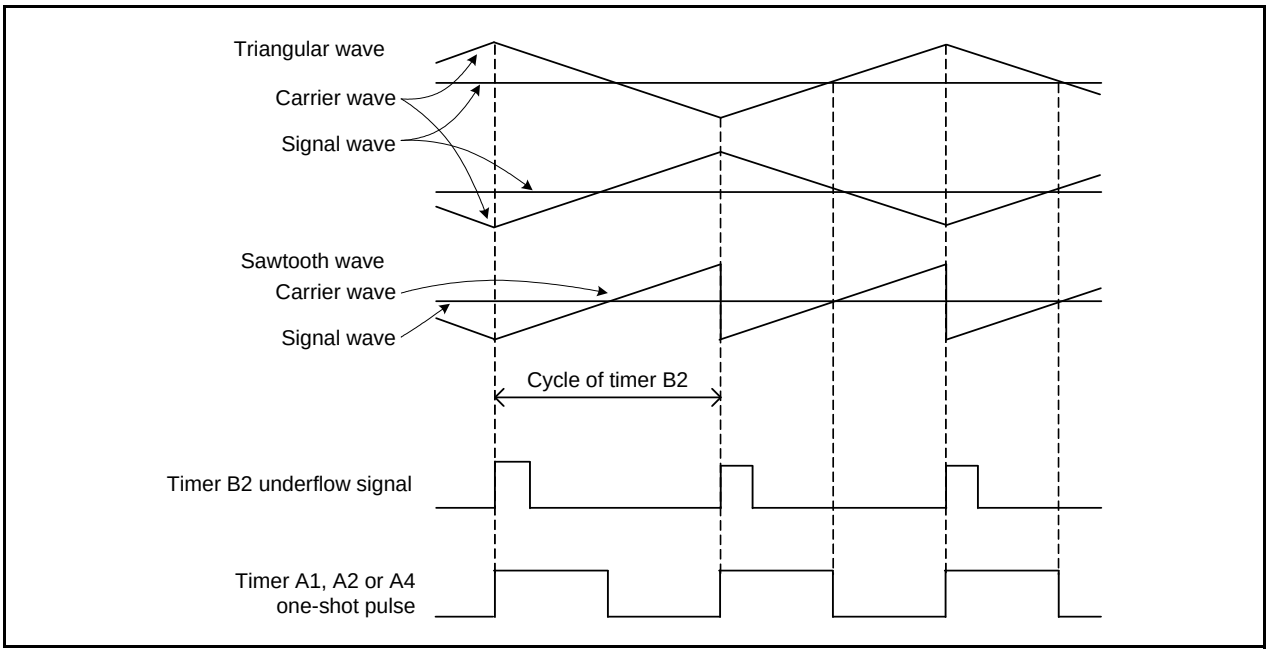


Figure 19.3 Relationship between Carrier Wave Cycle and Timer B2

19.3.1.2 Three-Phase PWM Wave Control

Timer A4 controls U- and $\overline{U}$-phase waveforms, timer A1 controls V- and $\overline{V}$-phase waveforms, and timer A2 controls W- and $\overline{W}$-phase waveforms. Timer Ai (i = 1, 2, 4) starts counting by a trigger selected by the INV10 bit in the INVC1 register, and generates a one-shot pulse (internal signal). The output signal of each phase changes at the falling edge of the one-shot pulse.
Triangular wave modulation three-phase mode 1 counts values in the TAi1 register and TAi register alternately, and generates a one-shot pulse.

19.3.1.3 Dead Time Control

Due to delays in the transistors turning off, the upper and lower transistors are turned on simultaneously. To prevent this, there are three 8-bit dead time timers, one in each phase. The reload resistor is shared. When the INV15 bit in the INVC1 register is 0 (dead time enabled), the dead time set in the DTT register is valid. When the INV15 bit is 1 (dead time disabled), no dead time is set.
Select a count source for the dead time timer by the INV12 bit in the INVC1 register.
A trigger for the dead time timer can be selected by the INV16 bit in the INVC1 register.
When both conditions below are met, set the INV16 bit to 1 (the rising edge of the three-phase output shift register is a trigger for the dead time timer).

- The INV15 bit is 0 (dead time enabled).
- The Dij bit and DiBj bit have different values whenever the INV03 bit is set to 1 (three-phase motor control timer output enabled) (i = U, V or W; j = 0, 1). (During the period except dead time, the high- and low-side output signals always output opposite level signals.)

If either of the conditions above is not met, set the INV16 bit to 0 (a trigger for the dead time timer is the falling edge of one-shot pulse of the timer).
In sawtooth wave modulation mode, the generation of a transfer trigger causes a trigger for the dead time timer.

19.3.1.4 Output Level of Three-Phase PWM Output Pins

Set a value in registers IDB0 and IDB1 to select the state of each high- or low-side output signal (either active (on) or not active (off)). The values of registers IDB0 and IDB1 are transferred to the three-phase output shift register by a transfer trigger. After a transfer trigger is generated, the value set in the IDB0 register becomes the first output signal of each phase (internal signal), and then at the falling edge of one-shot pulse of timer A1, A2, or A4 (internal signal), the value set in the IDB1 register becomes the output signal of each phase.
A transfer trigger is generated under any of the following conditions:

- At the first timer B2 underflow after registers IDB0 and IDB1 are written (in triangular wave modulation mode)
- Each time timer B2 underflows (in sawtooth wave modulation mode)
- Writing to the TB2 register (when the INV10 bit in the INVC1 register is 1)
- Setting the INV07 bit in the INVC0 register to 1 (software trigger)

The active level can be selected by the INV14 bit in the INVC1 register.

Table 19.6 Output Level of Three-Phase PWM Output Pins

Value Set in Registers IDB0 and IDV1	Output Signal of Each Phase (Internal Signal)	Value Set in INV14 Bit in INVC1 Register	
		0 (active, low level)	1 (active, high level)
0 (active (on))	0	Low	High
1 (not active (off))	1	High	Low

19.3.1.5 Simultaneous Conduction Prevention

This function prevents the upper and lower output signals from being active simultaneously due to program errors or an unexpected program operation. When the high- and low-side output signals become active at the same time while the simultaneous conduction is disabled by the INV04 bit in the INVC0 register, the following occur:

- The INV03 bit in the INVC0 register becomes 0 (three-phase motor control timer output disabled).
- The INV05 bit in the INVC0 register becomes 1 (simultaneous conduction detected).
- Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ go to a high-impedance state.

19.3.1.6 Three-Phase PWM Waveform Output Pins

Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ output the PWM waveform under the following conditions:

- The INVC02 bit in the INVC0 register is 1 (three-phase motor control timer function).
- The INVC03 bit is 1 (three-phase motor control timer output enabled).
- The PFCi bit in the PFCR register is 1 (three-phase PWM output (selected independently for each pin)).

The three-phase output forced cutoff by the $\overline{SD}$ pin is available.

19.3.1.7 Three-Phase PWM Output Pin Select

Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ output the three-phase PWM waveform when the PFCi bit (i = 0 to 5) in the PFCR register is 1 (three-phase PWM output). When the PFCi bit is 0 (I/O port), these pins are used as I/O ports (or other peripheral function I/O ports). Therefore, while some of the six pins output the three-phase PWM waveform, the other pins can be used as I/O ports (or other peripheral function I/O ports).

The PFCR register can be rewritten when the TPRC0 bit in the TPRC register is 1 (write to the PFCR register enabled). The functions of the three-phase PWM waveform output pins are protected from being rewritten due to an unexpected program operation. To prevent rewrite, follow these steps:

(1) Set the TPRC0 bit to 1.
(2) Rewrite the PFCR register.
(3) Set the TPRC0 bit to 0 (write to the PFCR register disabled).

Figure 19.4 shows Usage Example of Three-Phase Output and I/O Port Switch Function.

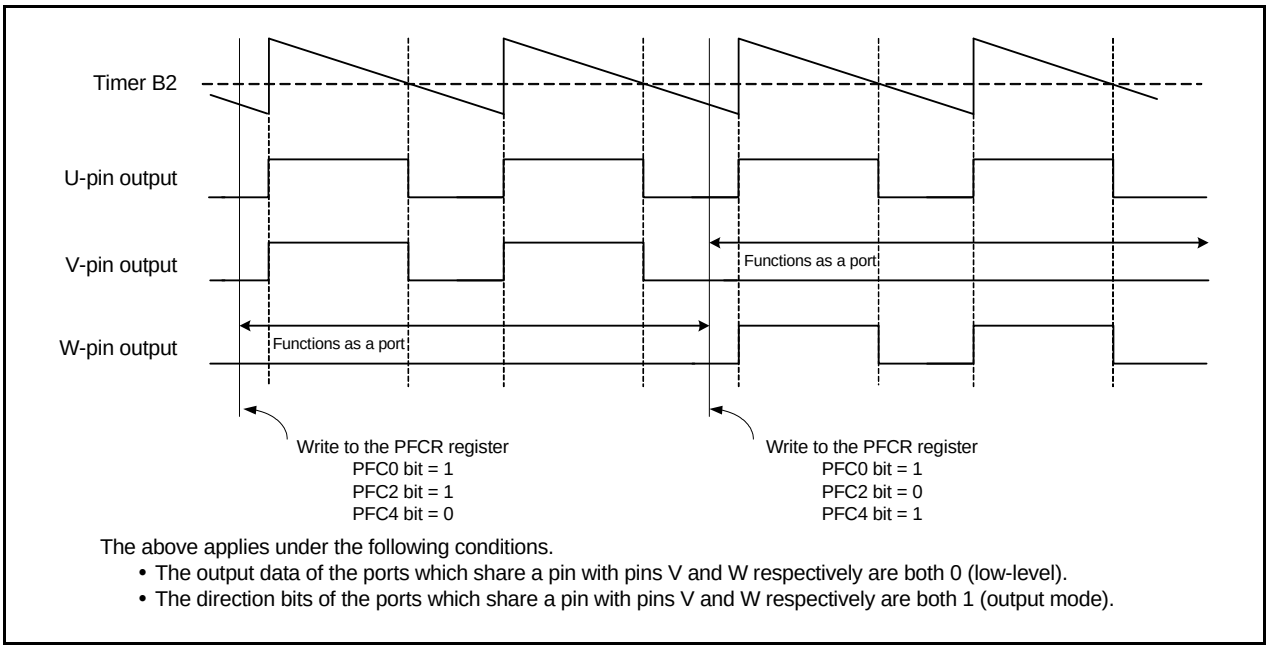


Figure 19.4 Usage Example of Three-Phase Output and I/O Port Switch Function

19.3.1.8 Three-Phase Output Forced Cutoff Function

While the INV02 bit in the INVC0 register is 1 (three-phase motor control timer function) and the INV03 bit is 1 (three-phase motor control timer output enabled), when a low-level signal is applied to the $\overline{SD}$ pin, the INV03 bit in the INVC0 register becomes 0 (three-phase motor control timer output disabled), and pins corresponding to U, $\overline{U}$, V, $\overline{V}$, W and $\overline{W}$ outputs change all together as follows:

- When the IVPCR1 bit in the TB2SC register is 1 (three-phase output forced cutoff enabled)
  High-impedance state
- When the IVPCR1 bit in the TB2SC register is 0 (three-phase output forced cutoff disabled)
  I/O ports or other peripheral function I/O ports

However, applying a low-level signal to the $\overline{SD}$ pin while the IVPCR1 bit is 1 places the pins in a high-impedance state even when the pins are used as functions other than U, $\overline{U}$, V, $\overline{V}$, W and $\overline{W}$ outputs. Table 19.7 lists State of Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$.

Table 19.7 State of Pins U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$

State of Bit and Pin		Function or State of Pins U, $\overline{U}$, V, $\overline{V}$, W and $\overline{W}$
IVPCR1 bit in TB2SC register	$\overline{SD}$ input	
1	High	Three-phase PWM output
	Low	High-impedance
0	High	Three-phase PWM output
	Low	I/O port or other peripheral functions

Note:
1. In the above case, bits INVC02, INVC03 and PFCi are all 1.

The digital filter is available for the $\overline{SD}$ pin. When the value of bits NMIDF2 to NMIDF0 in the NMIDF register is other than 000b (digital filter enabled), the $\overline{SD}$ level is sampled for every sampling clock. When the same sampled level is detected three times in a row, the level is transferred to the internal circuit. Refer to 13.4.3 "$\overline{NMI}$/$\overline{SD}$ Digital Filter".

To return the pin function to the three-phase PWM output after the forced cutoff, follow these steps below:

(1) Apply a high-level signal to the $\overline{SD}$ pin.
(2) Wait for more than three cycles of the digital filter sampling clock.
(3) Set the INV03 bit in the INVC0 register to 1 (three-phase motor control timer output enabled).
(4) Confirm that the INV03 bit is 1. If the bit is 0, return to step 3.
(5) Set the IVPCR1 bit to 0 (three-phase output forced cutoff disabled).
(6) Set the IVPCR1 bit to 1 (when enabling three-phase output forced cutoff again).

When not using the three-phase output forced cutoff function, set a port direction bit which shares the pin with $\overline{SD}$ input to 0 (input port), and apply a high-level signal to the $\overline{SD}$ pin.
The same pin is used for both $\overline{SD}$ input and $\overline{NMI}$ input. To disable the $\overline{NMI}$ interrupt, set the PM24 bit in the PM2 register to 0 ($\overline{NMI}$ interrupt disabled).

19.3.1.9 Position-Data-Retain Function

Three position-data input pins for U-, V-, and W-phases are available. Input levels of IDU, IDV and IDW inputs are retained. The falling edge or rising edge of the high-side output signal of each phase can be selected by the PDRT bit in the PDRF register as a position-data-retain trigger.

For example, in the case of U-phase, when the U-phase trigger is generated, the state at the IDU pin is transferred to the PDRU bit in the PDRF register. Until the next trigger of the U-phase waveform output, the value is retained.

Figure 19.5 shows Usage Example of Position-Data-Retain Function (U-Phase).

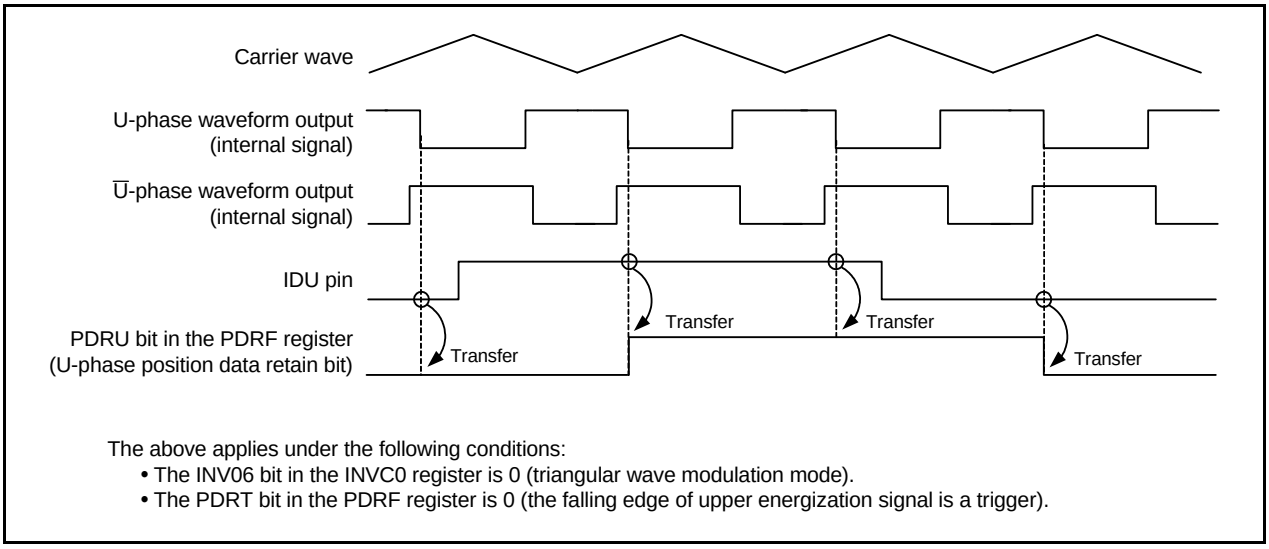


Figure 19.5 Usage Example of Position-Data-Retain Function (U-Phase)

19.3.2 Triangular Wave Modulation Three-Phase Mode 0

Triangular wave modulation uses the timer B2 cycle as a reference cycle. Table 19.8 lists Three-Phase Mode 0 Specifications, and Figure 19.6 shows Usage Example of Three-Phase Mode 0.

Table 19.8 Three-Phase Mode 0 Specifications

Item		Specification
Carrier wave cycle		$\frac{(m+1)\times 2}{fi}$ m: Setting value of the TB2 register, 0 to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width		$\frac{n\times 2}{fi}$ n: Setting value of the TAi register, 1 to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Differences from three-phase mode 1	Reference cycle	Timer B2 cycle (one-half cycle of the carrier wave)
	Timer B2 reload timing	Timer B2 underflow
	Three-phase PWM waveform control	Counts the value of the TAi register every time a timer Ai start trigger is generated (the TAi1 register is not used).
	Timer B2 interrupt	When the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated every nth time of timer B2 underflow (no bits INV00 and INV01 in the INVC1 register).
	Detection of a carrier wave cycle (first half or last half)	Not detected (the INV13 bit in the INVC1 register is invalid).

i = 1, 2, 4

Table 19.9 Registers Used and Settings in Three-Phase Mode 0 (1/2)

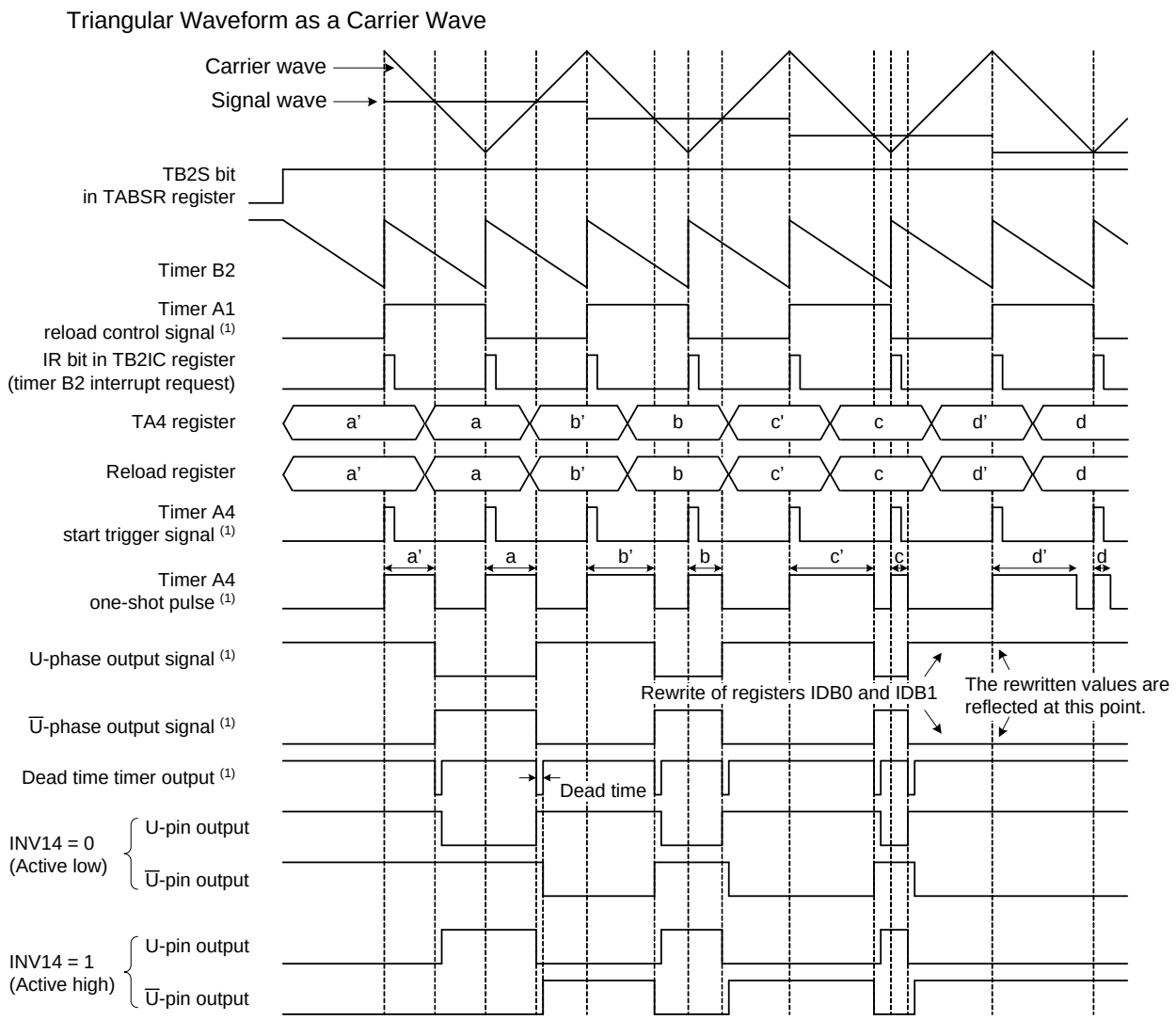
Register	Bit	Functions, Setting Value
INVC0	INV00	Invalid (Despite the settings, the ICTB2 register counts timer B2 underflow.)
	INV01	
	INV02	1 (three-phase motor control timer function used)
	INV03	1 (three-phase motor control timer output enabled)
	INV04	Select simultaneous conduction enabled or disabled.
	INV05	Simultaneous conduction detect flag
	INV06	Set to 0 (triangular wave modulation mode).
	INV07	Software trigger bit
INVC1	INV10	Select a start trigger for timers A1, A2, and A4.
	INV11	Set to 0 (three-phase mode 0).
	INV12	Select a count source for the dead time timer.
	INV13	Invalid
	INV14	Select the active level (either active high or active high).
	INV15	Select the dead time enabled or disabled.
	INV16	Select a trigger for the dead time timer.
	7	Set to 0.
IDB0, IDB1	5 to 0	Set an output logic of the three-phase output shift register.
DTT	7 to 0	Set the dead time.
ICTB2	3 to 0	Set the frequency of timer B2 interrupts.
TB2SC	PWCON	Set to 0 (timer B2 underflow).
	IVPCR1	Select three-phase output forced cutoff enabled or disabled.
	b7 to b2	Set to 0.
PDRF	PDRU, PDRV, PDRW	Position-data-retain bit
	PDRT	Select a position-data-retain trigger.
PFCR	PFC5 to PFC0	Select I/O port or three-phase PWM output.
TPRC	TPRC0	Set to 1 when writing to the PFCR register, or to 0 when not writing to it.
TA1, TA2, TA4	15 to 0	Set the one-shot pulse width.
TA11, TA21, TA41	15 to 0	Not used.
TB2	15 to 0	Set one-half cycle of the carrier wave.
TRGSR	TA1TGH to TA1TGL	01b (when using V-phase output control circuit)
	TA2TGH to TA2TGL	01b (when using W-phase output control circuit)
	TA3TGH to TA3TGL	Not used for three-phase motor control timer.
	TA4TGH to TA4TGL	01b (when using U-phase output control circuit)

i = 1, 2, 4
Note:
1. This table does not show the procedures.

Table 19.10 Registers Used and Settings in Three-Phase Mode 0 (2/2)

Register	Bit	Functions, Setting Value
TABSR	TA0S	Not used for three-phase motor control timer.
	TA1S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA2S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA3S	Not used for three-phase motor control timer.
	TA4S	Set to 1 when starting counting, and to 0 when stopping counting.
	TB0S	Not used for three-phase motor control timer.
	TB1S	Not used for three-phase motor control timer.
	TB2S	Set to 1 when starting counting, and to 0 when stopping counting.
TA1MR, TA2MR, TA4MR	TMOD1 to TMOD0	Set to 10b (one-shot timer mode).
	MR0	Set to 0.
	MR1	Set to 0.
	MR2	1 (Select a trigger by bits TAiTGH and TAiTGL.)
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
TB2MR	TMOD1 to TMOD0	Set to 00b (timer mode).
	MR1 to MR0	Set to 00b.
	4	Set to 0.
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
PCLKR	PCLK0	Select a count source.
TCKDIVC0	TCDIV00	Select a clock prior to timer AB division.
TACS0 to TACS2	7 to 0	Select a count source.
TBCS1	TCS3 to TCS0	Select a count source.
TAPOFS	POFSi	Set to 0.
UDF	TAiP	Set to 0.

i = 1, 2, 4
Note:
1. This table does not show the procedures.



The above applies under the following conditions.
The INVC0 register
- The INV02 bit is 1 (three-phase motor control timer function used).
- The INV03 bit is 1 (three-phase motor control timer output enabled).
- The INV06 bit is 0 (triangular wave modulation mode).

The INVC1 register
- The INV16 bit is 1 (The dead time timer is triggered on the rising edge of the three-phase output shift register).
- The INV15 bit is 0 (dead time timer enabled).
- The INV11 bit is 0 (three-phase mode 0).
- The INV10 bit is 0 (Timer B2 underflow is a start trigger for timers A1, A2 and A4).

The ICTB2 register is 1h (Timer B interrupt request is generated at every timer B2 underflow.).
The PWCOM bit in the TB2CS register is 0 (timer B2 reload at the timing of timer B2 underflow)
Bits PFC1 and PFC0 in the PFCR register are 11b (U-, $\overline{U}$-phase outputs).
The TA4 register
- Initial value : a'
- Changes at every timer B2 interrupt
  1st : a, 2nd : b', 3rd : b, 4th: c', 5th : c, 6th : d', 7th : d

Registers IDB0 and IDB1
- Initial values : DU0 = 1, DUB0 = 0, DU1 = 0, DUB1 = 1
- The values are changed to DU0 = 1, DUB0 = 0, DU1 = 1, DUB1 = 0 at the 6th timer B2 interrupt.

Note:
1. Internal signal. Refer to Figure 19.1.

Figure 19.6 Usage Example of Three-Phase Mode 0

19.3.2.1 Three-Phase PWM Wave Output Timing Control

In three-phase mode 0, when a start trigger for timers A1, A2, and A4 is generated, the counter starts counting the value of the TAi register (i = 1, 2, 4).

19.3.2.2 Three-Phase PWM Waveform Output Level Control

In triangular wave modulation mode, the output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift register by a transfer trigger. After a transfer trigger is generated, first the value set in the IDB0 register, and then, at the falling edge of one-shot pulse for timers A1, A2, and A4, the values set in the IDB1 register become output signals for each phase (internal signal) and consequently the three-phase PWM output changes. Afterward, the values in registers IDB0 and IDB1 alternately become an output signal for each phase at every falling edge of the one-shot pulse for timers A1, A2 and A4.
When the INV15 bit in the INVC1 register is 0 (dead time enabled), a phase changing from active to nonactive changes simultaneously with output signals for each phase (internal signal), while a phase changing from nonactive to active changes when the dead time timer stops.

A transfer trigger is generated under the following conditions:

- The first timer B2 underflow after registers IDB0 and IDB1 are written
- Writing to the TB2 register (when the INV10 bit in the INVC1 register is 1)
- Setting the INV07 bit in the INVC0 register to 1 (software trigger)

19.3.3 Triangular Wave Modulation Three-Phase Mode 1

Triangular wave modulation uses twice the cycles of timer B2 as a reference cycle. Table 19.11 lists Three-Phase Mode 1 Specifications, and Figure 19.7 shows Usage Example of Three-Phase Mode 1.

Table 19.11 Three-Phase Mode 1 Specifications

Item		Specification
Carrier wave cycle		$\frac{(m+1)\times 2}{fi}$ m: Setting value of the TB2 register, 0 to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width		$\frac{n\times 2}{fi}$ n: Setting value of the TAi register, 1 to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Differences from three-phase mode 0	Reference cycle	Twice the cycle of timer B2 (cycle of the carrier wave)
	Timer B2 reload timing	Select either of the following: • Timer B2 underflow • Timer A output at an odd number of times
	Three-phase PWM waveform control	Counts the values of registers TAi and TAi1 alternately every time the Timer Ai start trigger is generated
	Timer B2 interrupt	Select a count timing for the ICTB2 register: • Timer B2 underflow • When the INV13 bit changes its value from 0 to 1 • When the INV13 bit changes its value from 1 to 0 When the setting value in the ICTB2 register is n, the timer B2 interrupt request is generated every nth time of the timing selected by bits INV00 and INV01 in the INVC1 register.
	Detection of a carrier wave cycle (first half or last half)	Detected (The INV13 bit in the INVC1 register is valid.)

i = 1, 2, 4

Table 19.12 Registers Used and Settings in Three-Phase Mode 1 (1/2)

Register	Bit	Functions, Setting Value
INVC0	INV00	Select the timing that the ICTB2 register starts counting.
	INV01	
	INV02	1 (three-phase motor control timer function used)
	INV03	1 (three-phase motor control timer output enabled)
	INV04	Select simultaneous conduction enabled or disabled.
	INV05	Simultaneous conduction detect flag
	INV06	Set to 0 (triangular wave modulation mode).
	INV07	Software trigger bit
INVC1	INV10	Select a start trigger for timers A1, A2, and A4.
	INV11	Set to 1 (three-phase mode 1).
	INV12	Select a count source for the dead time timer.
	INV13	Carrier wave state detect flag
	INV14	Select the active level (either active high or active high).
	INV15	Select the dead time enabled or disabled.
	INV16	Select a trigger for the dead time timer.
	7	Set to 0.
IDB0, IDB1	5 to 0	Set an output logic of the three-phase output shift register.
DTT	7 to 0	Set the dead time.
ICTB2	3 to 0	Set the frequency of timer B2 interrupts.
TB2SC	PWCON	Select timer B2 reload timing.
	IVPCR1	Select three-phase output forced cutoff enabled or disabled.
	b7 to b2	Set to 0.
PDRF	PDRU, PDRV, PDRW	Position-data-retain bit
	PDRT	Select a position-data-retain trigger.
PFCR	PFC5 to PFC0	Select I/O port or three-phase PWM output.
TPRC	TPRC0	Set to 1 when writing to the PFCR register, or to 0 when not writing to it.
TA1, TA2, TA4	15 to 0	Set the one-shot pulse width.
TA11, TA21, TA41	15 to 0	Set the one-shot pulse width.
TB2	15 to 0	Set one-half cycle of the carrier wave.

i = 1, 2, 4

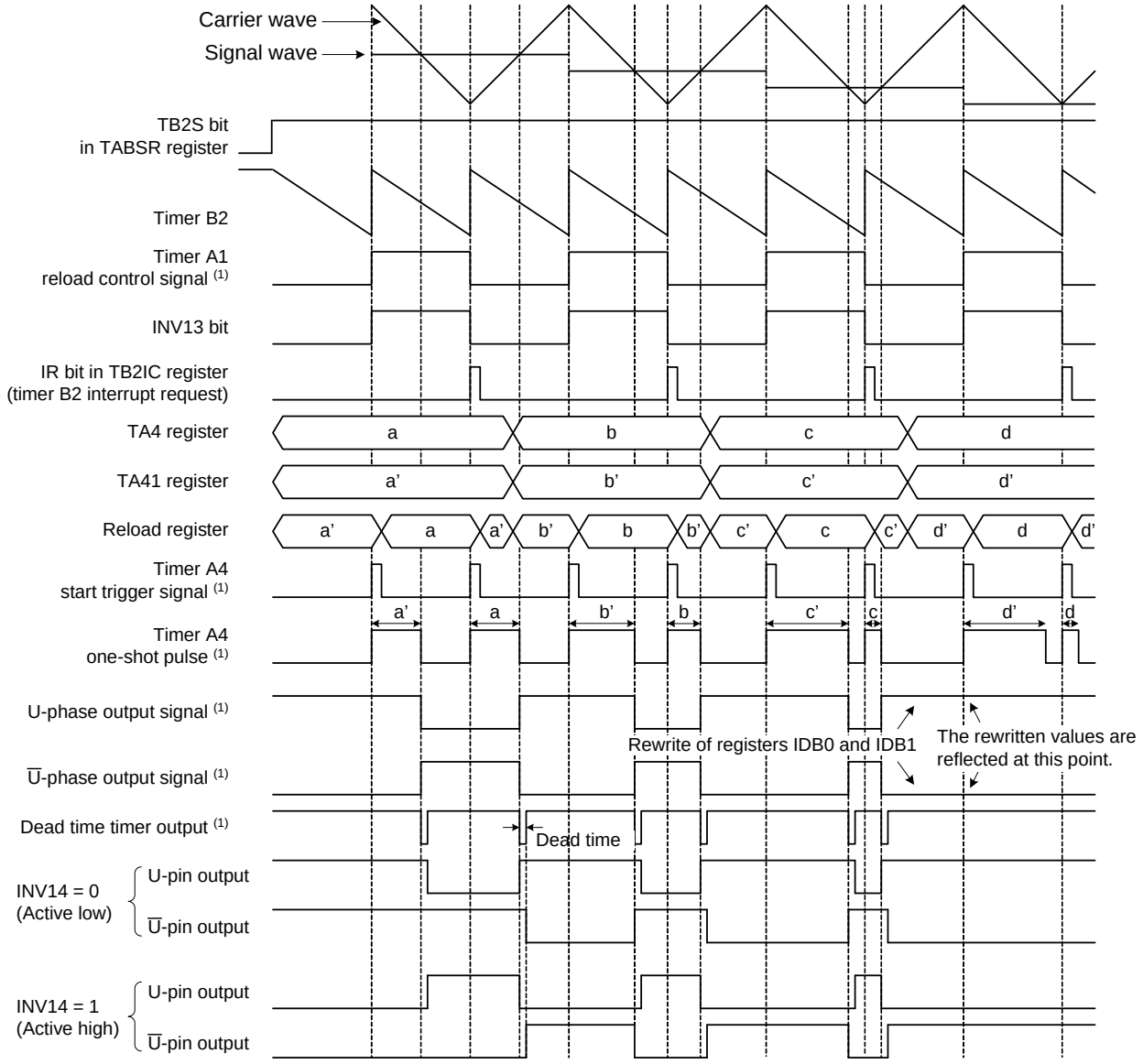
Note:

1. This table does not show the procedures.

Table 19.13 Registers Used and Settings in Three-Phase Mode 1 (2/2)

Register	Bit	Functions, Setting Value
TRGSR	TA1TGH to TA1TGL	01b (when using V-phase output control circuit)
	TA2TGH to TA2TGL	01b (when using W-phase output control circuit)
	TA3TGH to TA3TGL	(Not used for three-phase motor control timer.)
	TA4TGH to TA4TGL	01b (when using U-phase output control circuit)
TABSR	TA0S	Not used for three-phase motor control timer.
	TA1S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA2S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA3S	Not used for three-phase motor control timer.
	TA4S	Set to 1 when starting counting, and to 0 when stopping counting.
	TB0S	Not used for three-phase motor control timer.
	TB1S	Not used for three-phase motor control timer.
	TB2S	Set to 1 when starting counting, and to 0 when stopping counting.
TA1MR, TA2MR, TA4MR	TMOD1 to TMOD0	Set to 10b (one-shot timer mode).
	MR0	Set to 0.
	MR1	Set to 0.
	MR2	1 (Select a trigger by bits TAiTGH and TAiTGL.)
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
TB2MR	TMOD1 to TMOD0	Set to 00b (timer mode).
	MR1 to MR0	Set to 00b.
	4	Set to 0.
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
PCLKR	PCLK0	Select a count source.
TCKDIVC0	TCDIV00	Select a clock prior to timer AB division.
TACS0 to TACS2	7 to 0	Select a count source.
TBCS1	TCS3 to TCS0	Select a count source.
TAPOFS	POFSi	Set to 0.
UDF	TAiP	Set to 0.

i = 1, 2, 4
Note:
1. This table does not show the procedures.



The above applies under the following conditions:
The INVC0 register
- The INV02 bit is 1 (three-phase motor control timer function used).
- The INV03 bit is 1 (three-phase motor control timer output enabled).
- The INV06 bit is 0 (triangular wave modulation mode).
- The INV01 bit is 0 and the ICTB2 register is 2h (timer B2 interrupt at every second timer B2 underflow) or bits INV01 and INV00 are 11b and the ICTB2 register is 1h (timer B2 interrupt at timer B2 underflow while the timer A1 reload control signal is 1).

The INVC1 register
- The INV16 bit is 1 (The dead time timer is triggered on the rising edge of the three-phase output shift register).
- The INV15 bit is 0 (dead time timer enabled).
- The INV11 bit is 1 (three-phase mode 1).
- The INV10 bit is 0 (Timer B2 underflow is a start trigger for timers A1, A2 and A4).

The PWCOM bit in the TB2CS register is 0 (timer B2 reload at the timing of timer B2 underflow)
Bits PFC1 and PFC0 in the PFCR register are 11b (U-, $\overline{U}$-phase outputs).
Registers TA4 and TA41
- Initial value: TA41 = a', TA4 = a
- Registers TA4 and TA41 change at every timer B2 interrupt
  1st : TA41 = b', TA4 = b, 2nd : TA41 = c', TA4 = c, 3rd: TA41 = d', TA4 = d

Registers IDB0 and IDB1
- Initial values: DU0 = 1, DUB0 = 0, DU1 = 0, DUB1 = 1
- The values are changed to DU0 = 1, DUB0 = 0, DU1 = 1, DUB1 = 0 at the 3rd timer B2 interrupt.

Note:
1. Internal signal. Refer to Figure 19.1.

Figure 19.7 Usage Example of Three-Phase Mode 1

19.3.3.1 The INV13 Bit in the INVC1 Register

In three-phase mode 1, the INV13 bit can be used to detect whether the cycle of the carrier wave is the first half or the last half. The INV13 bit is a flag which checks the state of timer A1 reload control signals. Timer A1 reload control signal becomes 0 while timer A1 is stopped, and the value is reversed at every start trigger signal for timers A1, A2, and A4. Thus, if the cycle of carrier wave starts at the first timer B2 underflow, the first half comes when the INV13 bit is 1, and the last half comes when it is 0. Table 19.14 lists The Relations of the INV13 Bit with Other Factors.

Table 19.14 The Relations of the INV13 Bit with Other Factors

INV13 bit / Timer A1 reload control signal	1	0
One-shot pulse count value	Value at the TAi1 register	Value at the TAi register
Timer B2 underflow	At an odd number of times	At an even number of times
Carrier wave	First half	Last half

i = 1, 2, 4

19.3.3.2 Three-Phase PWM Waveform Output Timing Control

In three-phase mode 1, a start trigger for timers A1, A2, and A4 is generated, the value set in the TAi1 register is counted first. Afterward, the values in registers TAi1 and TAi alternately are counted every time a start trigger for timers A1, A2, and A4 is generated.

When the values in registers TAi1 and TAi are rewritten during the process, the updated value is output from the next carrier wave cycle. Figure 19.8 shows Three-Phase Mode 1 Update Timing of Registers TAi and TAi1.

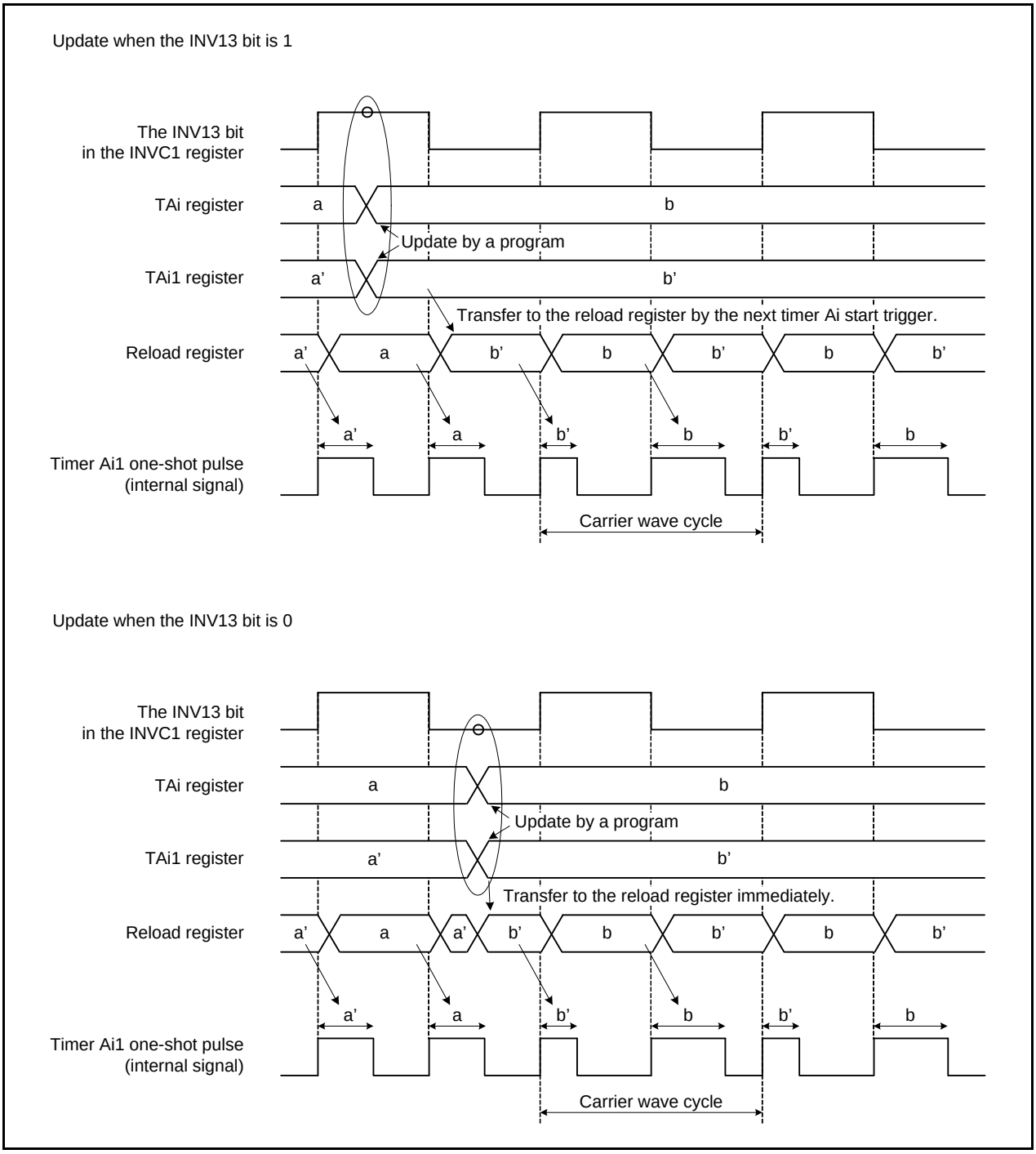


Figure 19.8 Three-Phase Mode 1 Update Timing of Registers TAi and TAi1

19.3.3.3 Carrier Wave Control

In three-phase mode 1, the reload timing of the TB2 register can be selected by the PWCON bit in the TB2SC register.

19.3.3.4 Three-Phase PWM Waveform Output Level Control

In triangular wave modulation mode, the output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift register by a transfer trigger. After a transfer trigger is generated, first the value set in the IDB0 register, and then, at the falling edge of one-shot pulse for timers A1, A2, and A4, the values set in the IDB1 register become output signals for each phase (internal signal) and consequently the three-phase PWM output changes. Afterward, the values in registers IDB0 and IDB1 alternately become an output signal for each phase at every falling edge of one-shot pulse for timers A1, A2, and A4.
When the INV15 bit in the INVC1 register is 0 (dead time enabled), a phase changing from active to nonactive changes simultaneously with output signals for each phase (internal signal), while a phase changing from nonactive to active changes when the dead time timer stops.

A transfer trigger is generated under the following conditions:

- The first timer B2 underflow after registers IDB0 and IDB1 are written
- Writing to the TB2 register (when the INV10 bit in the INVC1 register is 1)
- Setting the INV07 bit in the INVC0 register to 1 (software trigger)

19.3.4 Sawtooth Wave Modulation Mode

The sawtooth wave is modulated. Table 19.15 lists Sawtooth Wave Modulation Mode Specifications, and Figure 19.9 shows Usage Example of Sawtooth Wave Modulation Mode.

Table 19.15 Sawtooth Wave Modulation Mode Specifications

Item		Specification
Carrier wave cycle		$\frac{m+1}{fi}$ m: Setting value of the TB2 register, 0 to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Three-phase PWM output width		$\frac{n}{fi}$ n: Setting value of the TAi register, 1 to FFFFh fi: Count source frequency (f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-F, fOCO-S, fC32)
Differences from triangular wave modulation mode	Reference cycle	Timer B2 cycle (one-half cycle of the carrier wave)
	Timer B2 reload timing	Timer B2 underflow
	Three-phase PWM waveform control	Counts the value of the TAi register every time the timer Ai start trigger is generated (the TAi1 register is not used).
		The output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift register at every timer B2 underflow.
	Timer B2 interrupt	When the setting value in the ICTB2 register is n, the timer B2 interrupt request is generated every nth time of timer B2 underflow (no bits INV00 and INV01 in the INVC1 register).
	Dead time timer trigger	Both of the following: • Transfer trigger (generated at every timer B2 underflow) • Falling edge of timer Ai one-shot pulse
	Detection of a carrier wave cycle (first half or last half)	-

i = 1, 2, 4

Table 19.16 Registers Used and Settings in Sawtooth Wave Modulation Mode (1/2)

Register	Bit	Functions, Setting Value
INVC0	INV00	Invalid (despite the settings, the ICTB2 register counts timer B2 underflow)
	INV01	
	INV02	1 (three-phase motor control timer function used)
	INV03	1 (three-phase motor control timer output enabled)
	INV04	Select simultaneous conduction enabled or disabled.
	INV05	Simultaneous conduction detect flag
	INV06	Set to 1 (sawtooth wave modulation mode).
	INV07	Software trigger bit
INVC1	INV10	Select a start trigger for timers A1, A2, and A4.
	INV11	Set to 0.
	INV12	Select a count source for the dead time timer.
	INV13	Invalid
	INV14	Select the active level (either active high or active high).
	INV15	Select the dead time enabled or disabled.
	INV16	Select a trigger for the dead time timer.
	7	Set to 0.
IDB0, IDB1	5 to 0	Set an output logic of the three-phase output shift register.
DTT	7 to 0	Set the dead time.
ICTB2	3 to 0	Set the frequency of timer B2 interrupts.
TB2SC	PWCON	Set to 0 (timer B2 underflow).
	IVPCR1	Select three-phase output forced cutoff enabled or disabled.
	b7 to b2	Set to 0.
PDRF	PDRU, PDRV, PDRW	Position-data-retain bit
	PDRT	Select a position-data-retain trigger.
PFCR	PFC5 to PFC0	Select I/O port or three-phase PWM output.
TPRC	TPRC0	Set to 1 when writing to the PFCR register, or to 0 when not writing to it.
TA1, TA2, TA4	15 to 0	Set the one-shot pulse width.
TA11, TA21, TA41	15 to 0	Not used
TB2	15 to 0	Set the cycle of the carrier wave.

i = 1, 2, 4

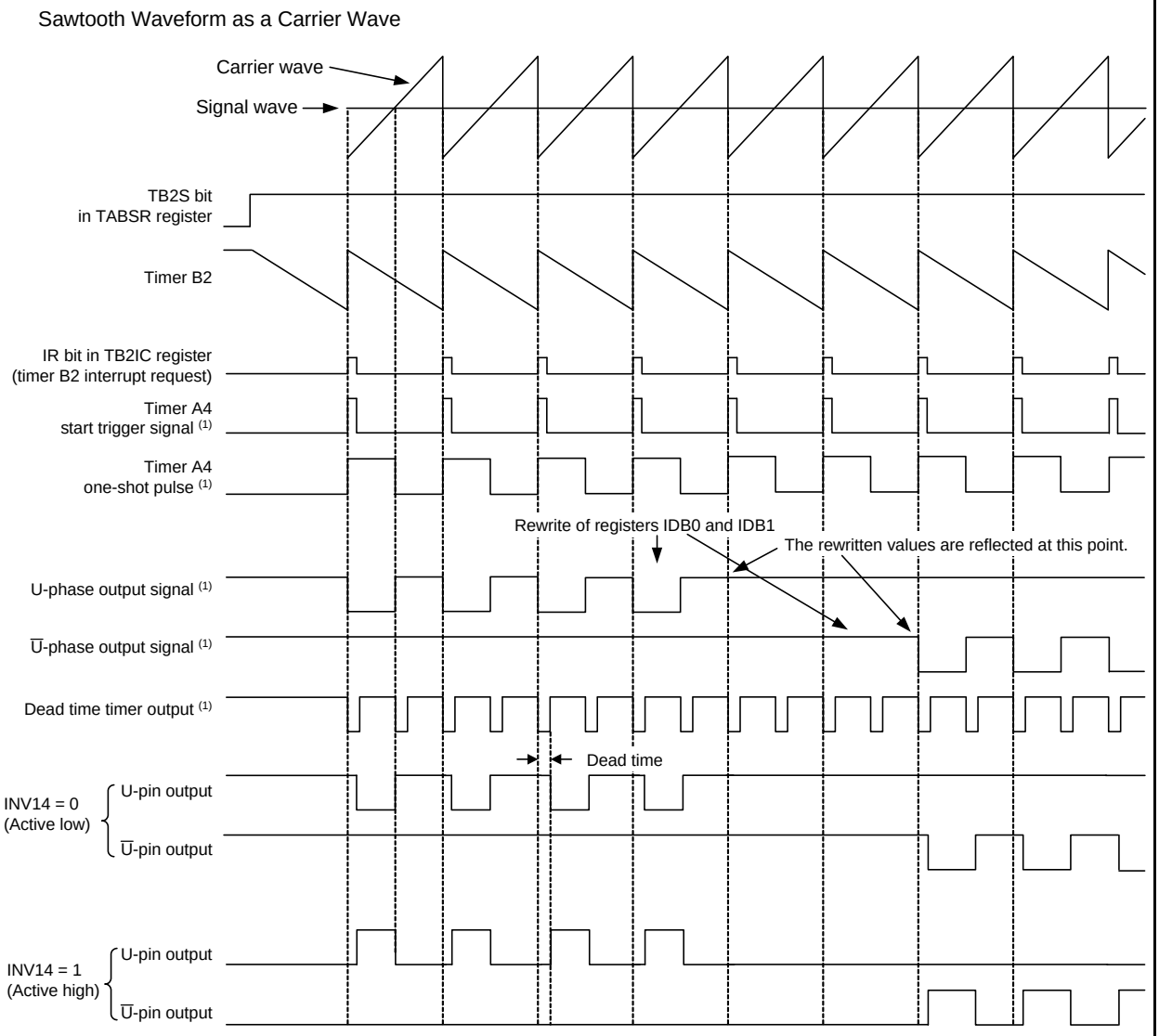
Note:

1. This table does not show the procedures.

Table 19.17 Registers Used and Settings in Sawtooth Wave Modulation Mode (2/2)

Register	Bit	Functions, Setting Value
TRGSR	TA1TGH to TA1TGL	01b (when using V-phase output control circuit)
	TA2TGH to TA2TGL	01b (when using W-phase output control circuit)
	TA3TGH to TA3TGL	(Not used for three-phase motor control timer.)
	TA4TGH to TA4TGL	01b (when using U-phase output control circuit)
TABSR	TA0S	Not used for three-phase motor control timer.
	TA1S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA2S	Set to 1 when starting counting, and to 0 when stopping counting.
	TA3S	Not used for three-phase motor control timer.
	TA4S	Set to 1 when starting counting, and to 0 when stopping counting.
	TB0S	Not used for three-phase motor control timer.
	TB1S	Not used for three-phase motor control timer.
	TB2S	Set to 1 when starting counting, and to 0 when stopping counting.
TA1MR, TA2MR, TA4MR	TMOD1 to TMOD0	Set to 10b (one-shot timer mode).
	MR0	Set to 0.
	MR1	Set to 0.
	MR2	1 (select a trigger by bits TAiTGH and TAiTGL)
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
TB2MR	TMOD1 to TMOD0	Set to 00b (timer mode).
	MR1 to MR0	Set to 00b.
	4	Set to 0.
	MR3	Set to 0.
	TCK1 to TCK0	Select a count source.
PCLKR	PCLK0	Select a count source.
TCKDIVC0	TCDIV00	Select a clock prior to timer AB division.
TACS0 to TACS2	7 to 0	Select a count source.
TBCS1	TCS3 to TCS0	Select a count source.
TAPOFS	POFSi	Set to 0.
UDF	TAiP	Set to 0.

i = 1, 2, 4
Note:
1. This table does not show the procedures.



The above applies under the following conditions.
The INVC0 register
- The INV02 bit is 1 (three-phase motor control timer function used).
- The INV03 bit is 1 (three-phase motor control timer output enabled).
- The INV06 bit is 1 (sawtooth wave modulation mode).
- The INV10 bit is 0 (Timer B2 underflow is a start trigger for timers A1, A2 and A4.).

The INVC1 register
- The INV11 bit is 0 and the ICTB2 register is 1h (Timer B interrupt request is generated at every timer B2 underflow.).
- The INV15 bit is 0 (dead time timer enabled).
- The INV16 bit is 0 (The dead time timer is triggered on the falling edge of timers A4, A1 and A2 one-shot pulse.).

The PWCOM bit in the TB2CS register is 0 (timer B2 reload at the timing of timer B2 underflow)
Bits PFC1 and PFC0 in the PFCR register are 11b (U-, U̅-phase outputs).
Registers IDB0 and IDB1
- Initial values : DU0 = 0, DUB0 = 1, DU1 = 1, DUB1 = 1
- The values are changed to DU0 = 1, DUB0 = 1, DU1 = 1, DUB1 = 1 at the 3rd timer B2 interrupt.
- The values are changed to DU0 = 1, DUB0 = 0, DU1 = 1, DUB1 = 1 at the 5th timer B2 interrupt.

Note:
1. Internal signal. Refer to Figure 19.1.

Figure 19.9 Usage Example of Sawtooth Wave Modulation Mode

19.3.4.1 Three-Phase PWM Waveform Output Timing Control

In sawtooth wave modulation mode, when a start trigger for timers A1, A2, and A4 is generated, the counter starts counting the value of the TAi register (i = 1, 2, 4).

19.3.4.2 Three-Phase PWM Waveform Output Level Control

In sawtooth wave modulation mode, the output levels set in registers IDB0 and IDB1 are transferred to the three-phase output shift register by a transfer trigger. After a transfer trigger is generated, first the value set in the IDB0 register, and then at the falling edge of one-shot pulse for timers A1, A2, and A4, the value set in the IDB1 register become output signals for each phase (internal signal) and consequently the three-phase PWM output changes. Afterward, the following two actions are repeated:
(1) The setting levels are transferred to the three-phase output shift register by a transfer trigger generated at timer B2 underflow, and therefore, the value in the IDB0 register becomes output signals for each phase. (2) The values set in the IDB1 register become output signals for each phase at the falling edge of one-shot pulse for timers A1, A2, and A4.
When the INV15 bit in the INVC1 register is 0 (dead time enabled), a phase changing from active to nonactive changes simultaneously with output signals for each phase (internal signal), while a phase changing from nonactive to active changes when the dead time timer stops.

A transfer trigger is generated under the following conditions:

- Timer B2 underflow (each time)
- Writing to the TB2 register (when the INV10 bit in the INVC1 register is 1)
- Setting the INV07 bit in the INVC0 register to 1 (software trigger)

19.4 Interrupts

The timer B2 interrupt and timer A1, A2 and A4 interrupts are available for the three-phase motor control timer.

19.4.1 Timer B2 Interrupt

When the setting value in the ICTB2 register is n, a timer B2 interrupt request is generated at the timings below. For details, refer to the specifications and usage examples of each mode.

In triangular wave modulation three-phase mode 0 and sawtooth wave modulation mode, the interrupt request is generated at the nth count of timer B2 underflow (when setting value in the ICTB2 register is n).

In triangular wave modulation three-phase mode 1, the interrupt request is generated at the nth count of the following timings selected by bits INV01 and INV00 in the INVC0 register:

- Timer B2 underflow
- When the INV13 bit changes its value from 0 to 1
- When the INV13 bit changes its value from 1 to 0

Refer to 14.7 “Interrupt Control” for details of interrupt control. Table 19.18 lists Timer B2 Interrupt Related Register.

Table 19.18 Timer B2 Interrupt Related Register

Address	Register Name	Register Symbol	After Reset
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b

19.4.2 Timers A1, A2 and A4 Interrupts

A timer Ai interrupt request is generated at the falling edge of timer Ai (i = 1, 2, 4) one-shot pulse (internal signal). Refer to 14.7 “Interrupt Control” for details of interrupt control. Table 19.19 lists Timers A1, A2, and A4 Interrupts Related Registers.

Table 19.19 Timers A1, A2, and A4 Interrupts Related Registers

Address	Register Name	Register Symbol	After Reset
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b

In the timer Ai interrupt, when the TMOD1 bit in the TAiMR register is changed from 0 to 1 (from timer mode or event counter mode to one-shot timer mode, PWM mode or programmable output mode), the IR bit in the TAiIC register is sometimes automatically set to 1 (interrupt requested). Thus, when changing the TMOD1 bit, follow the steps below. Also refer to 14.13 “Notes on Interrupts”.

(1) Set bits ILVL2 to ILVL0 in the TAiIC register to 000b (interrupt disabled).
(2) Set the TAiMR register.
(3) Set the IR bit in the TAiIC register to 0 (interrupt not requested).

19.5 Notes on Three-Phase Motor Control Timer Function

19.5.1 Timer A, Timer B

Refer to 17.5 “Notes on Timer A” and 18.5 “Notes on Timer B”.

19.5.2 Forced Cutoff Input

The following pins are affected by the three-phase forced cutoff due to the $\overline{SD}$ pin input:
P7_2/CLK2/TA1OUT/V, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$, P7_4/TA2OUT/W, P7_5/TA2IN/$\overline{W}$, P8_0/TA4OUT/RXD5/SCL5/U, P8_1/TA4IN/$\overline{CTS5}$/$\overline{RTS5}$/$\overline{U}$

20. Real-Time Clock

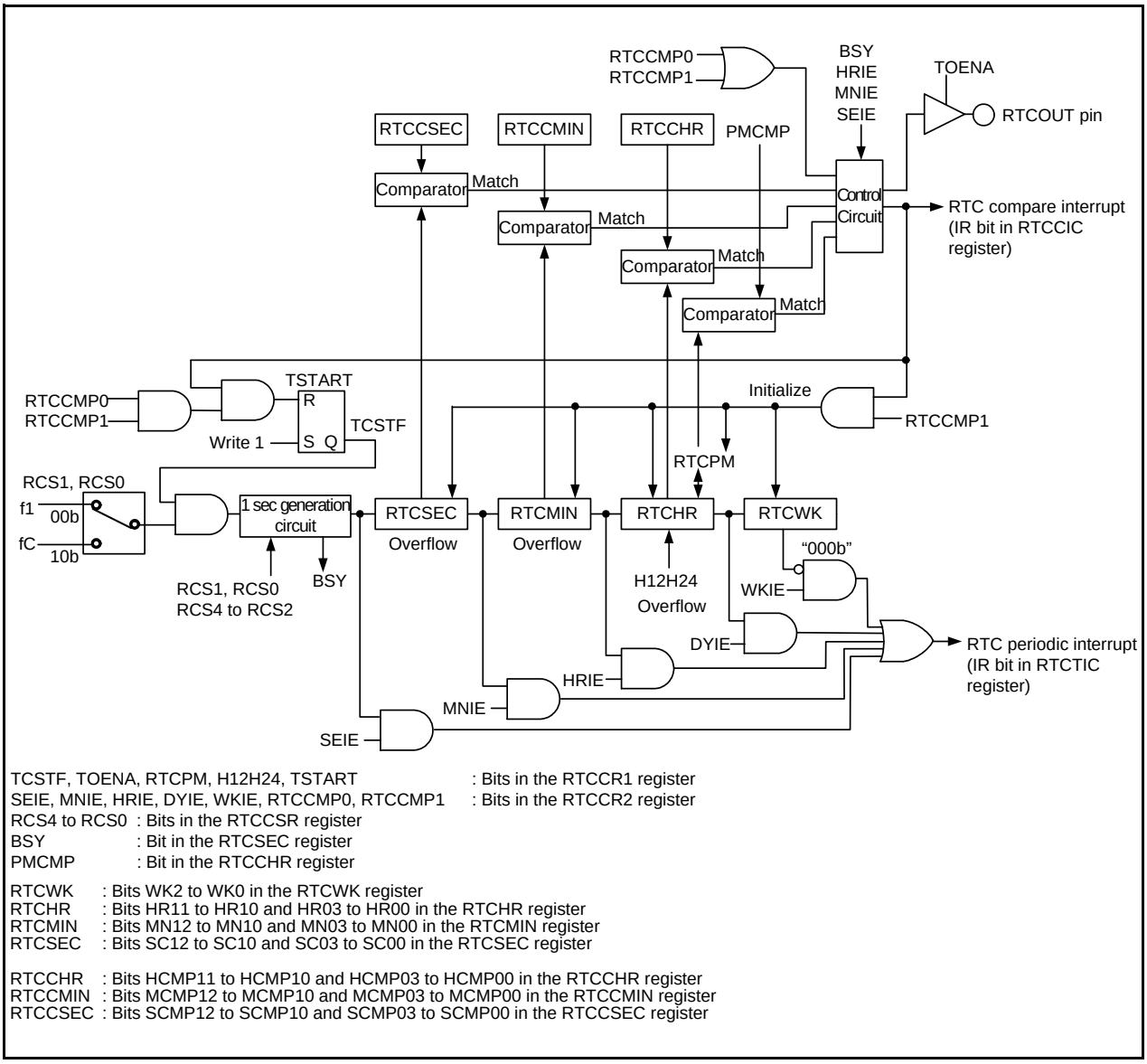
20.1 Introduction

The real-time clock generates a 1-second signal from a count source and counts seconds, minutes, hours, a.m./p.m., a day, and a week. It also detects matches with specified seconds, minutes, and hours. Table 20.1 lists Real-Time Clock Specifications, Figure 20.1 shows a Real-Time Clock Block Diagram, and Table 20.2 lists the I/O Port.

Table 20.1 Real-Time Clock Specifications

Item	Specification
Count source	f1, fC
Count operation	• Increment • Compare mode 1 or not using compare mode The count value is continuously used, and the count continues • Compare mode 2 When a compare match is detected, the count value is set to 0 and the count continues. • Compare mode 3 When a compare match is detected, the count value is set to 0 and the count stops.
Count start condition	1 (count starts) is written to the TSTART bit in RTCCR1 register
Count stop condition	0 (count stops) is written to the TSTART bit in RTCCR1 register
Interrupt request generation timing	Select one of the following: • Update second data • Update minute data • Update hour data • Update day data • When day data is set to 000b • When the count data and the compare data match
RTCOUT pin function	Programmable I/O ports or compare output
Read from timer	When the RTCSEC, RTCMIN, RTCHR, or RTCWK register is read, the count value can be read. The values read from registers RTCSEC, RTCMIN, and RTCHR are represented by the BCD code.
Write to timer	When bits TSTART and TCSTF in the RTCCR1 register are 0 (timer stopped), the RTCSEC, RTCMIN, RTCHR, and RTCWK registers can be written to. The values written to registers RTCSEC, RTCMIN, and RTCHR are represented by the BCD codes.
Select function	• 12-hour mode / 24-hour mode switch function • Compare output

Note:
1. In this manual, day refers to one day of the week. Refer to 20.2.4 “Real-Time Clock Day Data Register (RTCWK)” for details.



TCSTF, TOENA, RTCPM, H12H24, TSTART : Bits in the RTCCR1 register
SEIE, MNIE, HRIE, DYIE, WKIE, RTCCMP0, RTCCMP1 : Bits in the RTCCR2 register
RCS4 to RCS0 : Bits in the RTCCSR register
BSY : Bit in the RTCSEC register
PMCMP : Bit in the RTCCHR register

RTCWK : Bits WK2 to WK0 in the RTCWK register
RTCHR : Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
RTCMIN : Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
RTCSEC : Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register

RTCCHR : Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register
RTCCMIN : Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register
RTCCSEC : Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register

Figure 20.1 Real-Time Clock Block Diagram

Table 20.2 I/O Port

Pin Name	I/O Type	Function
RTCOUT	Output	Compare output

20.2 Registers

Table 20.3 Register Structure

Address	Register Name	Register Symbol	After Reset
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b

20.2.1 Real-Time Clock Second Data Register (RTCSEC)

Real-Time Clock Second Data Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
RTCSEC	0340h	00h

Bit Symbol	Bit Name	Function	Setting Range	RW
SC00	1st digit of second count bit	Count 0 to 9 every second. When the digit moves up, 1 is added to the 2nd digit of second	0 to 9	RW
SC01				RW
SC02				RW
SC03				RW
SC10	2nd digit of second count bit	When counting 0 to 5, 60 seconds are counted	0 to 5	RW
SC11				RW
SC12				RW
BSY	Real-time clock busy flag	This bit is 1 while registers RTCSEC, RTCMIN, RTCHR or RTCWK are updated		RO

SC03-SC00 (1st Digit of Second Count Bit) (b3-b0)
SC12-SC10 (2nd Digit of Second Count Bit) (b6-b4)

Set a value between 00 and 59 by the BCD codes.
These bits become 00 at compare match in compare 2 mode and compare 3 mode.
Write to bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register when both bits TSTART and TCSTF in the RTCCR1 register are 0 (timer stops). Read when the BSY bit is 0 (not while data is updated).

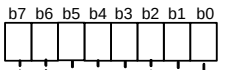
BSY (Real-Time Clock Busy Flag) (b7)

This bit is 1 while data is updated. Read the following bits when the BSY bit is 0 (not while data is updated).

- Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
- Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
- Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
- Bits WK2 to WK0 in the RTCWK register

20.2.2 Real-Time Clock Minute Data Register (RTCMIN)

Real-Time Clock Minute Data Register



Symbol	Address	After Reset
RTCMIN	0341h	X000 0000b

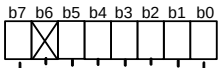
Bit Symbol	Bit Name	Function	Setting Range	RW
MN00	1st digit of minute count bit	Count 0 to 9 every minute. When the digit moves up, 1 is added to the 2nd digit of minute	0 to 9	RW
MN01				RW
MN02				RW
MN03				RW
MN10	2nd digit of minute count bit	When counting 0 to 5, 60 minutes are counted	0 to 5	RW
MN11				RW
MN12				RW
$\overline{\text{(b7)}}$	Reserved bit	Read as undefined value		RO

MN03-MN00 (1st Digit of Minute Count Bit) (b3-b0)
MN12-MN10 (2nd Digit of Minute Count Bit) (b6-b4)

Set a value between 00 and 59 by the BCD codes.
These bits become 00 at compare match in compare 2 mode and compare 3 mode.
Write to bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register when both bits TSTART and TCSTF in the RTCCR1 register are 0 (timer stops). Read when the BSY bit in the RTCSEC is 0 (not while data is updated).

20.2.3 Real-Time Clock Hour Data Register (RTCHR)

Real-Time Clock Hour Data Register



Symbol	Address	After Reset
RTCHR	0342h	XX00 0000b

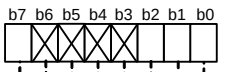
Bit Symbol	Bit Name	Function	Setting Range	RW
HR00	1st digit of hour count bit	Count 0 to 9 every hour. When the digit moves up, 1 is added to the 2nd digit of hour.	0 to 9	RW
HR01				RW
HR02				RW
HR03				RW
HR10	2nd digit of hour count bit	Count 0 to 1 when the H12H24 bit is set to 0 (12-hour mode). Count 0 to 2 when the H12H24 bit is set to 1 (24-hour mode).	0 to 2	RW
HR11				RW
— (b6)	No register bit. If necessary, set to 0. Read as undefined value			—
— (b7)	Reserved bit	Read as undefined value		RO

HR03-HR00 (1st Digit of Hour Count Bit) (b3-b0)
HR11-HR10 (2nd Digit of Hour Count Bit) (b5-b4)

When the H12H24 bit in the RTCCR1 register is 0 (12-hour mode), set a value between 00 and 11 by BCD code. When the H12H24 bit in the RTCCR1 register is 1 (24-hour mode), set a value between 00 and 23 by the BCD codes.
These bits become 00 at compare match in compare 2 mode and compare 3 mode.
Write to bits HR11 to HR10 and HR03 to HR00 in the RTCHR register when both bits TSTART and TCSTF in the RTCCR1 register are 0 (timer stops). Read when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.2.4 Real-Time Clock Day Data Register (RTCWK)

Real-Time Clock Day Data Register



Symbol	Address	After Reset
RTCWK	0343h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
WK0	Day count bit	b2 b1 b0 0 0 0 : Day 1 0 0 1 : Day 2 0 1 0 : Day 3 0 1 1 : Day 4 1 0 0 : Day 5 1 0 1 : Day 6 1 1 0 : Day 7 1 1 1 : Do not set	RW
WK1			RW
WK2			RW
— (b6-b3)	No register bits. If necessary, set to 0. Read as undefined value		—
— (b7)	Reserved bit	Read as undefined value	RO

WK2-WK0 (Day Count Bit) (b2-b0)

A week is counted by counting from 000b (Day 1) to 110b (Day 7) repeatedly. Do not set to 111b. These bits become 000b at compare match in compare 2 mode and compare 3 mode.
Write to bits WK2 to WK0 in the RTCWK register when both bits TSTART and TCSTF in the RTCCR1 register are 0 (timer stops). Read when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.2.5 Real-Time Clock Control Register 1 (RTCCR1)

Real-Time Clock Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
							0

Symbol	Address	After Reset
RTCCR1	0344h	0000 X00Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	Set to 0	RW
TCSTF	Real-time clock count status flag	0 : Count stopped 1 : Counting	RO
TOENA	RTCOUT pin output bit	0 : Compare output disabled 1 : Compare output enabled	RW
— (b3)	Reserved bit	Set to 0	RW
RTCRST	Real-time clock reset bit	Setting this bit to 0 after setting it to 1 resets the real-time clock	RW
RTCPM	A.m./p.m. bit	0 : a.m. 1 : p.m.	RW
H12H24	Operating mode select bit	0 : 12-hour mode 1 : 24-hour mode	RW
TSTART	Real-time clock count start bit	0 : Count stops 1 : Count starts	RW

TCSTF (Real-Time Clock Count Status Flag) (b1)
TSTART (Real-Time Clock Count Start Bit) (b7)

The real-time clock has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop.

The real-time clock starts counting and the TCSTF bit becomes 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to two cycles of the count source until the TCSTF bit becomes 1 after setting the TSTART bit to 1. During this time, do not access registers associated with the real-time clock (1) other than the TCSTF bit.

Also, when setting the TSTART bit to 0 (count stops), the real-time clock stops counting and the TCSTF bit becomes 0 (count stops). It takes the time for up to three cycles of the count source until the TCSTF bit becomes 0 after setting the TSTART bit to 0. During this time, do not access registers associated with the real-time clock (1) other than the TCSTF bit.

Note:
1. Registers associated with the real-time clock: RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR1, RTCCR2, and RTCCSR.

RTCRST (Real-Time Clock Reset Bit) (b4)

When setting this bit to 0 after setting it to 1, the following are set automatically.

- The values are reset in registers RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.
- Bits TCSTF, RTCPM, H12H24, and TSTART in the RTCCR1 register become 0.

RTCPM (A.M./P.M. Bit) (b5)

Write to the RTCPM bit when both bits TSTART and TCSTF in the RTCCR1 register are 0 (timer stops). Read this bit when the BSY bit in the RTCSEC register is 0 (not while data is updated).
The RTCPM bit is enabled when the H12H24 bit is 0 (12-hour mode) or 1 (24-hour mode). Set the RTCPM bit as below to set time while the H12H24 bit is 1.

- Set the RTCPM bit to 0 when bits HR11 to HR10 and HR03 to HR00 in the RTCHR register are 00 to 11.
- Set the RTCPM bit to 1 when bits HR11 to HR10 and HR03 to HR00 in the RTCHR register are 12 to 23.

The RTCPM bit changes as follows while counting.

- Becomes 0 when the RTCPM bit is 1 (p.m.) while the clock increments from 11:59:59 (23:59:59 for 24-hour mode) to 00:00:00.
- Becomes 1 when the RTCPM bit is 0 (a.m.) while the clock increments from 11:59:59 to 00:00:00 (12:00:00 for 24-hour mode).

Figure 20.2 shows Definition of Time Representation.

Noon

Contents of RTCHR Register	H12H24 bit = 1 (24-hour mode)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	H12H24 bit = 0 (12-hour mode)	0	1	2	3	4	5	6	7	8	9	10	11	0	1	2	3	4	5
Contents of RTCPM bit		0 (a.m.)												1 (p.m.)					
Contents in RTCWK register		000 (Day 1)																	

Date changes

Contents of RTCHR Register	H12H24 bit = 1 (24-hour mode)	18	19	20	21	22	23	0	1	2	3	...
	H12H24 bit = 0 (12-hour mode)	6	7	8	9	10	11	0	1	2	3	...
Contents of RTCPM bit		1 (p.m.)						0 (a.m.)				...
Contents in RTCWK register		000 (Day 1)						001 (Day 2)				...

Bits RTCPM and H12H24 : Bits in the RTCCR1 register
The above applies to the case when count starts from 0 a.m.of day 1.

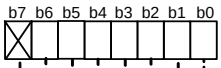
Figure 20.2 Definition of Time Representation

H12H24 (Operating Mode Select Bit) (b6)

Write to the H12H24 bit when both bits TSTART and TCSTF in the RTCCR1 register are 0 (timer stops).

20.2.6 Real-Time Clock Control Register 2 (RTCCR2)

Real-Time Clock Control Register 2



Symbol	Address	After Reset
RTCCR2	0345h	X000 0000b

Bit Symbol	Bit Name	Function	RW
SEIE	Periodic interrupt triggered every second enable bit	0 : Disable periodic interrupt triggered every second 1 : Enable periodic interrupt triggered every second	RW
MNIE	Periodic interrupt triggered every minute enable bit	0 : Disable periodic interrupt triggered every minute 1 : Enable periodic interrupt triggered every minute	RW
HRIE	Periodic interrupt triggered every hour enable bit	0 : Disable periodic interrupt triggered every hour 1 : Enable periodic interrupt triggered every hour	RW
DYIE	Periodic interrupt triggered every day enable bit	0 : Disable periodic interrupt triggered every day 1 : Enable periodic interrupt triggered every day	RW
WKIE	Periodic interrupt triggered every week enable bit	0 : Disable periodic interrupt triggered every week 1 : Enable periodic interrupt triggered every week	RW
RTCCMP0	Compare mode select bit	b6 b5 0 0 : No compare mode 0 1 : Compare 1 mode 1 0 : Compare 2 mode 1 1 : Compare 3 mode	RW
RTCCMP1			RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value		—

Write to the RTCCR2 register when both bits TSTART and TCSTF in the RTCCR1 register are 0 (timer stops).

While bits RTCCMP1 to RTCCMP0 are 00b (no compare mode), an interrupt request can be generated every second, minute, hour, day, or week. To generate an interrupt request, set one of the following bits to 1 (interrupt enabled): SEIE, MNIE, HRIE, DAYIE, and WKIE (Be sure to set only one bit to 1). Table 20.4 lists Periodic Interrupt Sources.

Table 20.4 Periodic Interrupt Sources

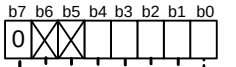
Factor	Interrupt Source	Interrupt Enable Bit
Periodic interrupt triggered every week	Value in RTCWK register is set to 000b (1-week period)	WKIE
Periodic interrupt triggered every day	RTCWK register is updated (1-day period)	DYIE
Periodic interrupt triggered every hour	RTCHR register is updated (1-hour period)	HRIE
Periodic interrupt triggered every minute	RTCMIN register is updated (1-minute period)	MNIE
Periodic interrupt triggered every second	RTCSEC register is updated (1-second period)	SEIE

When bits RTCCMP1 to RTCCMP0 are 01b, 10b, or 11b (any compare mode), set as follows depending on what to compare.

- When comparing to the RTCCSEC register, set the SEIE bit to 1 (interrupt enabled).
- When comparing to the RTCCMIN register, set both bits SEIE and MNIE to 1.
- When comparing to the RTCCHR register, set all the bits SEIE, MNIE, and HRIE to 1.

20.2.7 Real-Time Clock Count Source Select Register (RTCCSR)

Real-Time Clock Count Source Select Register



Symbol: RTCCSR | Address: 0346h | After Reset: XXX0 0000b

Bit Symbol	Bit Name	Function	RW
RCS0	Count source select bit	b1 b0 0 0 : f1 0 1 : Do not set 1 0 : fC 1 1 : Do not set	RW
RCS1			RW
RCS2	Count source frequency select bit	b4 b3 b2 0 0 0 : f1 = fC or 4 MHz 0 0 1 : f1 = 6 MHz 0 1 0 : f1 = 8 MHz 0 1 1 : f1 = 16 MHz 1 0 0 : f1 = 20 MHz 1 0 1 : f1 = 24 MHz 1 1 0 : f1 = 32 MHz 1 1 1 : Do not set	RW
RCS3			RW
RCS4			RW
— (b6-b5)	No register bits. If necessary, set to 0. Read as undefined value		—
— (b7)	Reserved bit	Set to 0	RW

When bits RCS1 to RCS0 are 10b (fC), set bits RCS4 to RCS2 to 000b.
When bits RCS1 to RCS0 are 00b (f1), select a frequency matched to f1 by bits RCS4 to RCS2.
Write to the RTCCSR register when both bits TSTART and TCSTF in the RTCCR1 register are 0 (timer stops).

20.2.8 Real-Time Clock Second Compare Data Register (RTCCSEC)

Real-Time Clock Second Compare Data Register

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	After Reset
	RTCCSEC	0348h	X000 0000b

Bit Symbol	Bit Name	Function	Setting Range	RW
SCMP00	1st digit of second compare data bit	Store compare data	0 to 9	RW
SCMP01				RW
SCMP02				RW
SCMP03				RW
SCMP10	2nd digit of second compare data bit	Store compare data	0 to 5	RW
SCMP11				RW
SCMP12				RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value			—

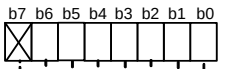
The RTCCSEC register is enabled when bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b, 10b, or 11b (any compare mode).

SCMP03-SCMP00 (1st Digit of Second Compare Data Bit) (b3-b0)
SCMP12-SCMP10 (2nd Digit of Second Compare Data Bit) (b6-b4)

Set a value between 00 and 59 by the BCD codes.
Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.2.9 Real-Time Clock Minute Compare Data Register (RTCCMIN)

Real-Time Clock Minute Compare Data Register



Symbol	Address	After Reset
RTCCMIN	0349h	X000 0000b

Bit Symbol	Bit Name	Function	Setting Range	RW
MCMP00	1st digit of minute compare data bit	Store compare data	0 to 9	RW
MCMP01				RW
MCMP02				RW
MCMP03				RW
MCMP10	2nd digit of minute compare data bit	Store compare data	0 to 5	RW
MCMP11				RW
MCMP12				RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value			—

The RTCCMIN register is enabled when bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b, 10b, or 11b (any compare mode).

MCMP03-MCMP00 (1st Digit of Minute Compare Data Bit) (b3-b0)
MCMP12-MCMP10 (2nd Digit of Minute Compare Data Bit) (b6-b4)

Set a value between 00 and 59 by the BCD codes.
Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.2.10 Real-Time Clock Hour Compare Data Register (RTCCHR)

Real-Time Clock Hour Compare Data Register

Symbol	Address	After Reset
RTCCHR	034Ah	X000 0000b

Bit Symbol	Bit Name	Function	Setting Range	RW
HCMP00	1st digit of hour compare data bit	Store compare data	0 to 9	RW
HCMP01				RW
HCMP02				RW
HCMP03				RW
HCMP10	2nd digit of hour compare data bit	Store compare data	0 to 2	RW
HCMP11				RW
PMCMP	A.m./p.m. compare bit	0 : a.m. 1 : p.m.		RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value			—

The RTCCHR register is enabled when bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b, 10b, or 11b (any compare mode).

HCMP03-HCMP00 (1st Digit of Hour Compare Data Bit) (b3-b0)
HCMP11-HCMP10 (2nd Digit of Hour Compare Data Bit) (b5-b4)

When the H12H24 bit in the RTCCR1 register is 0 (12-hour mode), set a value between 00 and 11 by the BCD codes. When the H12H24 bit in the RTCCR1 register is 1 (24-hour mode), set a value between 00 and 23 by the BCD codes.
Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

PMCMP (A.M./P.M Compare Bit) (b6)

This bit is enabled both when the H12H24 bit in the RTCCR1 register is 0 (12-hour mode) or 1 (24-hour mode). When the H12H24 bit is 1, set as follows.

- When bits HCMP11 to HCMP10 and HCMP03 to HCMP00 are 00 to 11, set the PMCMP bit to 0.
- When bits HCMP11 to HCMP10 and HCMP03 to HCMP00 are 12 to 23, set the PMCMP bit to 1.

Write to these bits when the BSY bit in the RTCSEC register is 0 (not while data is updated).

20.3 Operations

20.3.1 Basic Operation

Real-time clock generates one-second signal from the count source selected in the RTCCSR register and counts seconds, minutes, hours, a.m./p.m., a day, and a week.

Time and day to start counting are settable by registers RTCSEC, RTCMIN, RTCHR, RTCWK, and the RTCPM bit in the RTCCR1 register. Current time and day are read from registers RTCSEC, RTCMIN, RTCHR, RTCWK, and the RTCPM bit in the RTCCR1 register. However, do not read these registers when the BSY bit in the RTCSEC register is 1 (while data is updated).

An interrupt request can be generated every second, minute, hour, day, or week. While bits RTCCMP1 to RTCCMP0 are 00b (no compare mode), use the RTCCR2 register to enable one of the periodic interrupts triggered every second, minute, hour, day and week. When a periodic interrupt is generated, the IR bit in the RTCTIC register becomes 1 (interrupt request).

Figure 20.3 shows Real-Time Clock Basic Operating Example, Figure 20.4 shows Time and Day Change Procedure (No Compare Mode or Compare 1 Mode), and Figure 20.5 shows Time and Day Change Procedure (Compare 2 Mode or Compare 3 Mode).

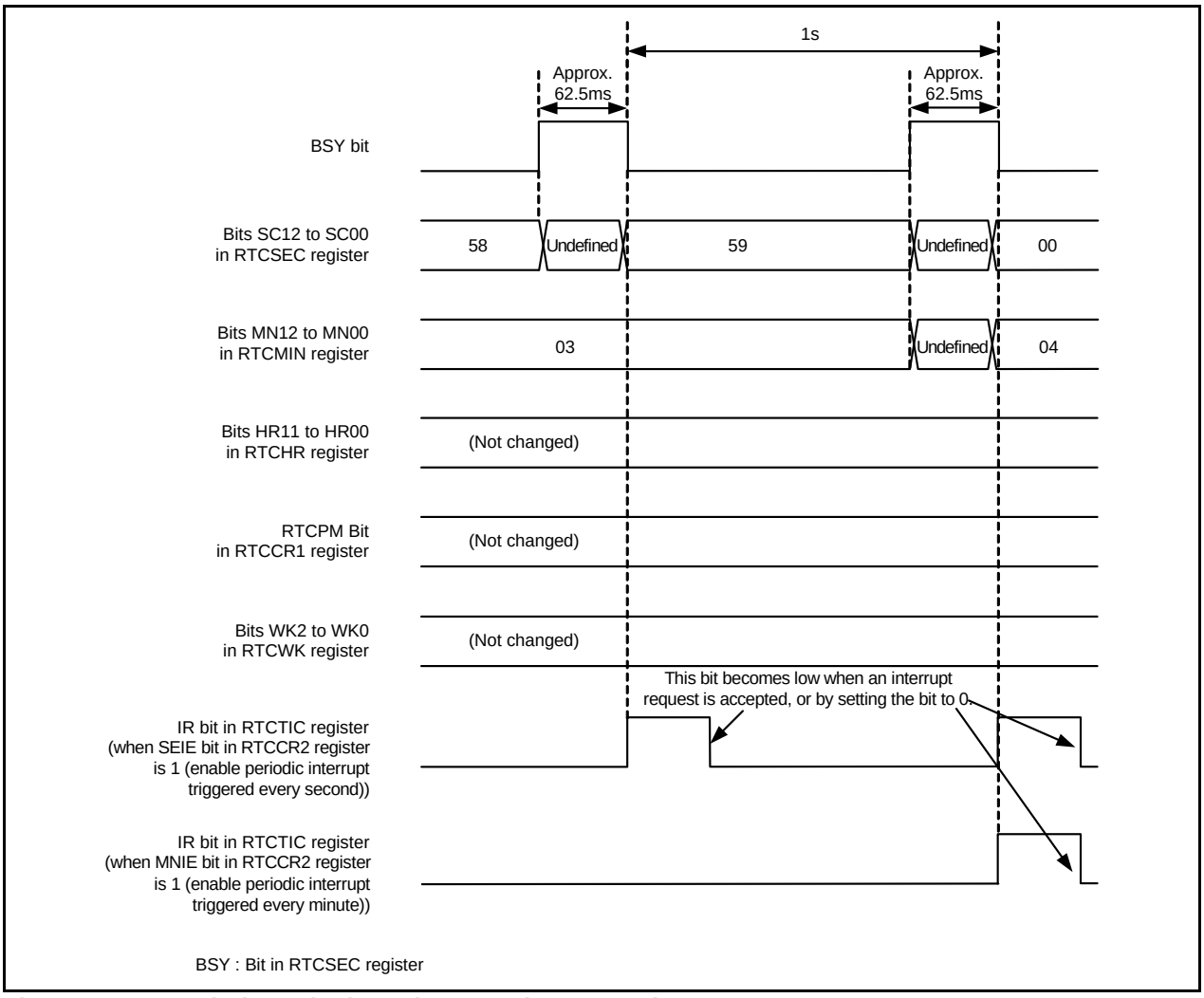


Figure 20.3 Real-Time Clock Basic Operating Example

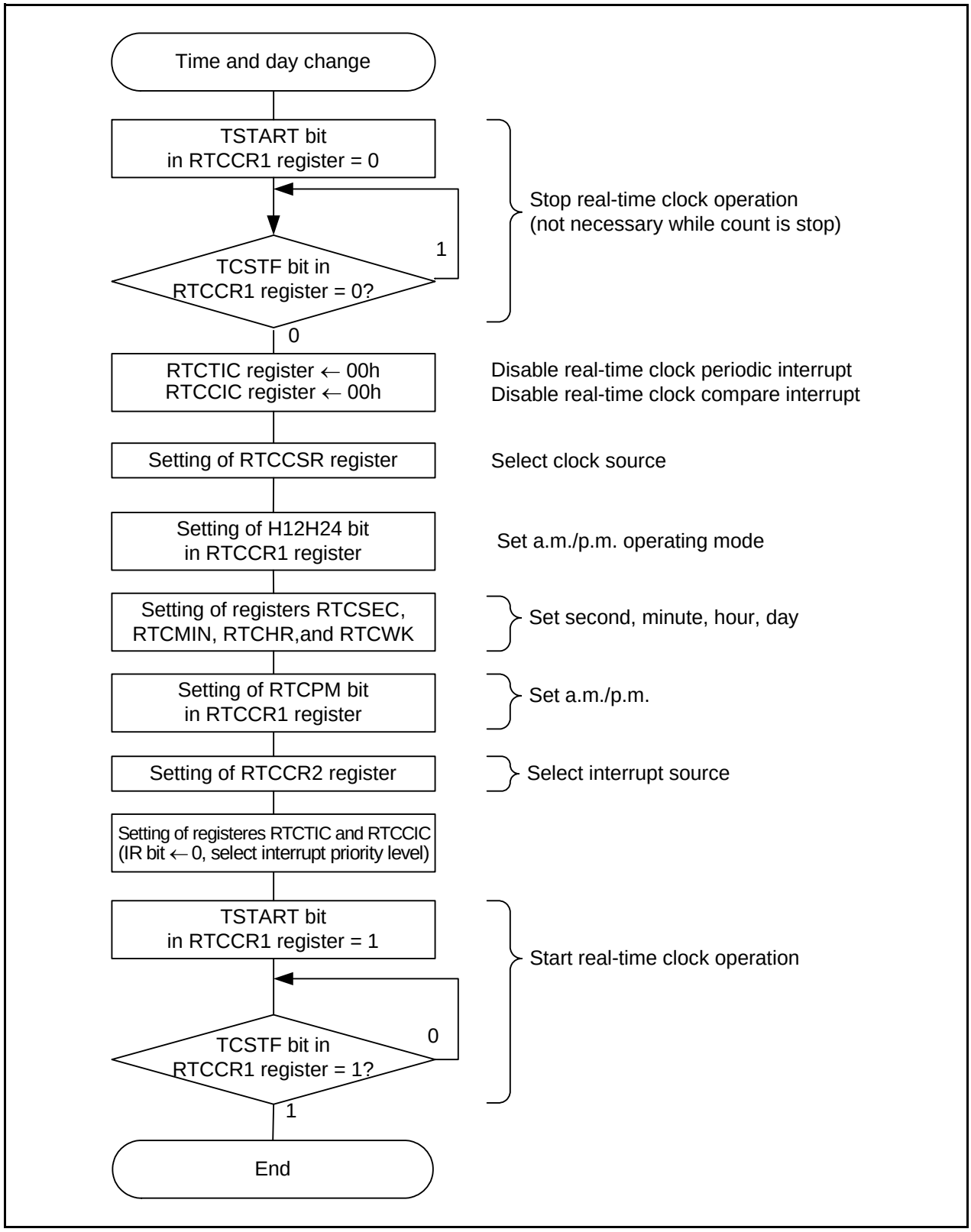
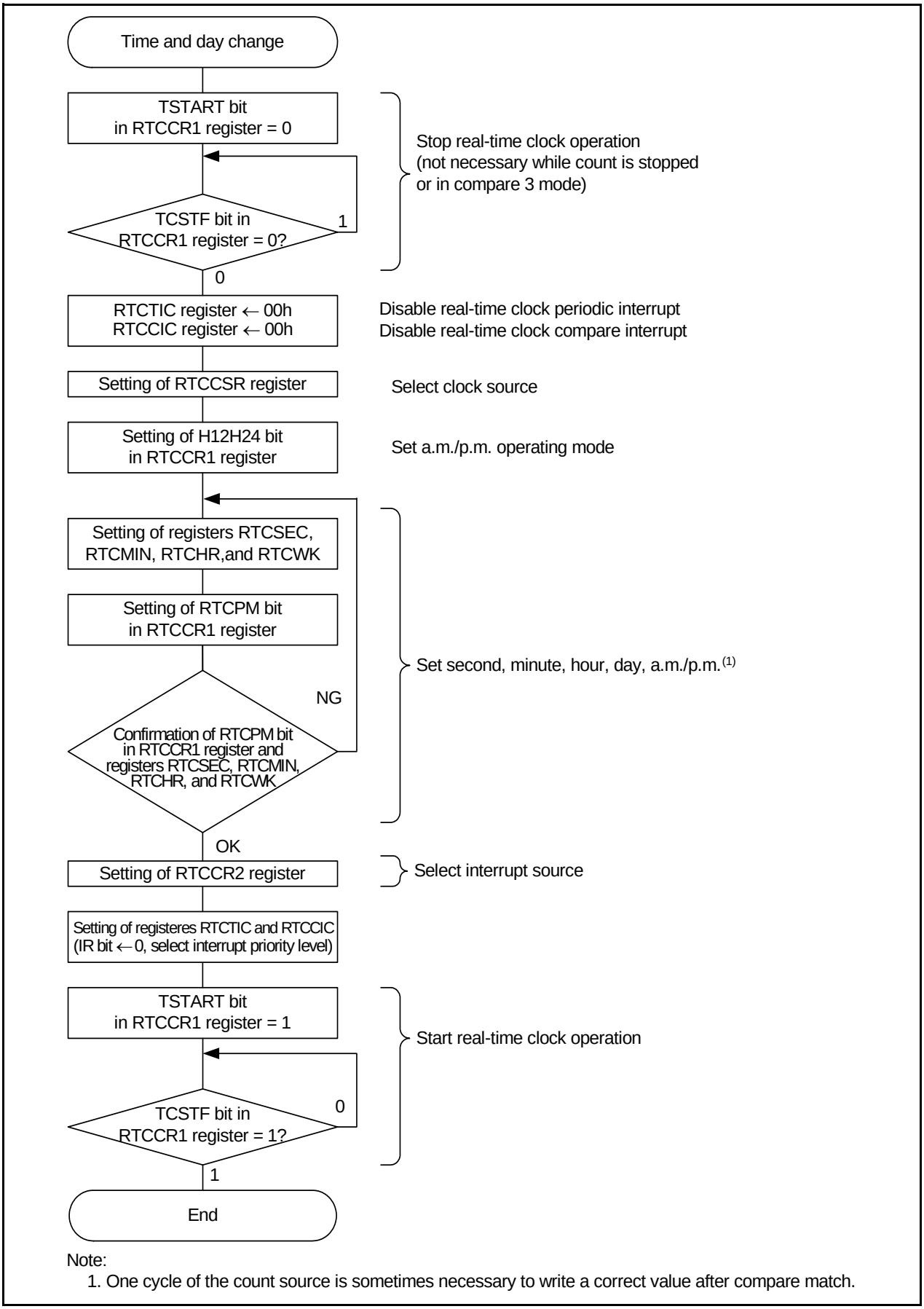


Figure 20.4 Time and Day Change Procedure (No Compare Mode or Compare 1 Mode)



Note:
1. One cycle of the count source is sometimes necessary to write a correct value after compare match.

Figure 20.5 Time and Day Change Procedure (Compare 2 Mode or Compare 3 Mode)

20.3.2 Compare Mode

In compare mode, time data (1) and compare data (1) are compared, and compare value match is detected. When match is detected, the following occur.

- Compare interrupt request
  Refer to 20.4 “Interrupts” for details.
- RTCOUT pin output level inversion
  While the TOENA bit in the RTCCR1 register is 1 (compare output enabled), when compare value match is detected, RTCOUT pin output level is converted.

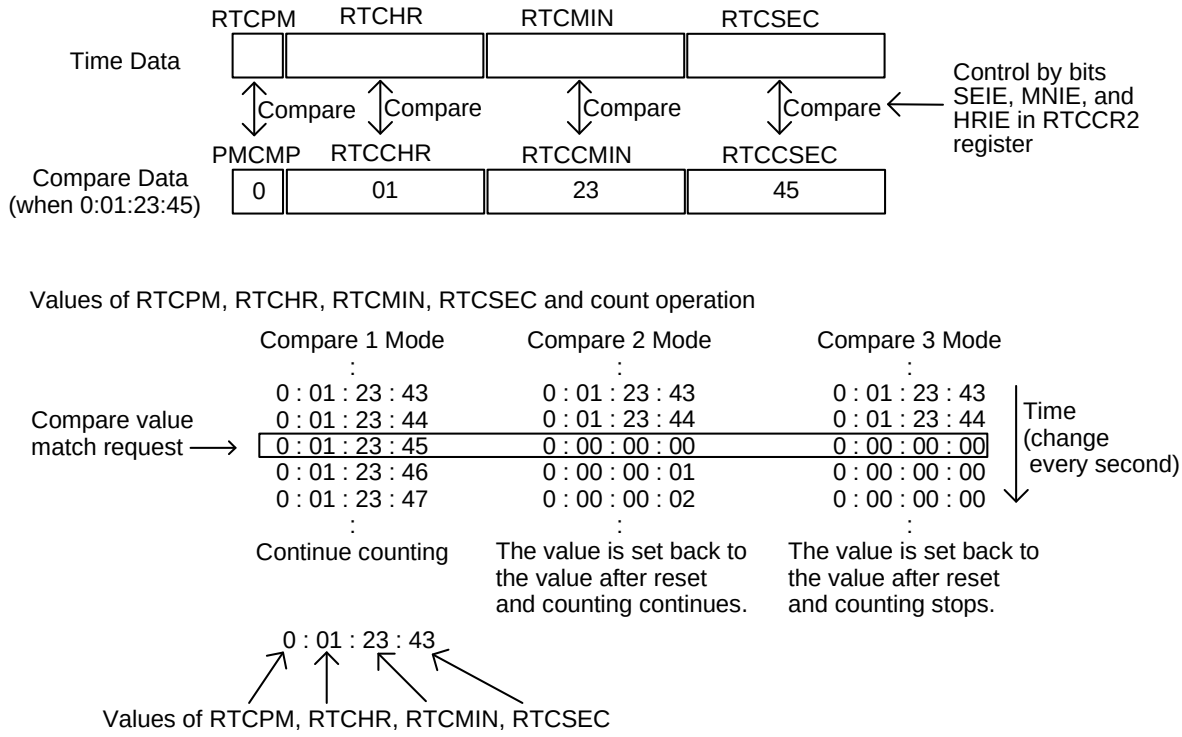
Notes:

1. Bits for time data are as follows:
   Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
   Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
   Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
   The RTCPM bit in the RTCCR1 register
   Bits for compare data are as follows:
   Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register
   Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register
   Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register
   The PMCMP bit in the RTCCHR register

In compare mode, set the SEIE, MNIE, or HRIE bit in the RTCCR2 register to 1 (interrupt enabled) according to compare data (second, minute, or hour). Refer to 20.2.6 “Real-Time Clock Control Register 2 (RTCCR2)” for details.
Compare mode has three modes: compare 1 mode, compare 2 mode, and compare 3 mode. Operation after compare value match differs depending on a compare mode.

- Compare 1 mode
  The time data is used continuously and counting continues.
- Compare 2 mode
  The value after reset is used as the time data and counting continues.
- Compare 3 mode
  The value after reset is used as the time data and counting stops.

Figure 20.6 shows Difference between Compare Modes, Figure 20.7 shows Count Start/Stop Operating Example, Figure 20.8 shows Compare 1 Mode Operating Example, Figure 20.9 shows Compare 2 Mode Operating Example, and Figure 20.10 shows Compare 3 Mode Operating Example.

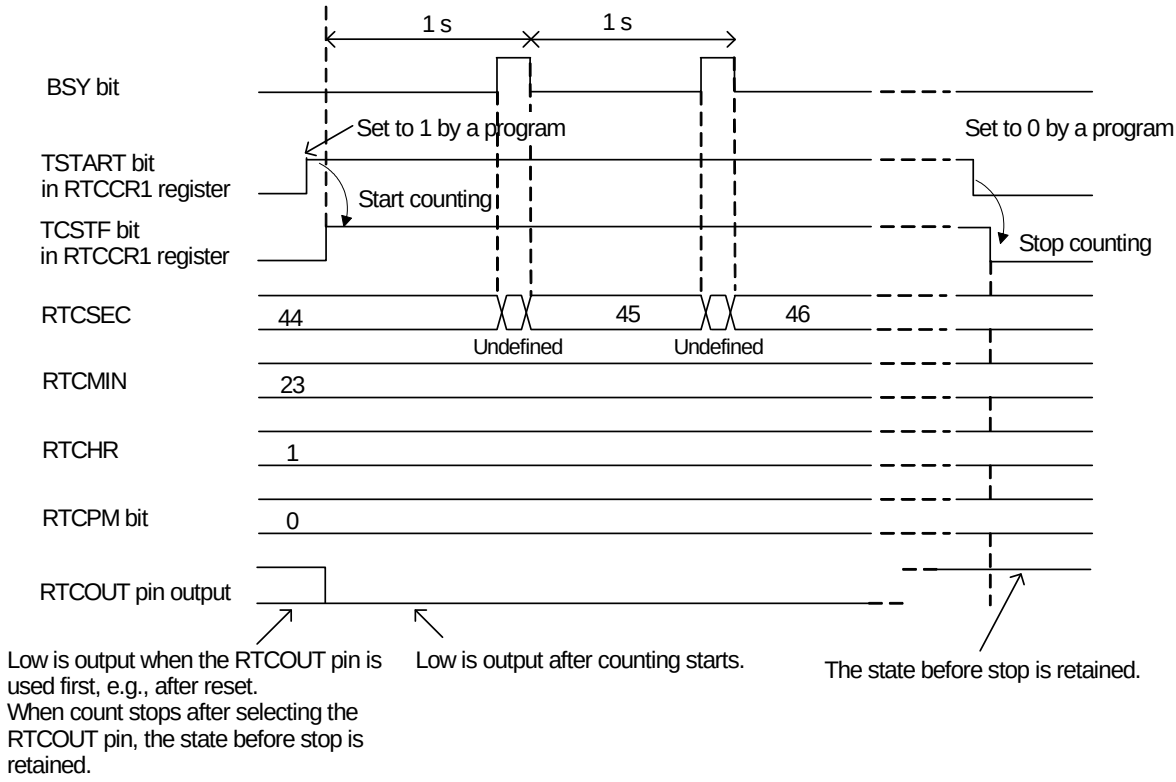


The above diagram shows an instance in which the following conditions are met:

- The H12H24 bit in the RTCCR1 register is 0 (12-hour mode).
- Bits SEIE, MNIE, and HRIE in the RTCCR2 register are 1.

RTCPM : RTCPM bit in RTCCR1 register
RTCHR : Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCMIN : Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCSEC : Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
PMCMP : PMCMP bit in RTCCHR register
RTCCHR : Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in RTCCHR register
RTCCMIN : Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in RTCCMIN register
RTCCSEC : Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in RTCCSEC register

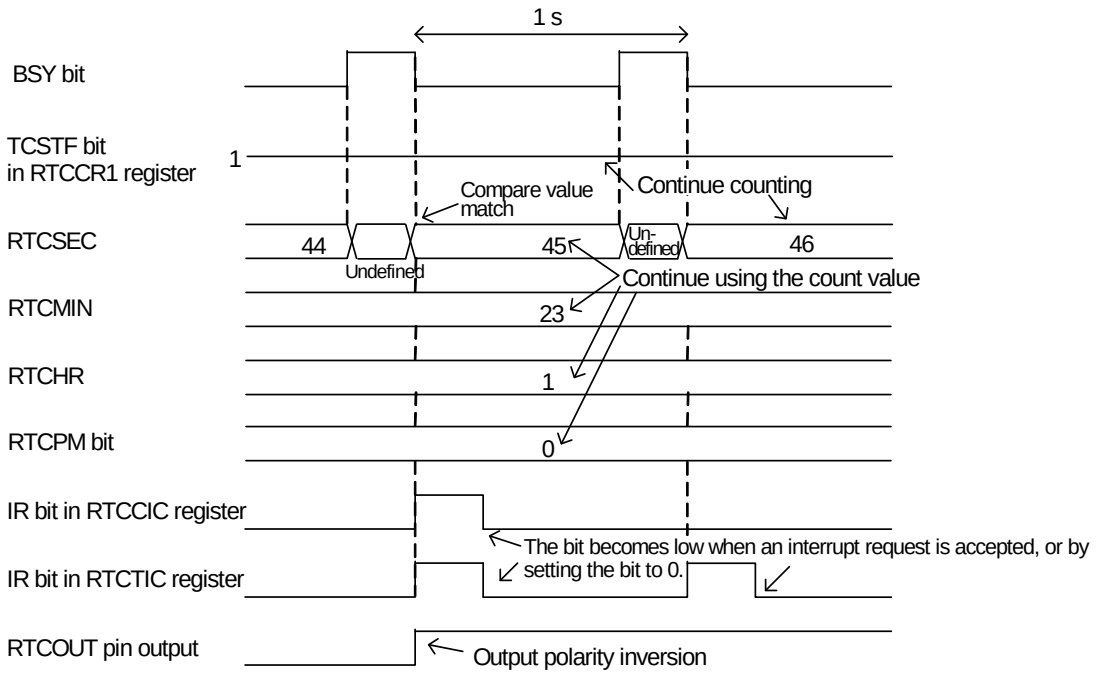
Figure 20.6 Difference between Compare Modes



The diagram above applies under the following conditions:
- The TOENA bit in the RTCCR1 register is 1 (compare output enabled).
- Bits RTCCMP1 to RTCCMP0 in the RTCCR2 register is 01b (compare 1 mode)

BSY bit : Bit in RTCSEC register
RTCSEC : Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
RTCMIN : Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCHR : Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCPM bit : Bit in RTCCR1 register

Figure 20.7 Count Start/Stop Operating Example

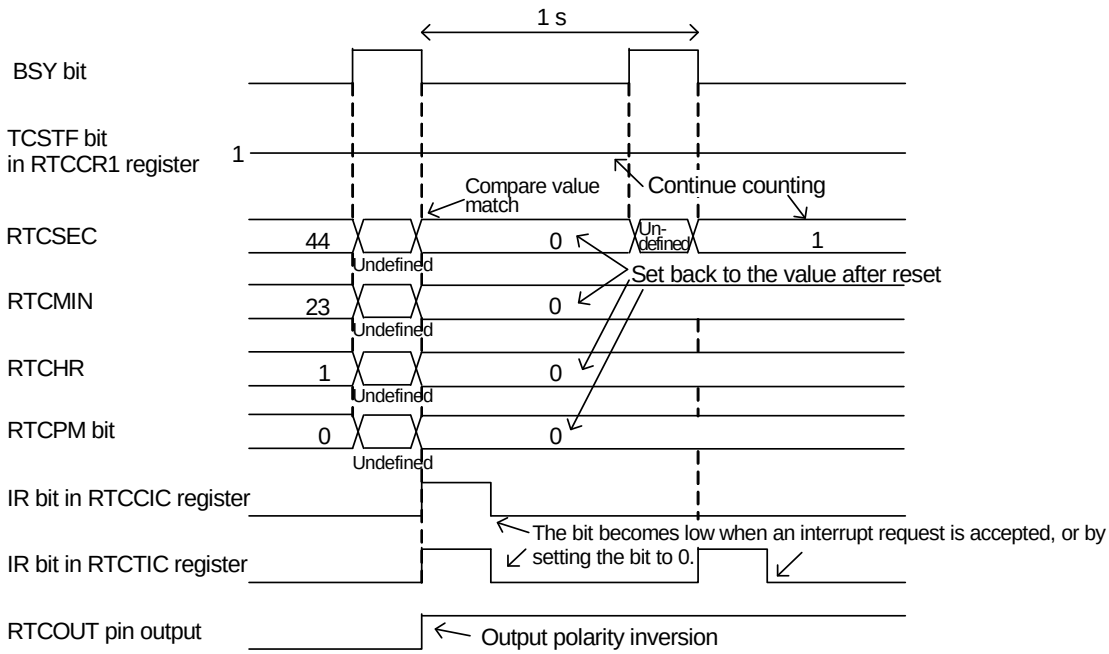


The diagram above applies under the following conditions:

- The TOENA bit in the RTCCR1 register is 1 (compare output enabled).
- Bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 01b (compare 1 mode).
- Bits SEIE, MNIE, and HRIE in the RTCCR2 are 1 (compare by seconds, minutes, and hours. Interrupt enabled).
- Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register are 4 and 5 respectively (second setting: 45).
  Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register are 2 and 3 respectively (minute setting: 23).
  Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register are 0 and 1 respectively (hour setting: 1).
  The PMCMP bit in the RTCCHR register is 0 (a.m.).

BSY bit : Bit in RTCSEC register
RTCSEC : Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
RTCMIN : Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCHR : Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCPM bit : Bit in RTCCR1 register

Figure 20.8 Compare 1 Mode Operating Example

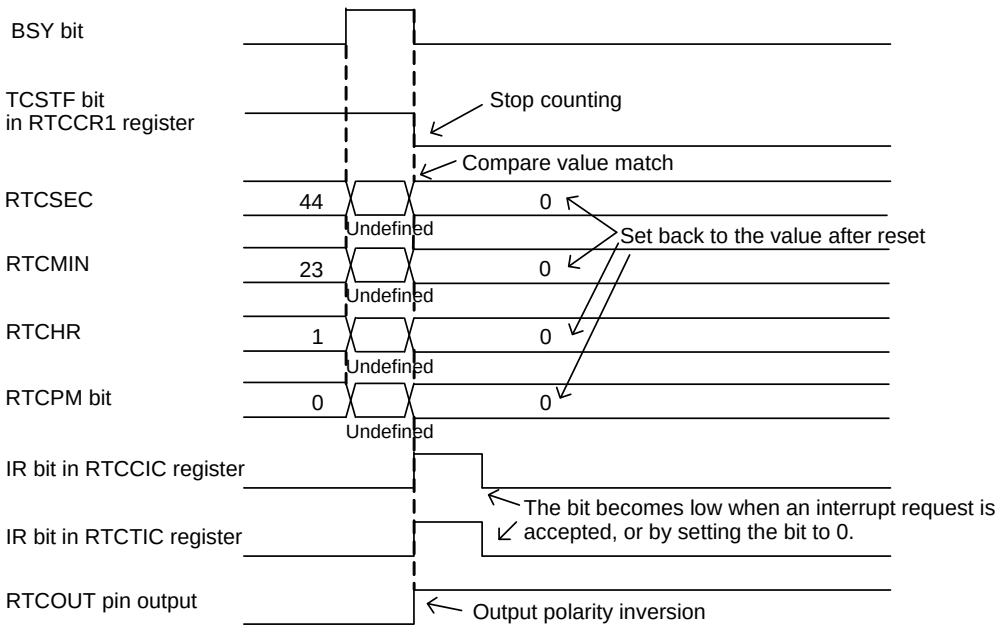


The diagram above applies under the following conditions:

- The TOENA bit in the RTCCR1 register is 1 (compare output enabled).
- Bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 10b (compare 2 mode).
- Bits SEIE, MNIE, and HRIE in the RTCCR2 register are 1 (compare by seconds, minutes, and hours. Interrupt enabled).
- Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register are 4 and 5 respectively (second setting: 45).
  Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register are 2 and 3 respectively (minute setting: 23).
  Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register are 0 and 1 respectively (hour setting: 1).
  The PMCMP bit in the RTCCHR register is 0 (a.m.).

BSY bit : Bit in RTCSEC register
RTCSEC : Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
RTCMIN : Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCHR : Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCPM bit : Bit in RTCCR1 register

Figure 20.9 Compare 2 Mode Operating Example



The diagram above applies under the following conditions:

- The TOENA bit in the RTCCR1 register is 1 (compare output enabled).
- Bits RTCCMP1 to RTCCMP0 in the RTCCR2 register are 11b (compare 3 mode).
- Bits SEIE, MNIE, and HRIE in the RTCCR2 register are 1 (compare by seconds, minutes, and hours. Interrupt enabled).
- Bits SCMP12 to SCMP10 and SCMP03 to SCMP00 in the RTCCSEC register are 4 and 5 respectively (second setting: 45).
  Bits MCMP12 to MCMP10 and MCMP03 to MCMP00 in the RTCCMIN register are 2 and 3 respectively (minute setting: 23).
  Bits HCMP11 to HCMP10 and HCMP03 to HCMP00 in the RTCCHR register are 0 and 1 respectively (hour setting: 1).
  The PMCMP bit in the RTCCHR register is 0 (a.m.).

BSY bit : Bit in RTCSEC register
RTCSEC : Bits SC12 to SC10 and SC03 to SC00 in RTCSEC register
RTCMIN : Bits MN12 to MN10 and MN03 to MN00 in RTCMIN register
RTCHR : Bits HR11 to HR10 and HR03 to HR00 in RTCHR register
RTCPM bit : Bit in RTCCR1 register

Figure 20.10 Compare 3 Mode Operating Example

20.4 Interrupts

Real-time clock generates the following two types of interrupts.

- Periodic interrupts triggered every second, minute, hour, day, and week
- Compare value match interrupt

Refer to Table 20.4 Periodic Interrupt Sources for details of periodic interrupt sources, each mode's specification and operating example for the interrupt request generating timing, and 14.7 "Interrupt Control" for details of interrupt control. Table 20.5 lists Real-Time Clock Interrupt-Associated Registers.

Table 20.5 Real-Time Clock Interrupt-Associated Registers

Address	Register Name	Register Symbol	After Reset
006Eh	Real-Time Clock Period Interrupt Control Register	RTCTIC	XXXX X000b
006Fh	Real-Time Clock Compare Match Interrupt Control Register	RTCCIC	XXXX X000b
0205h	Interrupt Source Select Register 3	IFSR3A	00h

Real-time clock shares the interrupt vectors and interrupt control registers with other peripheral functions. To use period interrupts, set the IFSR35 bit in the IFSR3A register to 1 (real-time clock cycle), and to use compare interrupts, set the IFSR36 bit in the IFSR3A register to 1 (real-time clock compare).

20.5 Notes on Real-Time Clock

20.5.1 Starting and Stopping Count

Real-time clock has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the RTCCR1 register.

Real-time clock starts counting and the TCSTF bit becomes 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to two cycles of the count source until the TCSTF bit becomes 1 after setting the TSTART bit to 1. During this time, do not access registers associated with real-time clock (1) other than the TCSTF bit.

Also, real-time clock stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit becomes 0 (count stops). It takes up to three cycles of the count source until the TCSTF bit becomes 0 after setting the TSTART bit to 0. During this time, do not access registers associated with real-time clock other than the TCSTF bit.

Note:

1. Registers associated with real-time clock: RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR1, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.

20.5.2 Register Setting (Time Data etc.)

Write to the following registers or bits while real-time clock is stopped.

- Registers RTCSEC, RTCMIN, RTCHR, RTCWK, and RTCCR2
- Bits H12H24 and RTCPM in the RTCCR1 register
- Bits RCS0 to RCS4 in the RTCCSR register

Real-time clock is stopped when bits TSTART and TCSTF in the RTCCR1 register are 0 (real-time clock stopped).

Also, set all above-mentioned registers and bits (immediately before real-time clock count starts) before setting the RTCCR2 register.

Figure 20.4 shows Time and Day Change Procedure (No Compare Mode or Compare 1 Mode), and Figure 20.5 shows Time and Day Change Procedure (Compare 2 Mode or Compare 3 Mode).

20.5.3 Register Setting (Compare Data)

Write to the following registers when the BSY bit in the RTCSEC register is 0 (not while data is updated).

- Registers RTCCSEC, RTCCMIN, and RTCCHR

20.5.4 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read time data bits (1) when the BSY bit in the RTCSEC register is 0 (not while data is updated).
When reading multiple registers, if data is rewritten between reading registers, an errant time will be read.
In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of time data bits in the real-time clock interrupt routine.
- Monitoring by a program 1
  Monitor the IR bit in the RTCTIC register by a program and read necessary contents of time data bits after the IR bit in the RTCTIC register becomes 1 (periodic interrupt request generated).
- Monitoring by a program 2
  (1)Monitor the BSY bit.
  (2)Monitor until the BSY bit becomes 0 after the BSY bit becomes 1 (the BSY bit is set to 1 for approximately 62.5 ms).
  (3)Read necessary contents of time data bits after the BSY bit becomes 0.
- Using read results if they are the same value twice
  (1)Read necessary contents of time data bits.
  (2)Read the same bit as (1) and compare the contents.
  (3)Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

Note:
1. Time data bits are shown below.
   Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
   Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
   Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
   Bits WK2 to WK0 in the RTCWK
   The RTCPM bit in the RTCCR1 register

21. Pulse Width Modulator

Note

The 80-pin package does not have pins P4_6 and P4_7. Use pins P9_3 and P9_4 for PWM0 and PWM1 output.

21.1 Introduction

The pulse width modulator (PWM) consists of two independent PWM circuits. Table 21.1 lists PWM Specification, Figure 21.1 shows Block Diagram of PWM, and Table 21.2 lists I/O Port.

Table 21.1 PWM Specification

Item	Specification
Resolution	8 bits
Count source	f1 divided by 2, 4, 8, or 16
PWM Cycle	$\frac{(2^8 - 1) \times (m + 1)}{fj}$ (Unit : s) m: PWMPREi register setting value fj: Count source frequency (Unit : Hz)
High-level pulse width	$\frac{(m + 1) \times n}{fj}$ (Unit : s) m: PWMPREi register setting value n: PWMREGi register setting value fj: Count source frequency (Unit : Hz)
Selectable function	Select output pin: P4 or P9

i = 0, 1

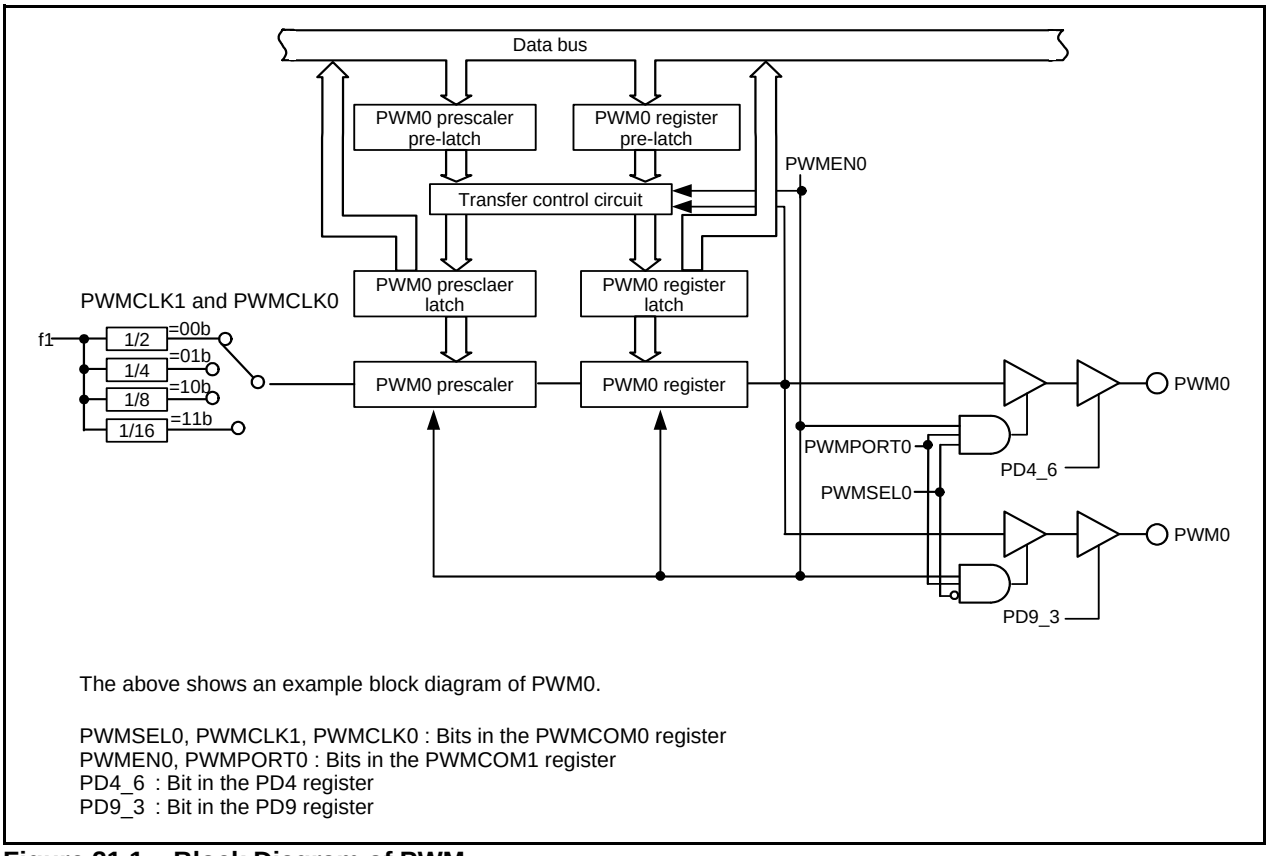


Figure 21.1 Block Diagram of PWM

Table 21.2 I/O Port

Port	I/O	Function
PWM0	O (1)	PWM output
PWM1		

Note:
1. Set the direction bit corresponding to selected pin to 1 (output mode)

21.2 Registers

Table 21.3 Register Structure

Address	Register Name	Symbol	After Reset
0370h	PWM Control Register 0	PWMCON0	00h
0372h	PWM0 Prescaler	PWMPRE0	00h
0373h	PWM0 Register	PWMREG0	00h
0374h	PWM1 Prescaler	PWMPRE1	00h
0375h	PWM1 Register	PWMREG1	00h
0376h	PWM Control Register 1	PWMCON1	00h

21.2.1 PWM Control Register 0 (PWMCON0)

PWM Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
		0	0	0	0		

Symbol	Address	After Reset
PWMCON0	0370h	00h

Bit Symbol	Bit Name	Function	RW
PWMSEL0	PWM0 output pin select bit	0: output PWM0 signal from P9_3 1: output PWM0 signal from P4_6	RW
PWMSEL1	PWM1 output pin select bit	0: output PWM1 signal from P9_4 1: output PWM1 signal from P4_7	RW
— (b5-b2)	Reserved bits	Set to 0	RW
PWMCLK0	PWM count source select bit	b7 b6 0 0: fi divided by 2 0 1: fi divided by 4 1 0: fi divided by 8 1 1: fi divided by 16	RW
PWMCLK1			RW

Set bits PWMSELi and PWMCLKi (i = 0, 1) in the PWMCON0 register when the PWMENi bit in the PWMCON1 register is 0 (PWMi output disabled).

PWMSEL0 (PWM0 Output Select Bit) (b0)

This bit select a PWM output pin. See Table 21.4 “PWM Pin and Bit Setting”.

PWMSEL1 (PWM1 Output Select Bit) (b1)

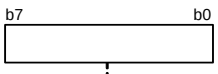
This bit select a PWM output pin. See Table 21.4 “PWM Pin and Bit Setting”.

PWMCLK1-PWMCLK0 (PWM Count Source Select Bit) (b7-b6)

Bits PWMCLK1 and PWMCLK0 select a count source for PWMi prescaler. Prescalers PWM0 and PWM1 share the same count source.

21.2.2 PWMi Prescaler (PWMPREi) (i = 0, 1)

PWMi Prescaler (i = 0, 1)



Symbol	Address	After Reset
PWMPRE0	0372h	00h
PWMPRE1	0374h	00h

Function	Setting Range	RW
PWM cycle	00h to FFh	RW

21.2.3 PWMi Register (PWMREGi) (i = 0, 1)

PWMi Register (i = 0, 1)

b7 b0

Symbol	Address	After Reset
PWMREG0	0373h	00h
PWMREG1	0375h	00h

Function	Setting Range	RW
Output high-level pulse width	00h to FFh	RW

The PWMi register (i = 0, 1) sets the PWMi cycle (i = 0, 1) and high-level pulse width. The PWM cycle and high-level pulse width are given by:

$$\text{PWM cycle} = \frac{(2^8 - 1) \times (m + 1)}{fj} \text{ (Unit : s)}$$

$$\text{High level pulse width} = \frac{(m + 1) \times n}{fj} \text{ (Unit : s)}$$

fj: PWM count source frequency (Unit : Hz)
m: PWMPREi register setting
n: PWMREGi register setting

The written value in the PWMPREi register is written into the PWMi prescaler prelatch. The state in the PWMi prescaler prelatch cannot be read. At the beginning of the next PWM cycle, the PWMi prescalser prelatch value is transferred to the PWMi prescaler latch and the PWMi prescaler, and then the associated PWMi waveform is output. When reading the PWMPREi register, the state in the PWMi prescaler latch can be read. (See Figure 21.1 “Block Diagram of PWM”)
The written value in the PWMREGi register is written into the PWMi register prelatch. The state in the PWMi register prelatch cannot be read. At the beginning of the next PWM cycle, the PWMi register prelatch value is transferred to the PWMi register latch and the PWMi register, and then the associated PWMi waveform is output. When reading the PWMREGi register, the state in the PWMi register latch can be read.
Therefore, the written value in registers PWMPREi and PWMREGi may differ from the values read from registers PWMPREi and PWMREGi.
Even if the PWMENi bit is set to 1 (PWMi output enabled) when the PWMPREi and PWMREGi register values are rewritten while the PWMENi bit in the PWMCON1 register is set to 0 (PWMi output disabled), the rewritten values are not reflected immediately. The values prior to the change are reflected for the first one cycle of PWM output. The values read from registers PWMPREi and PWMREGi during this cycle are the values prior to the change. When the second PWM cycle begins, the rewritten values should be read from registers PWMPREi and PWMREGi and the associated PWM waveform is output.
See 21.3.2 “Operation Example” for output waveforms and transfer timings.

21.2.4 PWM Control Register 1 (PWMCON1)

PWM Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

Symbol	Address	After Reset
PWMCON1	0376h	00h

Bit Symbol	Bit Name	Function	RW
PWMEN0	PWM0 output enable bit	0: output disabled 1: output enabled	RW
PWMEN1	PWM1 output enable bit	0: output disabled 1: output enabled	RW
PWMPORT0	PWM0 port switch bit	0: I/O port 1: PWM0 output	RW
PWMPORT1	PWM1 port switch bit	0: I/O port 1: PWM1 output	RW
— (b7-b4)	Reserved bits	Set to 0	RW

PWMEN0 (PWM0 Output Enable Bit) (b0)

The PWMEN0 bit is used to start PWM output. See Table 21.4 “PWM Pin and Bit Setting” for details.

PWMEN1 (PWM1 Output Enable Bit) (b1)

The PWMEN1 bit is used to start PWM output. See Table 21.4 “PWM Pin and Bit Setting” for details.

PWMPORT0 (PWM0 Port Switch Bit) (b2)

A PWM output pin can be selected. See Table 21.4 “PWM Pin and Bit Setting”.

PWMPORT1 (PWM1 Port Switch Bit) (b3)

A PWM output pin can be selected. See Table 21.4 “PWM Pin and Bit Setting”.

Table 21.4 PWM Pin and Bit Setting

Bit Setting			Pin Function or State			
PWMCON0 register	PWMCON1 register		i = 0		i = 1	
PWMSELi bit	PWMPORTi bit	PWMENi bit	P9_3	P9_4	P4_6	P4_7
0	0	0 or 1	I/O port or pin for other peripheral function		I/O port or pin for other peripheral function	
	1 (1)	0	PWM0 output level maintained (2)			
		1	PWM0 pulse output			
1	0	0 or 1	I/O port or pin for other peripheral function		I/O port or pin for other peripheral function	
	1 (1)	0			PWM1 output level maintained (2)	
		1			PWM1 pulse output	

i = 0, 1

Notes:

1. Set the direction bit corresponding to selected pin to 1 (output mode).
2. Even if the PWMENi bit is set from 1 to 0 during PWMi output, maintain the PWMi output remains unchanged. The PWM output signal is in the low-level state immediately after the MCU is reset.

21.3 Operations

21.3.1 Setting Procedure

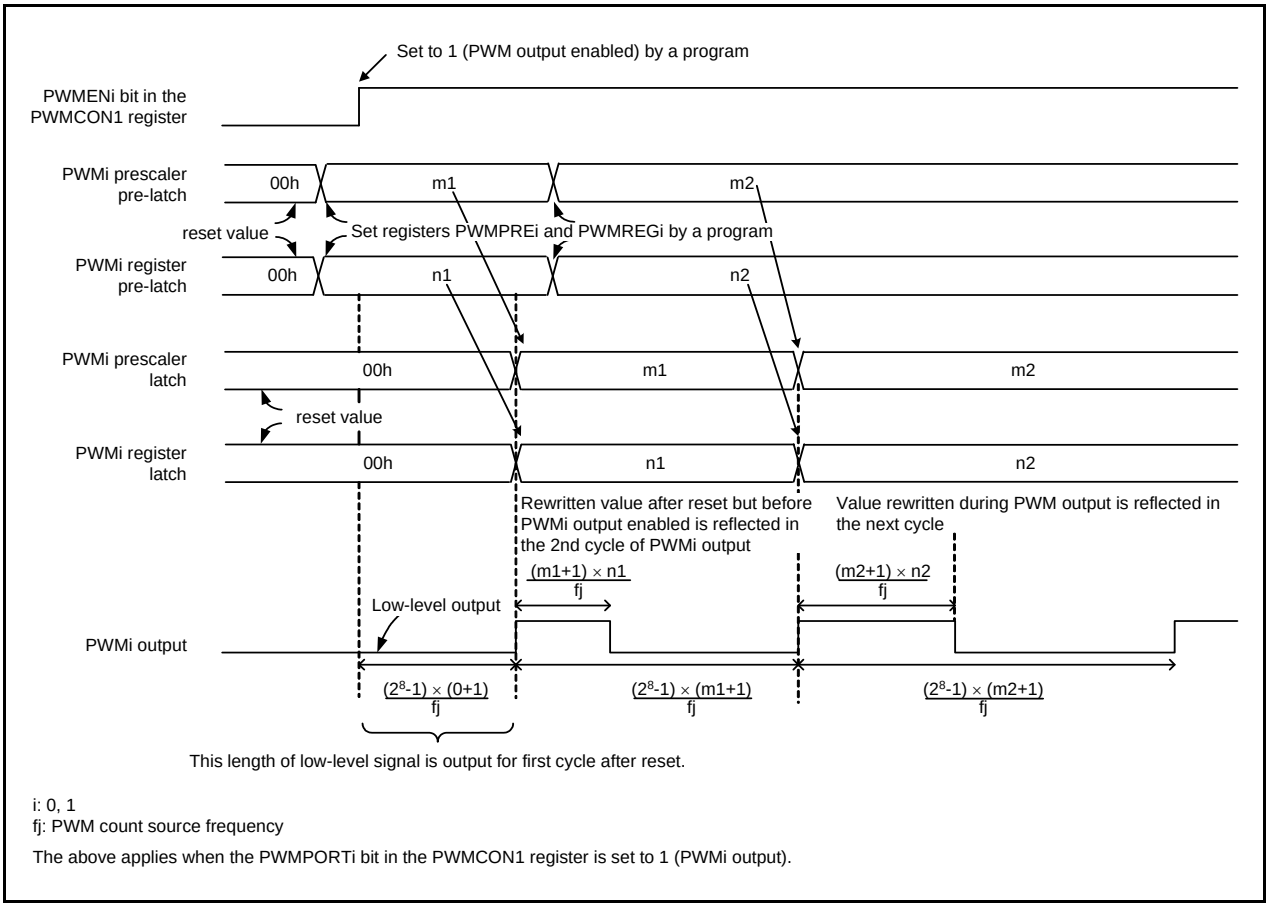
Follow the procedures below to set the individual register in order to start PWMi (i = 0, 1) output. (all SFRs are assumed to be reset. Refer the register descriptions to access registers or bits.)

(1) Write output data of the port corresponding to the pin for PWMi output to the P9 or P4 register. Then, set the direction bit for the corresponding port to 1 (output mode).
(2) Set the PWMSELi bit in the PWMCON0 register to select a pin for PWMi output. Set the PWMCLKi bit to select the count source.
(3) Set registers PWMPREi and PWMREGi to set the PWM cycle and high-level pulse width.
(4) Set the PWMPORTi bit in the PWMCON1 register to 1 (PWMi function) and the PWMENi bit to 1 (PWM output enabled).

21.3.2 Operation Example

The values written to the PWMPREi and PWMREGi register during PWMi (i = 0, 1) output is not reflected until the next cycle of PWMi output begins.

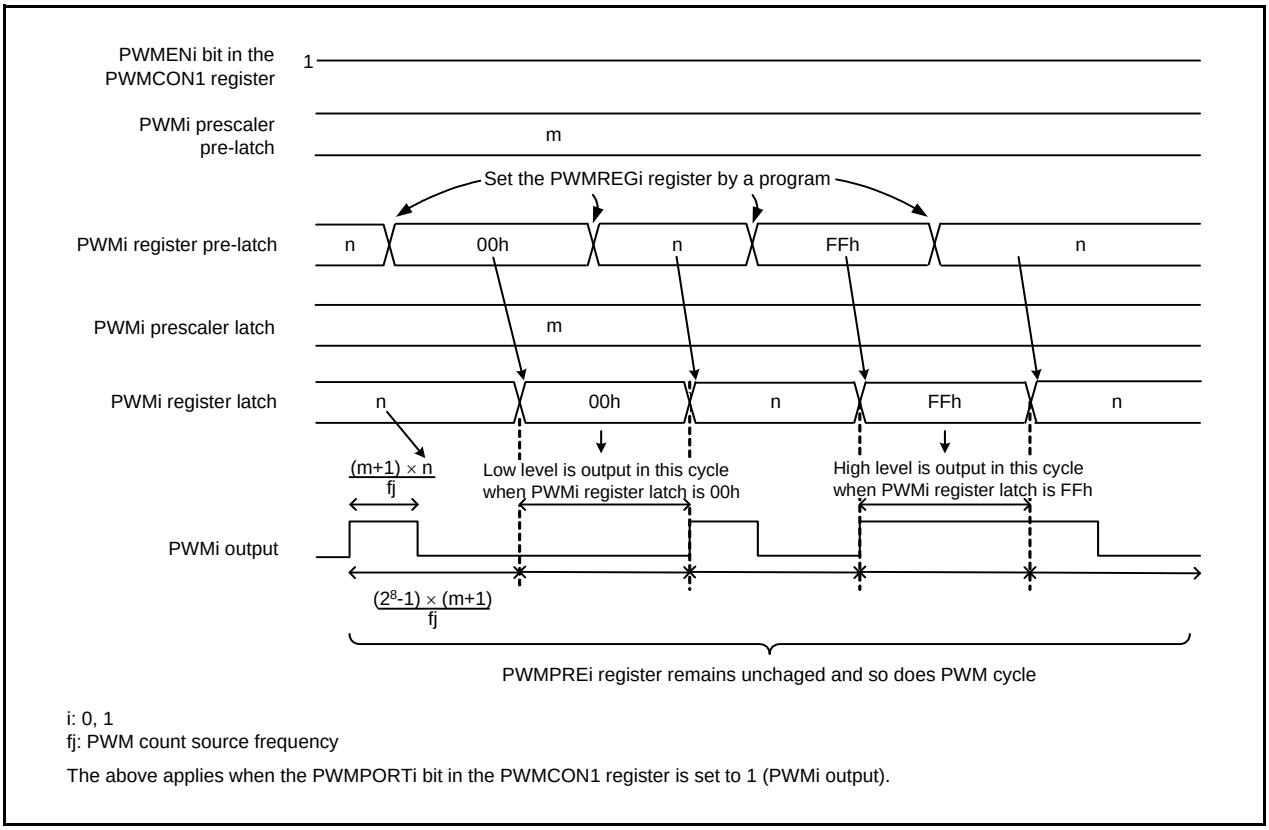
The PWM output signal is in the low state immediately after the MCU is reset. Then the associated waveform output starts. The PWMi output level remains unchanged even if the PWMENi bit is changed from 1 (PWMi output enabled) to 0 (PWMi output disabled) during PWMi output. Registers PWMPREi and PWMREGi maintains the value before the PWMi output is disabled. When the PWMENi bit is set to 1 after registers PWMPREi and PWMREGi are rewritten during PWMi output disabled, the PWMPREi and PWMREGi register values prior to the change are reflected for the first cycle of PWM output. The rewritten register values are reflected in the following PWMi cycle. Figure 21.2 to Figure 21.4 shows PWMi output examples.



i: 0, 1
fj: PWM count source frequency

The above applies when the PWMPORTi bit in the PWMCON1 register is set to 1 (PWMi output).

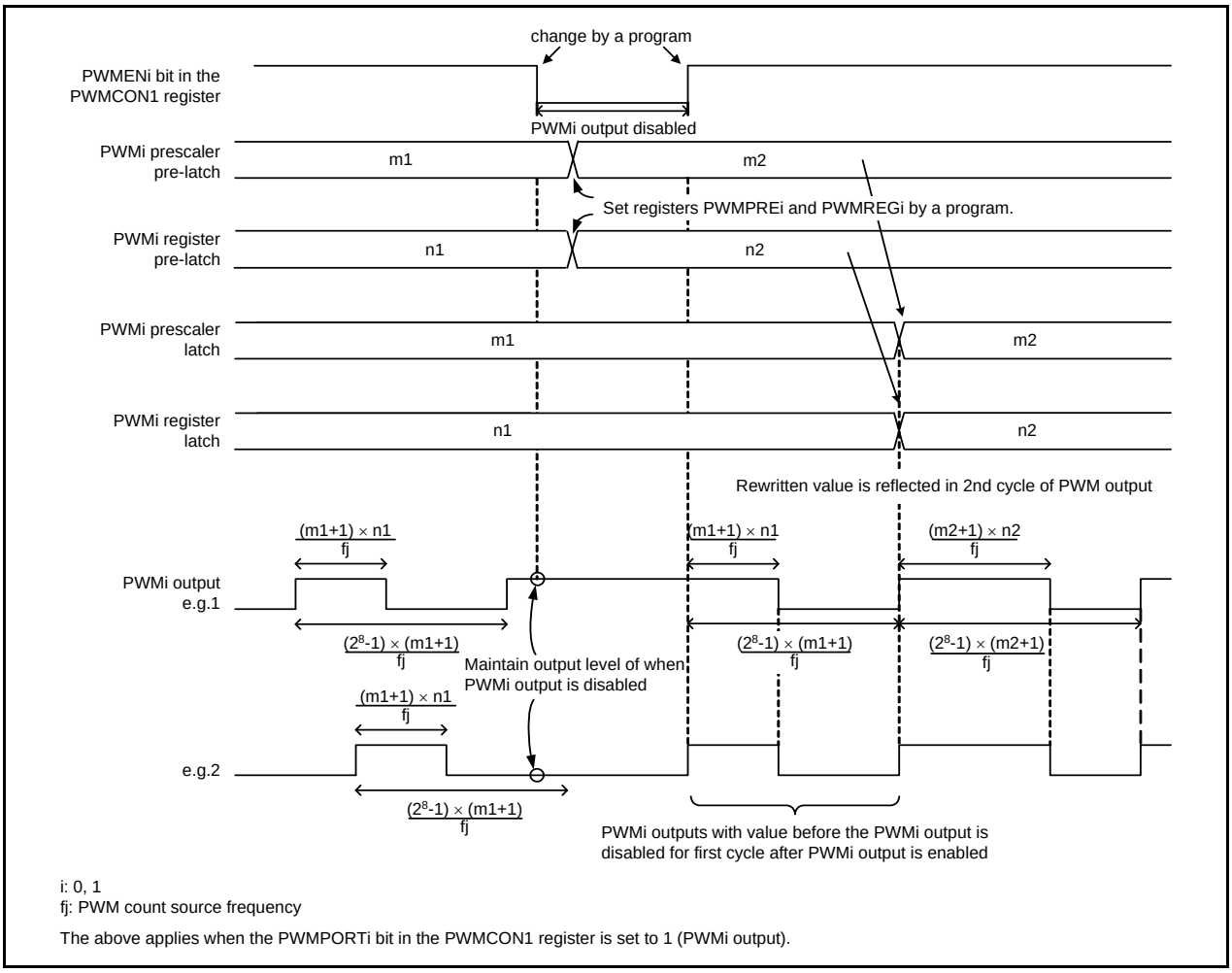
Figure 21.2 PWMi Output Example (after reset and during PWM output)



i: 0, 1
fj: PWM count source frequency

The above applies when the PWMPORTi bit in the PWMCON1 register is set to 1 (PWMi output).

Figure 21.3 PWMi Output Example (Duty 0%, Duty 100%)



i: 0, 1
fj: PWM count source frequency

The above applies when the PWMPORTi bit in the PWMCON1 register is set to 1 (PWMi output).

Figure 21.4 PWMi Output Example (PWM Output Disabled and PWM Output Resumed)

22. Remote Control Signal Receiver

Note

The 80-pin package does not have the PMC1 pin. Use the PMC0 pin for external pulse input.

22.1 Introduction

Remote control signal receiver has two circuits for checking width and period of external pulse.
Table 22.1 lists Remote Control Receiver Specifications, Figure 22.1 to Figure 22.3 show remote control signal receiver block diagram, and Table 22.2 lists Input/Output Pin.

Table 22.1 Remote Control Receiver Specifications

Item		Content	
		PMC0 circuit	PMC1 circuit
Count sources	Clock sources	One of the following • fC • f1 • Timer B2 underflow • Count source of PMC1	One of the following • fC • f1 • Timer B1 underflow • Timer B2 underflow
	Division	No division, divided-by-8, divided-by-32, or divided-by-64	
Count operation		Increment	
Operation modes		• Pattern match mode Determines that external pulse matches specified pattern • Input capture mode Measures width and period of external pulse	
Pattern match mode	Detect patterns	• Header • Data 0 • Data 1 • Special data	
	Receive buffer	6 bytes (48 bits)	None
	Interrupt request generation timing	• Receive error • Completion of data reception • Header match • Data 0/1 match • Special data match • Receive buffer full • Compare match	• Receive error • Completion of data reception • Header match • Data 0/1 match
	Selectable functions	• Input signal inversion • Digital filter	
Input capture mode	Measurement items	• Pulse period (between rising edge and rising edge) • Pulse period (between falling edge and falling edge) • Pulse width	
	Interrupt request generation timing	• Timer measurement • Counter overflow	
	Selectable functions	• Input signal inversion • Digital filter • Individual count of two inputs or simultaneous count of two inputs	

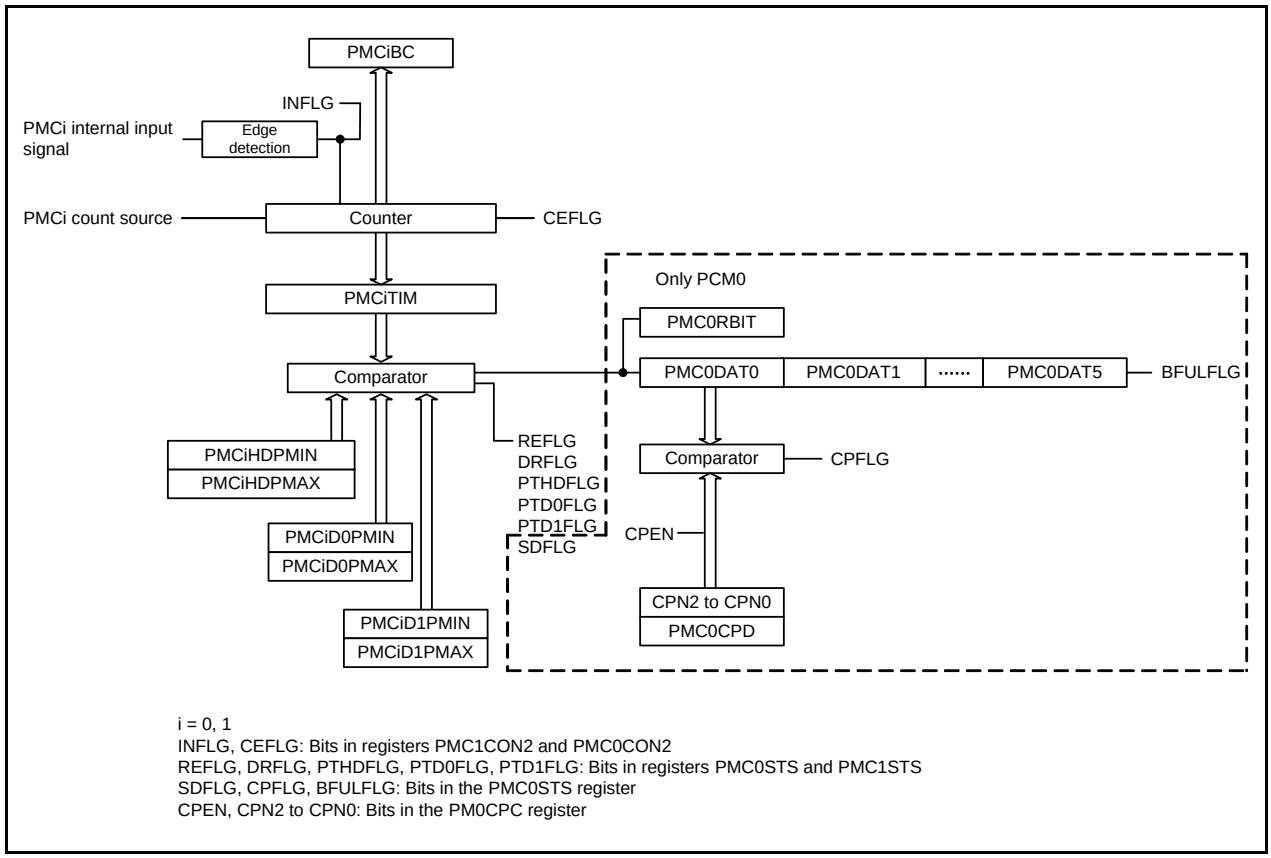


Figure 22.1 Remote Control Signal Receiver Block Diagram (1/3)

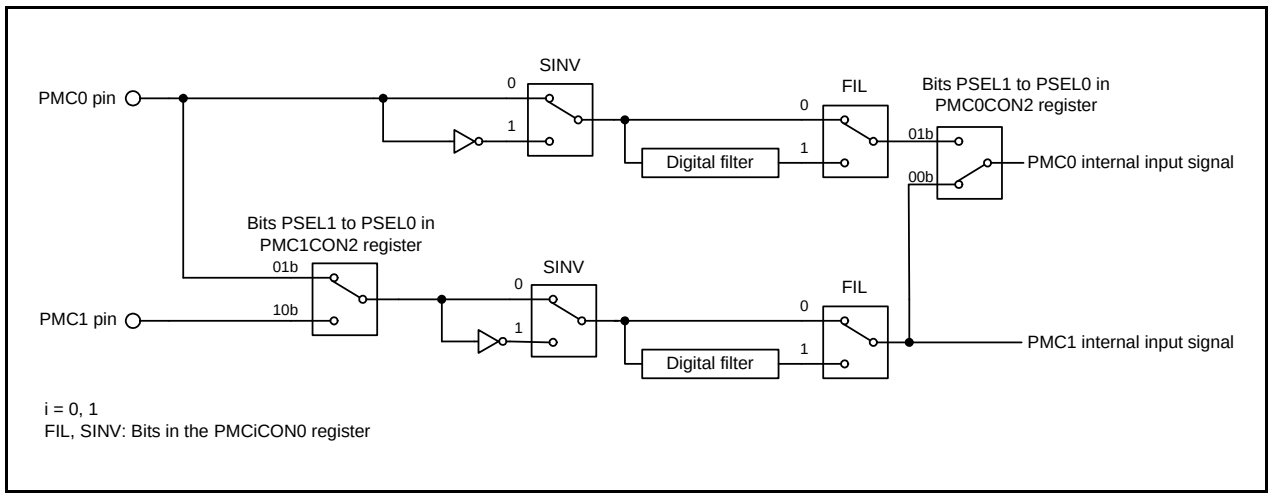


Figure 22.2 Remote Control Signal Receiver Block Diagram (2/3) (PMCi Input)

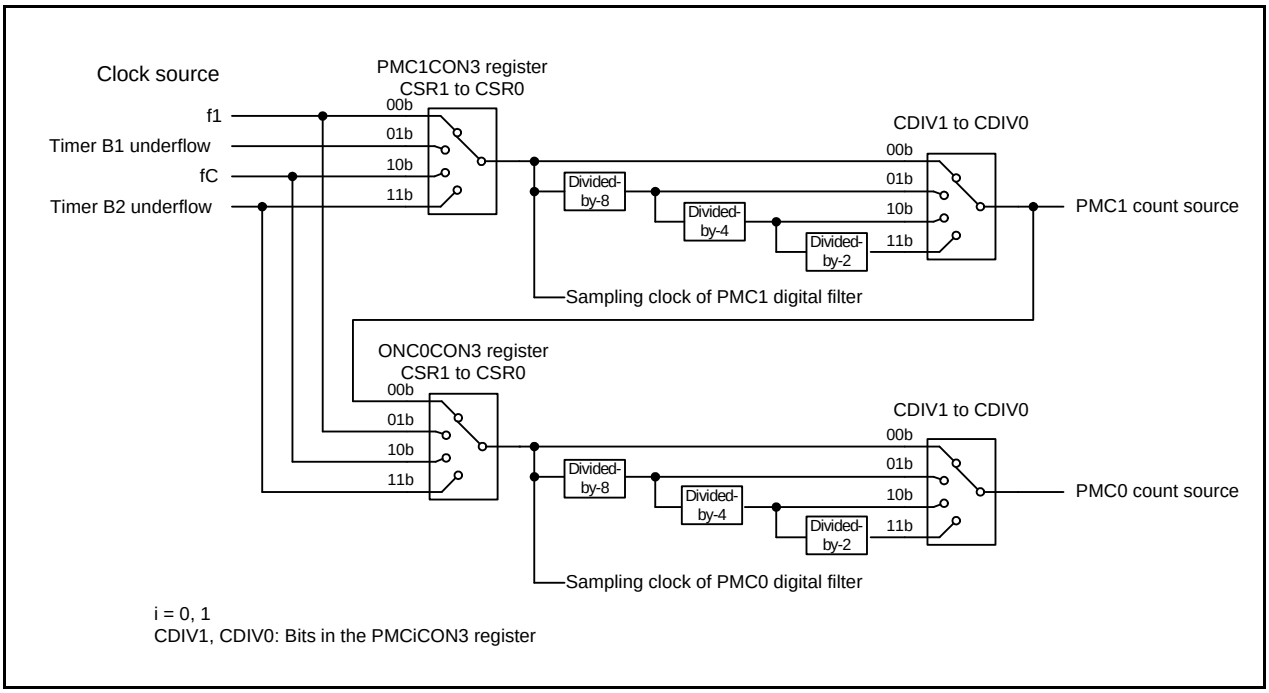


Figure 22.3 Remote Control Signal Receiver Block Diagram (3/3) (PMCi Count Source)

Table 22.2 Input/Output Pin

Pin Name	Input/Output	Function
PMC0	Input (1)	External pulse input
PMC1		

Note:
1. Set the port direction bits sharing pins to 0 (input mode).

22.2 Registers

Table 22.3 Register Structure (PMC0 Circuit)

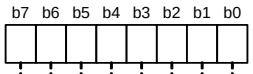
Address	Register Name	Register Symbol	After Reset
01F0h	PMC0 Function Select Register 0	PMC0CON0	00h
01F1h	PMC0 Function Select Register 1	PMC0CON1	00XX 0000b
01F2h	PMC0 Function Select Register 2	PMC0CON2	00h
01F3h	PMC0 Function Select Register 3	PMC0CON3	00h
01F4h	PMC0 Status Register	PMC0STS	00h
01F5h	PMC0 Interrupt Source Select Register	PMC0INT	00h
01F6h	PMC0 Compare Control Register	PMC0CPC	XXX0 X000b
01F7h	PMC0 Compare Data Register	PMC0CPD	00h
D080h D081h	PMC0 Header Pattern Set Register (Min)	PMC0HDPMIN	00h XXXX X000b
D082h D083h	PMC0 Header Pattern Set Register (Max)	PMC0HDPMAX	00h XXXX X000b
D084h	PMC0 Data0 Pattern Set Register (Min)	PMC0D0PMIN	00h
D085h	PMC0 Data0 Pattern Set Register (Max)	PMC0D0PMAX	00h
D086h	PMC0 Data1 Pattern Set Register (Min)	PMC0D1PMIN	00h
D087h	PMC0 Data1 Pattern Set Register (Max)	PMC0D1PMAX	00h
D088h D089h	PMC0 Measurements Register	PMC0TIM	0000h
D08Ah D08Bh	PMC0 Counter Value Register	PMC0BC	0000h
D08Ch	PMC0 Receive Data Store Register 0	PMC0DAT0	00h
D08Dh	PMC0 Receive Data Store Register 1	PMC0DAT1	00h
D08Eh	PMC0 Receive Data Store Register 2	PMC0DAT2	00h
D08Fh	PMC0 Receive Data Store Register 3	PMC0DAT3	00h
D090h	PMC0 Receive Data Store Register 4	PMC0DAT4	00h
D091h	PMC0 Receive Data Store Register 5	PMC0DAT5	00h
D092h	PMC0 Receive Bit Count Register	PMC0RBIT	XX00 0000b

Table 22.4 Register Structure (PMC1 Circuit)

Address	Register Name	Register Symbol	After Reset
01F8h	PMC1 Function Select Register 0	PMC1CON0	XXX0 X000b
01F9h	PMC1 Function Select Register 1	PMC1CON1	XXXX 0X00b
01FAh	PMC1 Function Select Register 2	PMC1CON2	00h
01FBh	PMC1 Function Select Register 3	PMC1CON3	00h
01FCh	PMC1 Status Register	PMC1STS	X000 X00Xb
01FDh	PMC1 Interrupt Source Select Register	PMC1INT	X000 X00Xb
D094h D095h	PMC1 Hedder Pattern Set Register (Min)	PMC1HDPMIN	00h XXXX X000b
D096h D097h	PMC1 Header Pattern Set Register (Max)	PMC1HDPMAX	00h XXXX X000b
D098h	PMC1 Data0 Pattern Set Register (Min)	PMC1D0PMIN	00h
D099h	PMC1 Data0 Pattern Set Register (Max)	PMC1D0PMAX	00h
D09Ah	PMC1 Data1 Pattern Set Register (Min)	PMC1D1PMIN	00h
D09Bh	PMC1 Data1 Pattern Set Register (Max)	PMC1D1PMAX	00h
D09Ch D09Dh	PMC1 Measurements Register	PMC1TIM	00h 00h
D09Eh D09Fh	PMC1 Counter Value Register	PMC1BC	00h 00h

22.2.1 PMCi Function Select Register (PMCiCON0) (i = 0, 1)

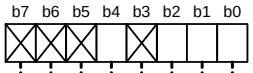
PMC0 Function Select Register 0



Symbol	Address	After Reset
PMC0CON0	01F0h	00h

Bit Symbol	Bit Name	Function	RW
EN	PMC0 operation enable bit	0: Operation disabled 1: Operation enabled	RW
SINV	Input signal polarity invert bit	0: Not inverted 1: Inverted	RW
FIL	Filter enable bit	0: Filter disabled 1: Filter enabled	RW
EHOLD	Error flag hold bit	State of the REFLG bit in the PMCiSTS register: 0: Held until next data received 1: Held even after next data received	RW
HDEN	Header pattern enable bit	0: Header disabled 1: Header enabled	RW
SDEN	Special data pattern enable bit	0: Special data pattern disabled 1: Special data pattern enabled	RW
DRINT0	Receive interrupt control bit	Interrupt request is generated under the following conditions: b7 b6 0 0: When reception completed 0 1: When compare match occurs and reception completed 1 0: When no receive error occurs and reception completed 1 1: When compare match and no receive error occurs, and reception completed	RW
DRINT1			

PMC1 Function Select Register 0



Symbol	Address	After Reset
PMC1CON0	01F8h	XXX0 X000b

Bit Symbol	Bit Name	Function	RW
EN	PMC1 operation enable bit	0: Operation disabled 1: Operation enabled	RW
SINV	Input signal polarity invert bit	0: Not inverted 1: Inverted	RW
FIL	Filter enable bit	0: Filter disabled 1: Filter enabled	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value.		—
HDEN	Header pattern enable bit	0: Header disabled 1: Header enabled	RW
— (b7-b5)	No register bits. If necessary, set to 0. Read as undefined value.		—

EN (PMC0 Operation Enable Bit) (b0)

The EN bit is used to control start/stop of PMCi operation. Confirm that the operation has started or stopped by the ENFLG bit in the PMCiCON2 register.

EHOLD (Error Flag Hold Bit) (b3)

When receive error occurs, period when the REFLG bit in the PMC0STS register holds 1 (receive error) can be selected. Refer to “REFLG (Receive Error Flag) (b1)” in 22.2.5 “PMCi Status Register (PMCiSTS) (i = 0, 1)” for details.

HDEN (Header Pattern Enable Bit) (b4)

If the HDEN bit is set to 1 (header enabled), the following occur when detecting data 0, data 1, or special data before detecting header.

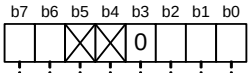
- The REFLG bit in the PMCiSTS register becomes 1 (error occurs)
- Bits PTD0FLG, PTD1FLG, and SDFLG in the PMCiSTS register remain unchanged.
- Registers PMCDAT0 to PMCDAT5 remain unchanged.

DRINT1-DRINT0 (Receive Interrupt Control Bit) (b7-b6)

A condition for generating a data reception complete interrupt request can be selected.
Set the DRINT bit in the PMC0INT register to 1 (reception complete interrupt enabled) after setting bits DRINT1 to DRINT0.
When setting the DRINT1 bit to 1, set the EHOLD bit in the PMC0CON0 register to 1 (hold the REFLG bit state after next data received).

22.2.2 PMCi Function Select Register (PMCiCON1) (i = 0, 1)

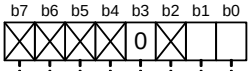
PMC0 Function Select Register 1



Symbol: PMC0CON1 | Address: 01F1h | After Reset: 00XX 0000b

Bit Symbol	Bit Name	Function	RW
TYP0	Receive mode select bit	b1 b0 0 0 : Period measurement (between rising edge and rising edge) 0 1 : In pattern match mode, high level width measurement (between rising edge and falling edge) In input capture mode, period measurement (between falling edge and falling edge) 1 0 : Pulse width measurement (between rising edge and falling edge, and falling edge and rising edge) 1 1 : Do not set.	RW
TYP1			
CSS	Counter start control bit	0: Counters operate individually 1: Counters operate simultaneously	RW
— (b3)	Reserved bit	Set to 0.	RW
— (b5-b4)	No register bits. If necessary, set to 0. Read as undefined value.		—
EXSDEN	Special pattern detect block select bit	0: PMC0 1: PMC1	RW
EXHDEN	Header pattern detect block select bit	0: PMC0 1: PMC1	RW

PMC1 Function Select Register 1



Symbol: PMC1CON1 | Address: 01F9h | After Reset: XXXX 0X00b

Bit Symbol	Bit Name	Function	RW
TYP0	Receive mode select bit	b1 b0 0 0 : Period measurement (between rising edge and rising edge) 0 1 : In pattern match mode, high level width measurement (between rising edge and falling edge) In input capture mode, period measurement (between falling edge and falling edge) 1 0 : Pulse width measurement (between rising edge and falling edge, and falling edge and rising edge) 1 1 : Do not set.	RW
TYP1			
— (b2)	No register bit. If necessary, set to 0. Read as undefined value.		—
— (b3)	Reserved bit	Set to 0.	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value.		—

EXSDEN (Special Pattern Detect Block Select Bit) (b6)
EXHDEN (Header Pattern Detect Block Select Bit) (b7)

Use these bits when PMC0 and PMC1 are linked and operated in pattern match mode. Otherwise, set to 0.

Set bits EXHDEN and EXSDEN to 01b or 10b when setting the HDEN bit in the PMC0CON0 register to 1 (header enabled) and SDEN bit to 1 (special data enabled).

22.2.3 PMCi Function Select Register 2 (PMCiCON2) (i = 0, 1)

PMC0 Function Select Register 2

b7	b6	b5	b4	b3	b2	b1	b0
					0		

Symbol	Address	After Reset
PMC0CON2	01F2h	00h

Bit Symbol	Bit Name	Function	RW
ENFLG	PMC0 status flag	0: Stops 1: Operating	RO
— (b1)	Reserved bit	Read as undefined value	RO
— (b2)	Reserved bit	Set to 0	RW
INFLG	Input signal flag	0: PMCi internal input signal level is low 1: PMCi internal input signal level is high	RO
CEFLG	Counter overflow flag	0: No overflow 1: Overflows	RO
CEINT	Counter overflow interrupt enable bit	0: Disabled 1: Enabled	RW
PSEL0	Input pin select bit	b7 b6 0 0 : Same as PMC1 0 1 : PMC0 pin 1 0 : Do not set 1 1 : Do not set	RW
PSEL1			

PMC1 Function Select Register 2

b7	b6	b5	b4	b3	b2	b1	b0
					0		

Symbol	Address	After Reset
PMC1CON2	01FAh	00h

Bit Symbol	Bit Name	Function	RW
ENFLG	PMC1 status flag	0: Stops 1: Operating	RO
— (b1)	Reserved bit	Read as undefined value	RO
— (b2)	Reserved bit	Set to 0	RW
INFLG	Input signal flag	0: PMCi internal input signal level is low 1: PMCi internal input signal level is high	RO
CEFLG	Counter overflow flag	0: No overflow 1: Overflows	RO
CEINT	Counter overflow interrupt enable bit	0: Disabled 1: Enabled	RW
PSEL0	Input pin select bit	b7 b6 0 0 : In an idle state 0 1 : PMC0 pin 1 0 : PMC1 pin 1 1 : Do not set	RW
PSEL1			

CEFLG (Counter Overflow Flag) (b4)

Condition to become 0:

- The EN bit is 0 (PMCi operation stops)
- Measurement timing selected by bits TYP1 to TYP0 in the PMCiCON1 register

Condition to become 1:

- The first counter overflow (the value exceeds FFFFh)

PSEL1-PSEL0 (Input Pin Select Bit) (b7-b6)

Change these bits when the EN bit in the PMCiCON0 register and the ENFLG bit in the PMCiCON2 register are both 0 (PMCi stops).

22.2.4 PMCi Function Select Register 3 (PMCiCON3) (i = 0, 1)

PMC0 Function Select Register 3

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
								PMC0CON3	01F3h	00h

Bit Symbol	Bit Name	Function	RW
CRE	Mode select bit	b3 b2 b1 b0 0 0 0 0 : Pattern match mode 1 1 1 1 : Input capture mode Do not set values not listed above.	RW
CFR			
CST			
PD			
CSRC0	Clock source select bit	b5 b4 0 0 : Same as PMC1 0 1 : f1 1 0 : fC1 1 1 : Timer B2 underflow	RW
CSRC1			
CDIV0	Count source divisor select bit	b7 b6 0 0 : No division 0 1 : Divided-by-8 1 0 : Divided-by-32 1 1 : Divided-by-64	RW
CDIV1			

PMC1 Function Select Register 3

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
								PMC1CON3	01FBh	00h

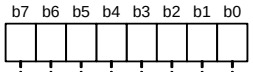
Bit Symbol	Bit Name	Function	RW
CRE	Mode select bit	b3 b2 b1 b0 0 0 0 0 : Pattern match mode 1 1 1 1 : Input capture mode Do not set values not listed above.	RW
CFR			
CST			
PD			
CSRC0	Clock source select bit	b5 b4 0 0 : f1 0 1 : Timer B1 underflow 1 0 : fC1 1 1 : Timer B2 underflow	RW
CSRC1			
CDIV0	Count source divisor select bit	b7 b6 0 0 : No division 0 1 : Divided-by-8 1 0 : Divided-by-32 1 1 : Divided-by-64	RW
CDIV1			

CDIV1-CDIV0 (Clock Source Select Bit) (b5-b4)

When bits CSCR1 to CSCR0 in the PMC0CON3 register is set to 00b (same as PMC1), set bits CDIV1 to CDIV0 in the PMC0CON3 register to 00b (no division).

22.2.5 PMCi Status Register (PMCiSTS) (i = 0, 1)

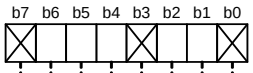
PMC0 Status Register



Symbol: PMC0STS | Address: 01F4h | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
CPFLG	Compare match flag	0: Not match 1: Match	RO
REFLG	Receive error flag	0: No error occurs 1: Error occurs	RO
DRFLG	Data receiving flag	0: Waiting for data reception 1: Data receiving	RO
BFULFLG	Receive buffer full flag	0: Receive buffer empty 1: Receive buffer full (48 bits received)	RO
PTHDFLG	Header pattern match flag	0: Not match 1: Match	RO
PTD0FLG	Data 0 pattern match flag	0: Not match 1: Match	RO
PTD1FLG	Data 1 pattern match flag	0: Not match 1: Match	RO
SDFLG	Special pattern match flag	0: Not match 1: Match	RO

PMC1 Status Register



Symbol: PMC1STS | Address: 01FCh | After Reset: X000 X00Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. Read as undefined value.		—
REFLG	Receive error flag	0: No error occurs 1: Error occurs	RO
DRFLG	Data receiving flag	0: Waiting for data reception 1: Data receiving	RO
— (b3)	No register bit. If necessary, set to 0. Read as undefined value.		—
PTHDFLG	Header pattern match falg	0: Not match 1: Match	RO
PTD0FLG	Data 0 pattern match flag	0: Not match 1: Match	RO
PTD1FLG	Data 1 pattern match flag	0: Not match 1: Match	RO
— (b7)	No register bit. If necessary, set to 0. Read as undefined value.		—

CPFLG (Compare Match Flag) (b0)

This bit is valid when the CPEN bit in the PMC0CPC register is set to 1 (compare enabled).
Condition to become 0:

- When the DRFLG bit in the PMC0STS register changes from 0 to 1 (next frame reception starts).
- When the 48th bit is received after the CPFLG bit becomes 1, and then (the DRFLG bit remains 1 (receiving)) no compare match occurs after receiving bit n (n = value set by bits CPN2 to CPN0 in the PMC0CPC register)

Condition to become 1:

- The PMC0CPD register matches the PMC0DAT0 register (when the setting value of bits CPN2 to CPN0 in the PMC0CPC register is n, bits n to 0 in the PMC0CPD register matches bits n to 0 in the PMC0DAT0 register).

REFLG (Receive Error Flag) (b1)

The REFLG bit is a flag indicating receive error. Conditions for changing the REFLG bit are affected by the HDEN bit in the PMCiCOM0 register and bits EHOLD and SDEN in the PMC0COM0 register. Table 22.5 lists Conditions for Changing the REFLG Bit.

Table 22.5 Conditions for Changing the REFLG Bit

Bit Setting (1)		Conditions for Changing the REFLG Bit to 1 (2)	Conditions for Changing the REFLG bit to 0 (2)(3)
EHOLD	HDEN		
0	0	Input signal width is neither data 0 nor data 1 (special data)	Receive data 0 or data 1 (or special data)
0	1	• Input signal width is none of header, data 0, or data 1 (special data) • Detect data 0 or data 1 (or special data) prior to header	• Receive header • Receive header prior to data 0 or data 1 (or special data)
1	0	Input signal width is neither data 0 nor data 1 (special data)	-
1	1	• Input signal width is none of header, data 0, or data 1 (special data) • Detect data 0 or data1 (or special data) prior to header	• Receive header

EHOLD: Bit in the PMC0COM0 register
HDEN: Bit in the PMCiCOM0 register (i = 0, 1)
Notes:

1. Refer to EHOLD = 0 when operating PMC1 individually.
2. Special data is added to the conditions when the SDEN bit in the PMC0COM0 register is 1 (special data enabled)
3. The REFLG bit becomes 0 regardless of bits HEDN and EHOLD under the following conditions:
   - EN bit is 0 (PMCi stops)
   - The DRFLG bit in the PMCiSTS register changes from 0 to 1 (next frame reception starts)

DRFLG (Data Receiving Flag) (b2)

The DRFLG bit indicates the receiving state of the remote control signal.
Condition to become 0:

- The counter value is larger than values of registers PMCiHDPMAX, PMCiD0PMAX, and PMCiD1PMAX (if the counter value is larger than these register values, this bit becomes 0 after waiting for 1 to 2 cycles of the count source).

Condition to become 1:
It depends on bits TYP1 to TYP0 in the PMCiCON1 register (receive mode select).

- When bits TYP1 to TYP0 are 00b (pulse period measurement) or 01b (high level width measurement):
  rising edge of the PMCi internal input signal
- When bits TYP1 to TYP0 are 10b (pulse width measurement):
  rising edge and falling edge of the PMCi internal input signal

BFULFLG (Receive Buffer Full Flag) (b3)

Condition to become 0:

- The value of the PMC0RBIT register changes from 48 to 1.

Condition to become 1:

- The value of the PMC0RBIT register is 48.

PTHDFLG (Header Pattern Match Flag) (b4), PTD0FLG (Data 0 Pattern Match Flag) (b5), PTD1FLG (Data 1 Pattern Match Flag) (b6), SDFLG (Special Pattern Match Flag) (b7)

Condition to become 0:

- The EN bit is 0 (PMCi stops)
- DRFLG bit in the PMCiSTS register changes from 0 to 1 (next frame reception starts)
- Refer to Table 22.6 “Measurements and Flag”.

Condition to become 1:

- Refer to Table 22.6 “Measurements and Flag”.

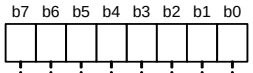
Table 22.6 Measurements and Flag

Value (Measurements) of the PMCiTIM Register	Flag			
	PTHDFLG	PTD0FLG	PTD1FLG	SDFLG
Between PMCiHDPMIN and PMCiHDPMAX (header measurement in PMCi)	1	0	0	0
Between PMCiD0PMIN and PMCiD0PMAX	0	1 (1)	0	0
Between PMCiD1PMIN and PMCiD1PMAX	0	0	1 (1)	0
Between PMCiHDPMIN and PMCiHDPMAX (special data measurement in PMCi)	0	0	0	1 (1)
Other than those above	0	0	0	0

Note:
1. When the HDEN bit in the PMCiCON0 register is 1(header enabled), PTD0FLG, PTD1FLG, and SDFLG remain unchanged until header is detected.

22.2.6 PMCi Interrupt Source Register (PMCiINT) (i = 0, 1)

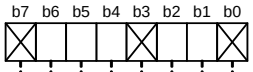
PMC0 Interrupt Source Register



Symbol	Address	After Reset
PMC0INT	01F5h	00h

Bit Symbol	Bit Name	Function	RW
CPINT	Compare match flag interrupt enable bit	0: Disabled 1: Enabled	RW
REINT	Receive error flag interrupt enable bit	0: Disabled 1: Enabled	RW
DRINT	Data reception complete interrupt enable bit	0: Disabled 1: Enabled	RW
BFULINT	Receive buffer full flag interrupt enable bit	0: Disabled 1: Enabled	RW
PTHDINT	Header match flag interrupt enable bit	0: Disabled 1: Enabled	RW
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled 1: Enabled	RW
TIMINT	Timer measure interrupt enable bit	0: Disabled 1: Enabled	RW
SDINT	Special data match flag interrupt enable bit	0: Disabled 1: Enabled	RW

PMC1 Interrupt Source Register

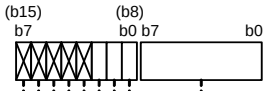


Symbol	Address	After Reset
PMC1INT	01FDh	X000 X00Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. Read as undefined value.		—
REINT	Receive error flag interrupt enable bit	0: Disabled 1: Enabled	RW
DRINT	Data reception complete interrupt enable bit	0: Disabled 1: Enabled	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value.		—
PTHDINT	Header match flag interrupt enable bit	0: Disabled 1: Enabled	RW
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled 1: Enabled	RW
TIMINT	Timer measure interrupt enable bit	0: Disabled 1: Enabled	RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value.		—

22.2.7 PMCi Header Pattern Set Register (MIN) (PMCiHDPMIN) (i = 0, 1)
PMCi Header Pattern Set Register (MAX) (PMCiHDPMAX) (i = 0, 1)

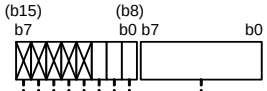
PMCi Header Pattern Set Register (MIN) (i = 0, 1)



Symbol	Address	After Reset
PMC0HDPMIN	D081h to D080h	XXXX X000 0000 0000b
PMC1HDPMIN	D095h to D094h	XXXX X000 0000 0000b

Function	Setting Range	RW
Set the minimum width of header pattern or special data pattern.	0000h to 07FFh	RW
No register bits. If necessary, set to 0. Read as undefined value.		—

PMCi Header Pattern Set Register (MAX) (i = 0, 1)



Symbol	Address	After Reset
PMC0HDPMAX	D083h to D082h	XXXX X000 0000 0000b
PMC1HDPMAX	D097h to D096h	XXXX X000 0000 0000b

Function	Setting Range	RW
Set the maximum width of header pattern or special data pattern.	0000h to 07FFh	RW
No register bits. If necessary, set to 0. Read as undefined value.		—

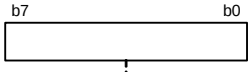
Set the minimum width of header or special data pattern to the PMCiHDPMIN register and the maximum width to the PMCiHDPMAX.

$$\text{Setting value n} = \frac{\text{Minimum width (maximum width) of header or special data pattern}}{\text{Count source}}$$

Set the different value from data 0 or data 1 to these register.
Set the following: PMCiHDPMIN register value < PMCiHDPMAX register value.
When not using header or special data detection, set registers PMCiHDPMIN and PMCiHDPMAX to 0000h.

22.2.8 PMCi Data 0 Pattern Set Register (MIN) (PMCiD0PMIN) (i = 0, 1)
PMCi Data 0 Pattern Set Register (MAX) (PMCiD0PMAX) (i = 0, 1)
PMCi Data 1 Pattern Set Register (MIN) (PMCiD1PMIN) (i = 0, 1)
PMCi Data 1 Pattern Set Register (MAX) (PMCiD1PMAX) (i = 0, 1)

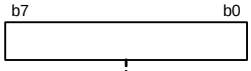
PMCi Data 0 Pattern Set Register (MIN) (i = 0, 1)



Symbol	Address	After Reset
PMC0D0PMIN	D084h	00h
PMC1D0PMIN	D098h	00h

Function	Setting Range	RW
Set the minimum width of data 0 pattern.	00h to FFh	RW

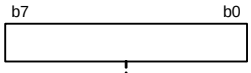
PMCi Data 0 Pattern Set Register (MAX) (i = 0, 1)



Symbol	Address	After Reset
PMC0D0PMAX	D085h	00h
PMC1D0PMAX	D099h	00h

Function	Setting Range	RW
Set the maximum width of data 0 pattern.	00h to FFh	RW

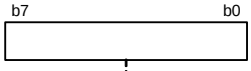
PMCi Data 1 Pattern Set Register (MIN) (i = 0, 1)



Symbol	Address	After Reset
PMC0D1PMIN	D086h	00h
PMC1D1PMIN	D09Ah	00h

Function	Setting Range	RW
Set the minimum width of data 1 pattern.	00h to FFh	RW

PMCi Data 1 Pattern Set Register (MAX) (i = 0, 1)



Symbol	Address	After Reset
PMC0D1PMAX	D087h	00h
PMC1D1PMAX	D09Bh	00h

Function	Setting Range	RW
Set the maximum width of data 1 pattern.	00h to FFh	RW

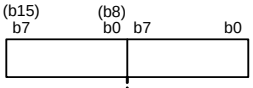
Set the minimum width of data 0 pattern to the PMCiD0PMIN register and the maximum width to the PMCiD0PMAX register. Also set the minimum width of data 1 pattern to the PMCiD1PMIN register and the maximum width to the PMCiD1PMAX register.

$$\text{Setting value n} = \frac{\text{minimum width (maximum width) of data 0/1 pattern}}{\text{count source}}$$

Data 0, data 1, and header or special data pattern must be the different values. Set the following: PMCiD0PMIN register value < PMCiD0PMAX register value, and PMCiD1PMIN < PMCiD1PMAX. When not detecting data 0, registers PMCiD0PMIN and PMCiD0PMAX to 00h. When not detecting data 1, registers PMCiD1PMIN and PMCiD1PMAX to 00h.

22.2.9 PMCi Measurements Register (PMCiTIM) (i = 0, 1)

PMCi Measurements Register

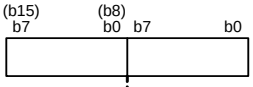


Symbol	Address	After Reset
PMC0TIM	D089h to D088h	0000h
PMC1TIM	D09Dh to D09Ch	0000h

Function	RW
Measurements of pulse period and pulse width can be read.	RO

22.2.10 PMCi Counter Value Register (PMCiBC) (i = 0, 1)

PMCi Counter Value Register (i = 0, 1)

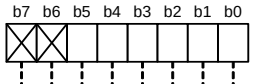


Symbol	Address	After Reset
PMC0BC	D08Bh to D08Ah	0000h
PMC1BC	D09Fh to D09Eh	0000h

Function	RW
The state of the counter can be read.	RO

22.2.11 PMC0 Receive Bit Count Register (PMC0RBIT)

PMC0 Receive Bit Count Register



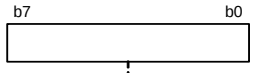
Symbol	Address	After Reset
PMC0RBIT	D092h	XX00 0000b

Function	RW
Receive bit count can be read.	RO
No register bit. If necessary, set to 0. Read as undefined value.	—

Bit position of the storing buffer is specified by counting detected data 0/1.
When the receive bit count exceeds 48, it returns 1. Header and special data are not counted.
When the DRFLG bit in the PMC0STS register changes from 0 to 1, the PMC0RBIT register becomes 0.

22.2.12 PMC0 Receive Data Store Register i (PMC0DATi) (i = 0 to 5)

PMC0 Receive Data Store Register i (i = 0 to 5)



Symbol	Address	After Reset
PMC0DAT0	D08Ch	00h
PMC0DAT1	D08Dh	00h
PMC0DAT2	D08Eh	00h
PMC0DAT3	D08Fh	00h
PMC0DAT4	D090h	00h
PMC0DAT5	D091h	00h

Function	RW
Received data is stored.	RO

When detecting data 0 or data 1, the result is stored bit by bit according to the PMC0RBIT register. The data is stored into the PMC0DATi register starting from the bit 0 in the PMC0DAT0 register. Table 22.7 lists Order of Storing Data.

When the data exceeds 48 bits, the PMC0DATi register is sequentially overwritten from the first bit in the PMC0DAT0 register. Also, after the DRFLG bit in the PMCiSTS register changes from 0 to 1 (next frame reception starts), the PMC0DATi register is sequentially overwritten from the first bit in the PMC0DAT0 register.

Header and special data are not stored.

Table 22.7 Order of Storing Data

Register	b7	b6	b5	b4	b3	b2	b1	b0
PMC0DAT0	8	7	6	5	4	3	2	1
PMC0DAT1	16	15	14	13	12	11	10	9
PMC0DAT2	24	23	22	21	20	19	18	17
PMC0DAT3	32	31	30	29	28	27	26	25
PMC0DAT4	40	39	38	37	36	35	34	33
PMC0DAT5	48	47	46	45	44	43	42	41

22.2.13 PMC0 Compare Control Register (PMC0CPC)

PMC0 Compare Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X		X			

Symbol	Address	After Reset
PMC0CPC	01F6h	XXX0 X000b

Bit Symbol	Bit Name	Function	RW
CPN0	Compare bit specified bit	When the setting value is n, bits n to 0 are compared.	RW
CPN1			RW
CPN2			RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value.		—
CPEN	Compare enable bit	0: Compare disabled 1: Compare enabled	RW
— (b7-b5)	No register bits. If necessary, set to 0. Read as undefined value.		—

CPN2-CPN0 (Compare Bit Specified Bit) (b2-b0)

These bits are valid when the CPEN bit is 1 (compare enabled).
When the setting value of bits CPN2 to CPN0 is n, bits n to 0 are compared.
e.g.1 Setting value = 0
Bit 0 in the PMC0CPD register and bit 0 in the PMC0DAT0 register are compared.
e.g.2 Setting value = 7
Bits 7 to 0 in the PMC0CPD register and bits 7 to 0 in the PMC0DAT0 register are compared.

CPEN (Compare Enable Bit) (b4)

When the CPEN bit is 1 (compare enabled), contents of registers PMC0CPD and PMC0DAT0 are compared.
The contents are matched, the CPFLG bit in the PMC0STS register becomes 1 (compare match).

22.2.14 PMC0 Compare Data Register (PMC0CPD)

PMC0 Compare Data Register

b7	b0	Symbol	Address	After Reset
		PMC0CPD	01F7h	00h

Function	RW
Compare data	RW

This register is valid when the CPEN bit in the PMC0CPC register is 1 (compare enabled).
Bits to be compared are selected by bits CPN2 to CPN0 in the PMC0CPC register.

22.3 Operations

22.3.1 Common Operations in Multiple Modes

22.3.1.1 Count Source

Clock source and divisor of the count source can be selected by bits CSRC1 to CSRC0 and bits CDIV1 to CDIV0 in the PMCiCON3 register (Refer to Figure 22.3 “Remote Control Signal Receiver Block Diagram (3/3) (PMCi Count Source)”).

When using fC, set the PM25 bit in the PM2 register to 1 (peripheral clock fC provided). Refer to 8. “Clock Generator” for details of fC.

When using timer B1 or B2 underflow, the internal signal of a timer B1 or B2 is inverted every time the timer B1 or B2 underflows. This internal signal is the count source. One cycle of the count source consists of two timer B1 or B2 underflow cycles. Figure 22.4 shows Clock Source When Selecting Timer B1 or B2 Underflow. Use the timer B1 or B2 in timer mode. Refer to 18. “Timer B” for details.

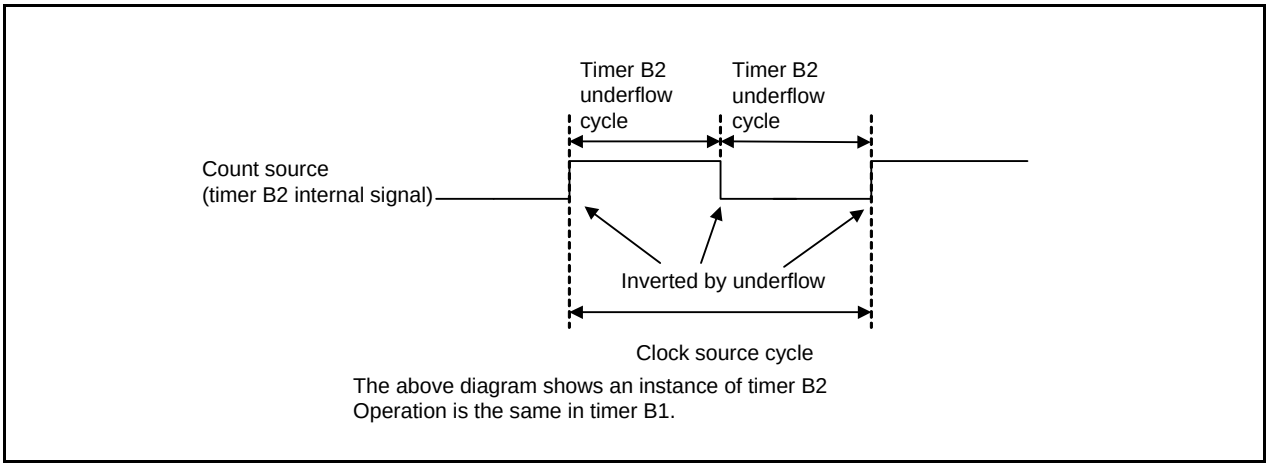


Figure 22.4 Clock Source When Selecting Timer B1 or B2 Underflow

To use the same count source in PMC0 and PMC1, set bits CSRC1 to CSRC0 in the PMC0CON3 register to 00b (same count source as PMC1), and bits CDIV1 to CDIV0 in the PMC0CON3 register to 00b (no division).

22.3.1.2 PMCi Input

The following can be selected in PMCi input (Refer to Figure 22.2 “Remote Control Signal Receiver Block Diagram (2/3) (PMCi Input)”).

- Input pin
- Input polarity
- Digital filter

A pin to which the PMCi signal is input is selected by bits PSEL1 to PSEL0 in the PMCiCON2 register.

Input polarity of the PMCi pin can be inverted. Whether to invert or not can be selected by the SINV bit in the PMCiCON0 register.

If the signal input to the PMCi pin holds the same level four sequential cycles when the FIL bit in the PMCiCON0 register is 1 (digital filter enabled), that level is transferred to internal circuit. Sampling clock of the digital filter is the count source.

Input to the PMCi pin is transferred to the internal circuit in synchronization with the count source. Internal processing causes delay. Figure 22.5 shows PMCi Input Delay.

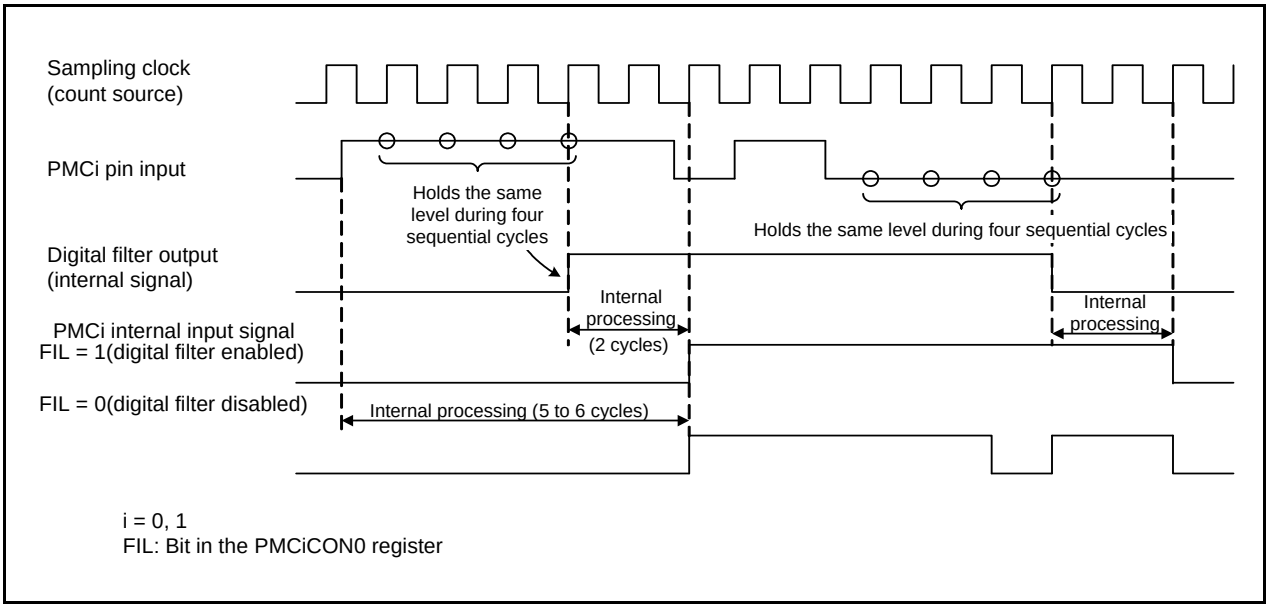


Figure 22.5 PMCi Input Delay

22.3.2 Pattern Match Mode (PMC0 and PMC1 Operate Individually)

Pattern match mode determines whether external pulse matches specified pattern. Header, data 0, and data 1 patterns can be measured in PMC0 and PMC1 separately.
Table 22.8 lists Specifications in Pattern Match Mode (Individual Operation), Table 22.9 and Table 22.10 list registers and setting values in pattern match mode (individual operation), Figure 22.6 shows Difference of Operations in Receive Modes (Pattern Match Mode), and Figure 22.7 shows Flag Operation Example.

Table 22.8 Specifications in Pattern Match Mode (Individual Operation)

Item		Contents	
		PMC0 Circuit	PMC1 Circuit
Count sources	Clock sources	One of the following: • fC • f1 • Timer B2 underflow • Count source of PMC1	One of the following: • fC • f1 • Timer B1 underflow • Timer B2 underflow
	Division	No division, divided-by-8, divided-by-32, or divided-by-64	
Count operation		Increment	
Detect patterns		• Header or special data • Data 0 • Data 1	• Header • Data 0 • Data 1
Receive buffer		6 bytes (48 bits)	None
Interrupt request generation timing		• Receive error • Completion of data reception • Header match • Data 0/1 match • Special data match • Receive buffer full • Compare match	• Receive error • Completion of data reception • Header match • Data 0/1 match
Selectable functions		• Input signal inversion • Digital filter	

Table 22.9 Registers and Setting Values in Pattern Match Mode (Individual Operation) (1/2)

Register	Bit	Function	
		PMC0	PMC1
PMCiCON0	EN	1	1
	SINV	Select input signal polarity	Select input signal polarity
	FIL	Select filter enabled or disabled	Select filter enabled or disabled
	EHOLD	Select receive error holding period	-
	HDEN	Select header enabled or disabled	Select header enabled or disabled
	SDEN	Select special data enabled or disabled	-
	DRINT0	Select receive interrupt generating condition	-
	DRINT1		
PMCiCON1	TYP0	Select measuring object	Select measuring object
	TYP1		
	CSS	0	-
	EXSDEN	0	-
	EXHDEN	0	-
PMCiCON2	ENFLG	Flag indicating PMCi operated/ stopped	Flag indicating PMCi operated/ stopped
	INFLG	Input signal flag	Input signal flag
	CEFLG	Not used	Not used
	CEINT	0	0
	PSEL0	01b	Select input pin
	PSEL1		
PMCiCON3	CRE	0	0
	CFR	0	0
	CST	0	0
	PD	0	0
	CSRC0	Select clock source	Select clock source
	CSRC1		
	CDIV0	Select count source divisor	Select count source divisor
	CDIV1		
PMCiSTS	CPFLG	Compare match flag	-
	REFLG	Receive error flag	Receive error flag
	DRFLG	Data receiving flag	Data receiving flag
	BFULFLG	Receive buffer full flag	-
	PTHDFLG	Header pattern match flag	Header pattern match flag
	PTD0FLG	Data 0 pattern match flag	Data 0 pattern match flag
	PTD1FLG	Data 1 pattern match flag	Data 1 pattern match flag
	SDFLG	Special pattern match flag	-

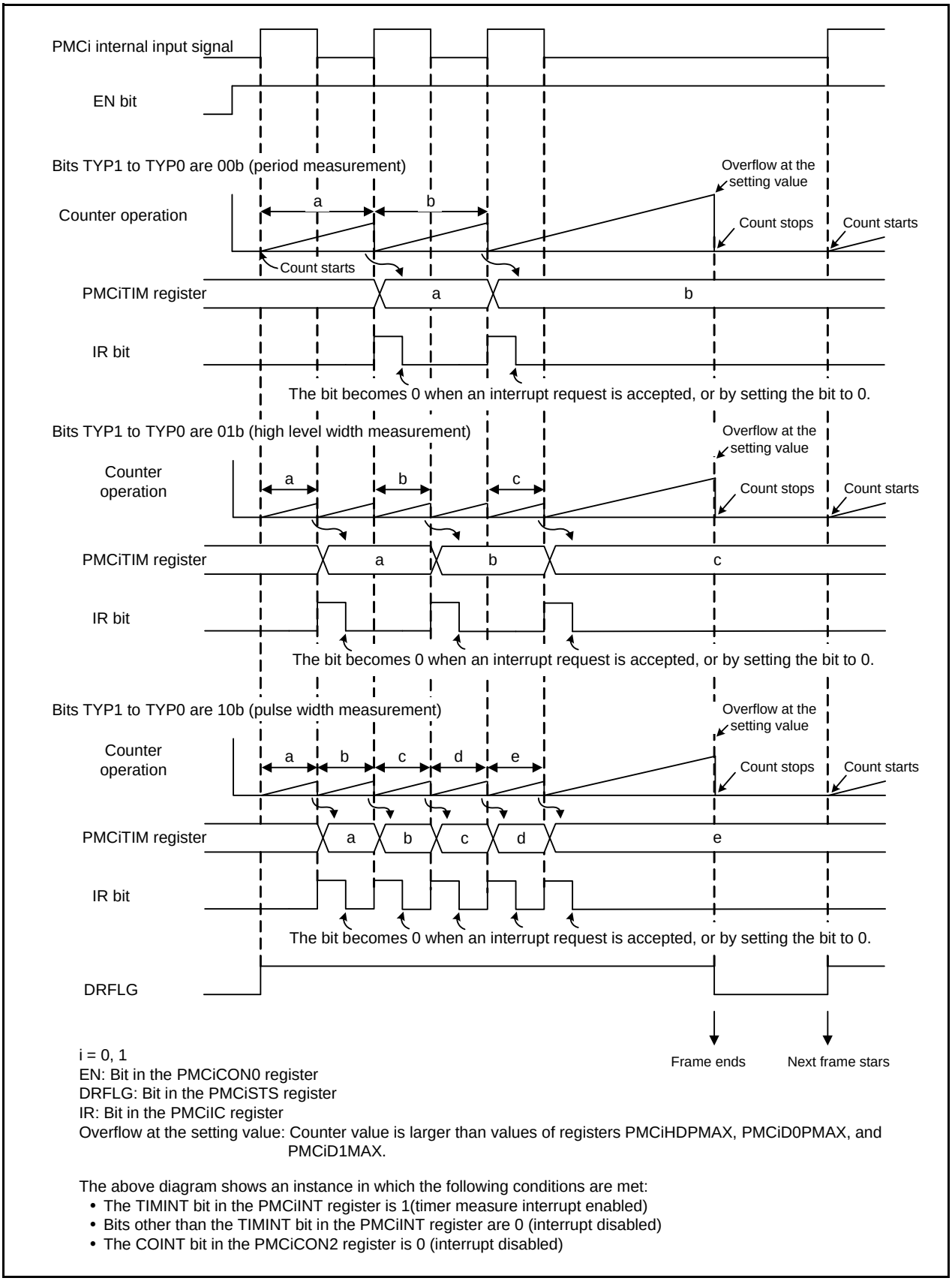
i = 0, 1

-: No register bits in PMC1

Table 22.10 Registers and Setting Values in Pattern Match Mode (Individual Operation) (2/2)

Register	Bit	Function	
		PMC0	PMC1
PMCiINT	CPINT	Set to 1 when using compare match flag interrupt	-
	REINT	Set to 1 when using receive error flag interrupt	Set to 1 when using receive error flag interrupt
	DRINT	Set to 1 when using data reception complete interrupt	Set to 1 when using data reception complete interrupt
	BFULINT	Set to 1 when using receive buffer full flag interrupt	-
	PTHDINT	Set to 1 when using header match flag interrupt	Set to 1 when using header match flag interrupt
	PTDINT	Set to 1 when using data 0/1 match flag interrupt	Set to 1 when using data 0/1 match flag interrupt
	TIMINT	Set to 1 when using timer measure interrupt	Set to 1 when using timer measure interrupt
	SDINT	Set to 1 when using special data match flag interrupt	-
PMCiCPC	CPN0	Select bits to be compared when using compare function	-
	CPN1		
	CPN2		
	CPEN	Set to 1 when using compare function	-
PMCiCPD	0 to 7	Set compare value when using compare function	-
PMCiHDPMIN	0 to 10	Set minimum value of header pattern	Set minimum value of header pattern
PMCiHDPMAX	0 to 10	Set maximum value of header pattern	Set maximum value of header pattern
PMCiD0PMIN	0 to 7	Set minimum value of data 0 pattern	Set minimum value of data 0 pattern
PMCiD0PMAX	0 to 7	Set maximum value of data 0 pattern	Set maximum value of data 0 pattern
PMCiD1PMIN	0 to 7	Set minimum value of data 1 pattern	Set minimum value of data 1 pattern
PMCiD1PMAX	0 to 7	Set maximum value of data 1 pattern	Set maximum value of data 1 pattern
PMCiTIM	0 to 15	Measured value of pulse period or width can be read	Measured value of pulse period or width can be read
PMCiBC	0 to 15	Counter value can be read	Counter value can be read
PMCiDAT0 to PMCiDAT5	0 to 7	Received data can be read	-
PMC0RBIT	0 to 5	Received bit count can be read	-

i = 0, 1
-: No register bit in PMC1



i = 0, 1
EN: Bit in the PMCiCON0 register
DRFLG: Bit in the PMCiSTS register
IR: Bit in the PMCiIC register
Overflow at the setting value: Counter value is larger than values of registers PMCiHDPMAX, PMCiD0PMAX, and PMCiD1MAX.

The above diagram shows an instance in which the following conditions are met:
- The TIMINT bit in the PMCiINT register is 1(timer measure interrupt enabled)
- Bits other than the TIMINT bit in the PMCiINT register are 0 (interrupt disabled)
- The COINT bit in the PMCiCON2 register is 0 (interrupt disabled)

Figure 22.6 Difference of Operations in Receive Modes (Pattern Match Mode)

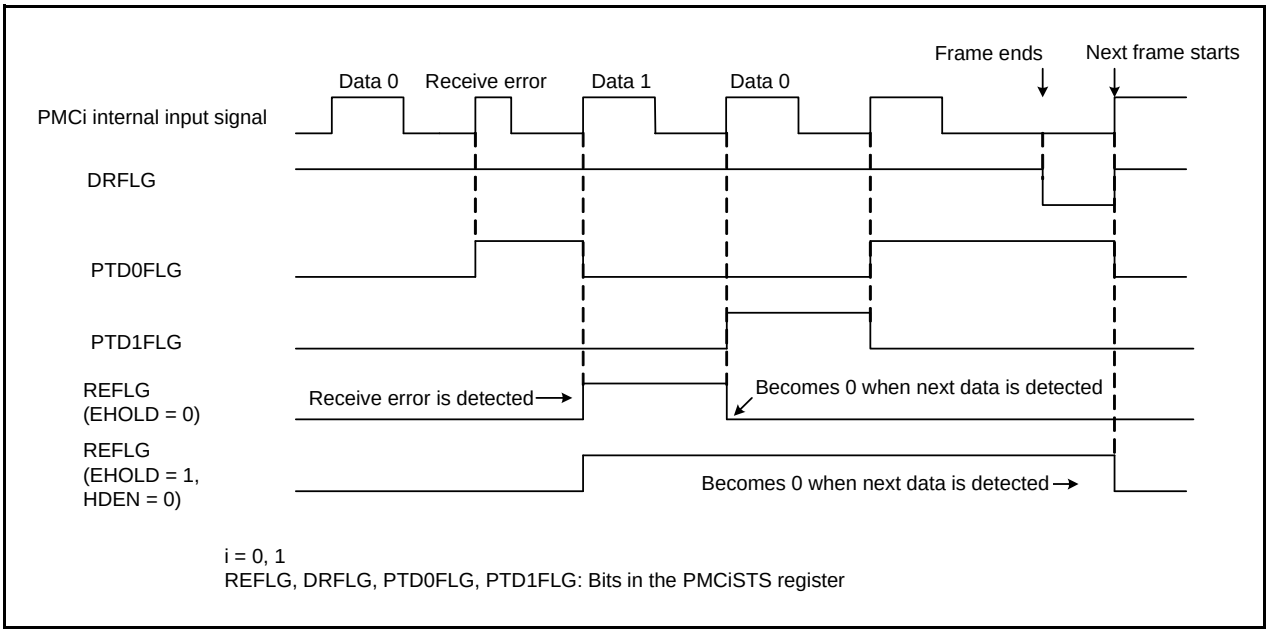


Figure 22.7 Flag Operation Example

22.3.2.1 Header Detection (PMC0, PMC1)

When the HDEN bit in the PMCiCON0 register is 1 (header enabled), the following occur by detecting data 0, data 1, or special data prior to header.

- The REFLG bit in the PMCiSTS register becomes 1 (error occurs).
- Bits PTD0FLG, PTD1FLG, and SDFLG in the PMCiSTS register remain unchanged.
- Registers PMCDAT0 to PMCDAT5 remain unchanged.

When detecting header in PMC0, set the SDEN bit in the PMC0CON0 register to 0 (special data disabled).

22.3.2.2 Special Data Detection (PMC0)

When the SDEN bit in the PMC0COM0 register is 1 (special data enabled), special data can be detected. When detecting the special data, set the HDEN bit in the PMC0CON0 register to 0 (header disabled).

22.3.2.3 Receive Data Buffer (PMC0)

There is a 6-byte (48-bit) buffer for storing received data. When the data exceeds 48 bits, the buffer is sequentially overwritten from the first bit. Refer to 22.2.12 “PMC0 Receive Data Store Register i (PMC0DATi) (i = 0 to 5)” and 22.2.11 “PMC0 Receive Bit Count Register (PMC0RBIT)”.

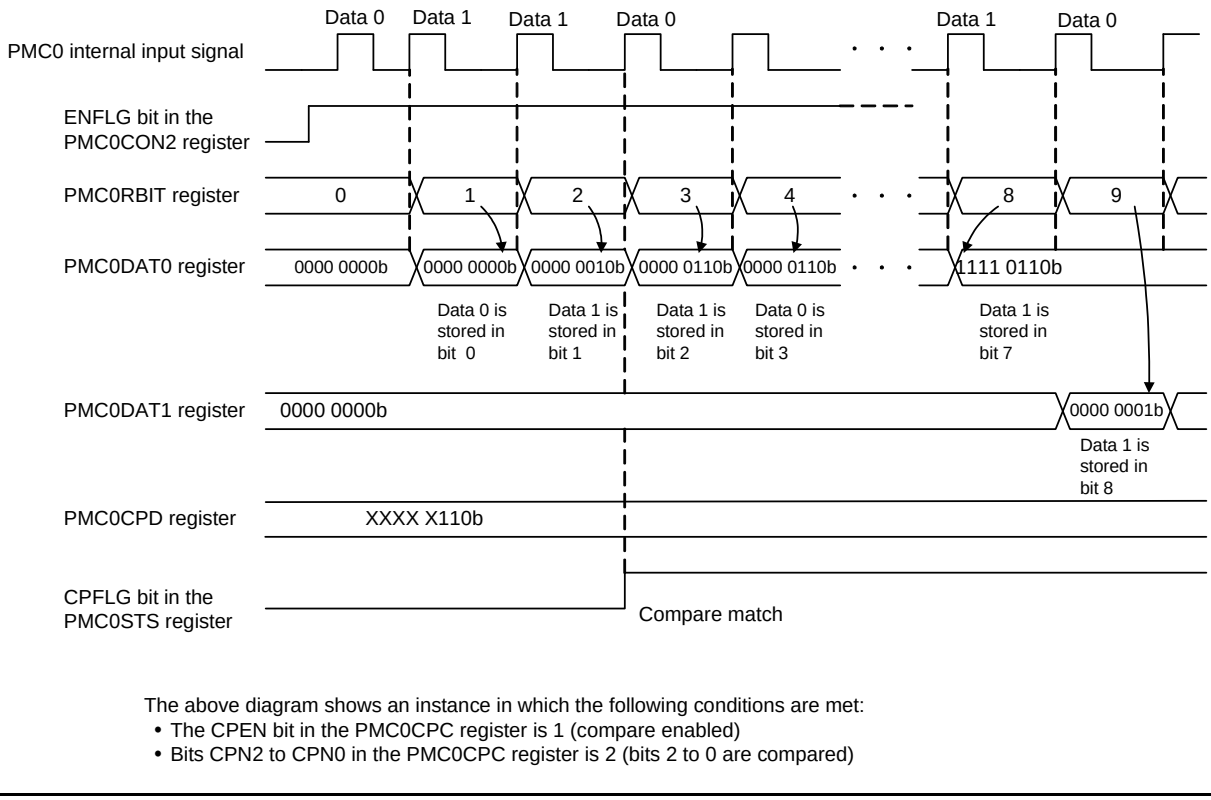
22.3.2.4 Compare Function (PMC0)

Contents of registers PMC0CPD and PMCDAT0 are compared. Reception of the specific data which is 1 to 8 bits can be detected.

When using compare function, follow the instructions below:

- The CPEN bit in the PMC0CPC register: 1 (compare enabled)
- Select bits to be compared by bits CPN2 to CPN0 in the PMC0CPC register (when setting value is n, bits n to 0 are compared. n: 0 to 7)
- Set the compare data in the PMC0CPD register

The contents which have been compared are matched, the CPFLG bit in the PMC0STS register becomes 1 (compare match).



The above diagram shows an instance in which the following conditions are met:

- The CPEN bit in the PMC0CPC register is 1 (compare enabled)
- Bits CPN2 to CPN0 in the PMC0CPC register is 2 (bits 2 to 0 are compared)

Figure 22.8 Receive Buffer and Compare Function

22.3.3 Pattern Match Mode (Connected Operation of PMC0 and PMC1)

PMC0 and PMC1 is connected and one remote control signal can be received. In connected operation, data 0 and data 1 are detected in PMC1. Whether to detect header and special data in PMC0 or PMC 1 can be selected. Select count source and remote control signal input pins in PMC1.
Table 22.11 lists Specifications in Pattern Match Mode (Connected Operation) and Figure 22.1 and Figure 22.2 shows registers and setting values in pattern match mode (connected operation).

Table 22.11 Specifications in Pattern Match Mode (Connected Operation)

Item		Content	
		PMC0 Circuit	PMC1 Circuit
Count sources	Clock sources	Count source of PMC1	One of the following: • fC • f1 • Timer B1 underflow • Timer B2 underflow
	Division	No division	No division, divided-by-8, divided-by-32, or divided-by-64
Count operation		Increment	
Detect patterns		• Header • Data 0 • Data 1 • Special data	• Header • Special data
Receive buffer		6 bytes (48 bits)	None
Interrupt request generation timing		• Receive error • Completion of data reception • Header match • Data 0/1 match • Special data match • Receive buffer full • Compare match	Not used
Selectable functions		• Input signal inversion • Digital filter	

Table 22.12 Registers and Setting Values in Pattern Match Mode (Connected Operation) (1/2)

Register	Bit	Function	
		PMC0	PMC1
PMCiCON0	EN	1. Refer to 22.3.3.1 “Setting Procedure”	1. Refer to 22.3.3.1 “Setting Procedure”
	SINV	0	Select input signal polarity
	FIL	0	Select filter enabled/disabled
	EHOLD	Select receive error holding period	-
	HDEN	Select header enabled/ disabled	1
	SDEN	Select special data enabled/ disabled	-
	DRINT0	Select receive interrupt generating condition	-
	DRINT1		
PMCiCON1	TYP0	Select measuring object	Select measuring object
	TYP1		
	CSS	0	-
	EXSDEN	Select block in which header and special pattern is detected	-
	EXHDEN		
PMCiCON2	ENFLG	Flag indicating PMCi operated/ stopped	Flag indicating PMCi operated/ stopped
	INFLG	Input signal flag	Not used
	CEFLG	Not used	Not used
	CEINT	0	0
	PSEL0	00b	Select input pin
	PSEL1		
PMCiCON3	CRE	0	0
	CFR	0	0
	CST	0	0
	PD	0	0
	CSRC0	00b	Select clock source
	CSRC1		
	CDIV0	00b	Select count source divisor
	CDIV1		
PMCiSTS	CPFLG	Compare match flag	-
	REFLG	Receive error flag	Not used
	DRFLG	Data receiving flag	Not used
	BFULFLG	Receive buffer full flag	-
	PTHDFLG	Header pattern match flag	Not used
	PTD0FLG	Data 0 pattern match flag	Not used
	PTD1FLG	Data 1 pattern match flag	Not used
	SDFLG	Special pattern match flag	-

i = 0, 1

-: No register bit in PMC1

Table 22.13 Registers and Setting Values in Pattern Match Mode (Connected Operation) (2/2)

Register	Bit	Function	
		PMC0	PMC1
PMCiINT	CPINT	Set to 1 when using compare match flag interrupt	-
	REINT	Set to 1 when using receive error flag interrupt	0
	DRINT	Set to 1 when using data reception complete interrupt	0
	BFULINT	Set to 1 when using receive buffer full flag interrupt	-
	PTHDINT	Set to 1 when using header match flag interrupt	0
	PTDINT	Set to 1 when using data 0/1 match flag interrupt	0
	TIMINT	Set to 1 when using timer measure interrupt	0
	SDINT	Set to 1 when using special data match flag interrupt	-
PMCiCPC	CPN0	Select bits to be compared when using compare function	-
	CPN1		
	CPN2		
	CPEN	Set to 1 when using compare function	-
PMCiCPD	0 to 7	Set compare value when using compare function	-
PMCiHDPMIN	0 to 10	Set minimum value of header pattern or special data pattern	Set minimum value of header pattern or special data pattern
PMCiHDPMAX	0 to 10	Set maximum value of header pattern or special data pattern	Set maximum value of header pattern or special data pattern
PMCiD0PMIN	0 to 7	Set minimum value of data 0 pattern	00h
PMCiD0PMAX	0 to 7	Set maximum value of data 0 pattern	00h
PMCiD1PMIN	0 to 7	Set minimum value of data 1 pattern	00h
PMCiD1PMAX	0 to 7	Set maximum value of data 1 pattern	00h
PMCiTIM	0 to 15	Measured value of pulse period or width can be read	Not used
PMCiBC	0 to 15	Counter value can be read	Not used
PMCiDAT0 to PMCiDAT5	0 to 7	Received data can be read	-
PMC0RBIT	0 to 5	Received bit count can be read	-

i = 0, 1
-: No register bit in PMC1

22.3.3.1 Setting Procedure

To start or stop counting, follow procedures below:
(1) Set the EN bit in the PMC0CON0 register to 1 (0 to stop).
(2) Set the EN bit in the PMC1CON0 register to 1 (1 to stop).
(3) Wait for two cycles of count source.
(4) Confirm that the ENFLG bit in the PMC0CON2 register is 1 (0 to stop). (The ENFLG bit in the PMC1CON2 register is disabled)

22.3.3.2 Header and Special Data Detection

Header and special data can be detected. Table 22.14 lists Selection of Header and Special Data Detecting Block.

Table 22.14 Selection of Header and Special Data Detecting Block

Detected Item		Bit Setting			
PMC0	PMC1	PMC0CON0 register		PMC0CON1 register	
		HDEN bit	SDEN bit	EXHDEN bit	EXSDEN bit
-	Header	1	0	1	0
-	Special data	0	1	0	1
Header	Special data	1	1	0	1
Special data	Header	1	1	1	0

-: Neither header nor special data is detected
Note:
1. Do not set values not listed above.

When header is valid, the following occur by detecting data 0, data 1, or special data prior to header.
- The REFLG bit in the PMCiSTS register becomes 1 (error occurs).
- Bits PTD0FLG, PTD1FLG, and SDFLG in the PMCiSTS register remain unchanged.
- Registers PMCDAT0 to PMCDAT5 remain unchanged.

22.3.3.3 Status Flag and Interrupt

When connecting PMC0 and PMC1, use flags and interrupt control in PMC0. The object bits are as follows:
Each bit in the PMC0STS register
Each bit in the PMC0INT register
INFLG bit in the PMC0CON2 register
Even when detecting header or special data in PMC1, the result including those data can be detected in the above registers.

22.3.3.4 Receive Data Buffer (PMC0)

There is a 6-byte (48-bit) buffer for storing received data. When the data exceeds 48 bits, the buffer is sequentially overwritten from the first bit. Refer to 22.2.12 “PMC0 Receive Data Store Register i (PMC0DATi) (i = 0 to 5)” and 22.2.11 “PMC0 Receive Bit Count Register (PMC0RBIT)”.

22.3.3.5 Compare Function (PMC0)

Contents of registers PMC0CPD and PMCDAT0 are compared. Reception of the specific data which is 1 to 8 bits can be detected.

When using compare function, follow the instructions below:

- The CPEN bit in the PMC0CPC register: 1 (compare enabled)
- Select bits to be compared by bits CPN2 to CPN0 in the PMC0CPC register (when setting value is n, bits n to 0 are compared. n: 0 to 7)
- Set the compare data in the PMC0CPD register

The contents which have been compared are matched, the CPFLG bit in the PMC0STS register becomes 1 (compare match).

22.3.4 Input Capture Mode (PMC0 and PMC1 Operate Individually)

Input capture mode measures width or period of external pulse. PMC0 and PMC1 can be measured individually.

Table 22.15 lists Specifications in Input Capture Mode (Individual Operation), Table 22.16 and Table 22.17 list registers and setting values in input capture mode (individual operation), and Figure 22.9 shows Difference of Operations in Receive Modes (Input Capture Mode).

Table 22.15 Specifications in Input Capture Mode (Individual Operation)

Item		Content	
		PMC0 Circuit	PMC1 Circuit
Count sources	Clock sources	One of the following: • fC • f1 • Timer B2 underflow • Count source of PMC1	One of the following: • fC • f1 • Timer B1 underflow • Timer B2 underflow
	Division	No division, divided-by-8, divided-by-32, or divided-by-64	
Count operation		Increment	
Measurement items		One of the following: Pulse period (between rising edge and rising edge) Pulse period (between falling edge and falling edge) Pulse width (both high level and low level)	
Interrupt request generation timing		• Timer measurement • Counter overflow	
Selectable functions		• Input signal inversion • Digital filter	

Table 22.16 Registers and Setting Values in Input Capture Mode (Individual Operation) (1/2)

Register	Bit	Function	
		PMC0	PMC1
PMCiCON0	EN	1	1
	SINV	Select input signal polarity	Select input signal polarity
	FIL	Select filter enabled or disabled	Select filter enabled or disabled
	EHOLD	0	-
	HDEN	0	0
	SDEN	0	-
	DRINT0	00b	-
	DRINT1		
PMCiCON1	TYP0	Select measuring object	Select measuring object
	TYP1		
	CSS	0	-
	EXSDEN	0	-
	EXHDEN	0	-
PMCiCON2	ENFLG	Flag indicating PMCi operated/ stopped	Flag indicating PMCi operated/ stopped
	INFLG	Input signal flag	Input signal flag
	CEFLG	Counter overflow flag	Counter overflow flag
	CEINT	Set to 1 when using counter overflow interrupt	Set to 1 when using counter overflow interrupt
	PSEL0	01b	10b
	PSEL1		
PMCiCON3	CRE	1	1
	CFR	1	1
	CST	1	1
	PD	1	1
	CSRC0	Select clock source	Select clock source
	CSRC1		
	CDIV0	Select count source divisor	Select count source divisor
	CDIV1		
PMCiSTS	CPFLG	Not used (read as undefined value)	-
	REFLG	Not used (read as undefined value)	Not used (read as undefined value)
	DRFLG	Not used (read as undefined value)	Not used (read as undefined value)
	BFULFLG	Not used (read as undefined value)	-
	PTHDFLG	Not used (read as undefined value)	Not used (read as undefined value)
	PTD0FLG	Not used (read as undefined value)	Not used (read as undefined value)
	PTD1FLG	Not used (read as undefined value)	Not used (read as undefined value)
	SDFLG	Not used (read as undefined value)	-

i = 0, 1

-: No register bits in PMC1

Table 22.17 Registers and Setting Values in Input Capture Mode (Individual Operation) (2/2)

Register	Bit	Function	
		PMC0	PMC1
PMCiINT	CPINT	0	-
	REINT	0	0
	DRINT	0	0
	BFULINT	0	-
	PTHDINT	0	0
	PTDINT	0	0
	TIMINT	Set to 1 when using timer measure interrupt	Set to 1 when using timer measure interrupt
	SDINT	0	-
PMCiCPC	CPN0	000b	-
	CPN1		
	CPN2		
	CPEN	0	-
PMCiCPD	0 to 7	00h	-
PMCiHDPMIN	0 to 10	0000h	0000h
PMCiHDPMAX	0 to 10	0000h	0000h
PMCiD0PMIN	0 to 7	00h	00h
PMCiD0PMAX	0 to 7	00h	00h
PMCiD1PMIN	0 to 7	00h	00h
PMCiD1PMAX	0 to 7	00h	00h
PMCiTIM	0 to 15	Measured value of pulse period or width can be read	Measured value of pulse period or width can be read
PMCiBC	0 to 15	Counter value can be read	Counter value can be read
PMCiDAT0 to PMCiDAT5	0 to 7	Not used	Not used
PMC0RBIT	0 to 5	Not used	Not used

i = 0, 1
-: No register bit in PMC1

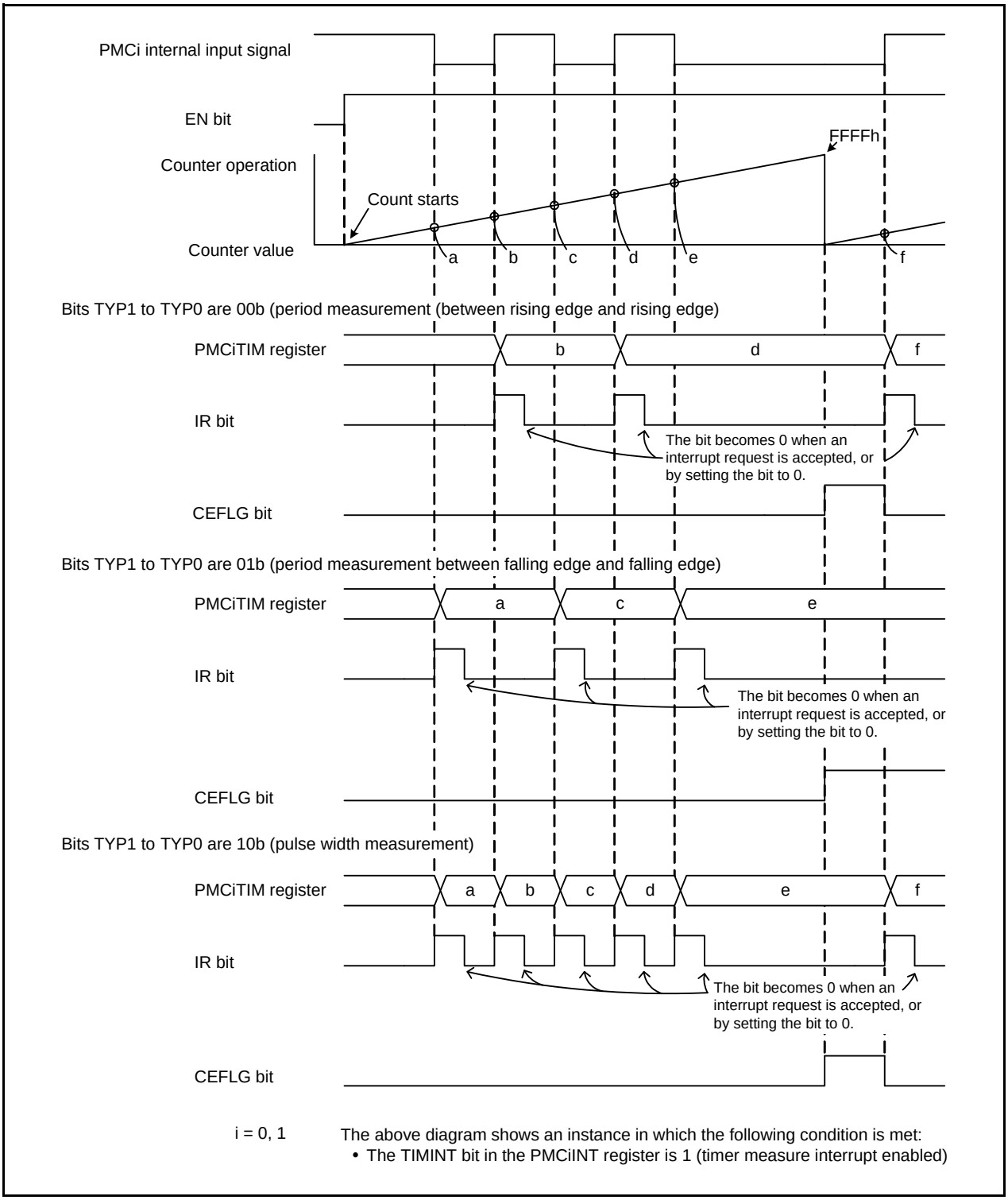


Figure 22.9 Difference of Operations in Receive Modes (Input Capture Mode)

22.3.4.1 Count Operation

In input capture mode, the counter counts from 0000h to FFFFh, and then return to 0000h to continue counting.

When the counter becomes 0000h after FFFFh, the CEFLG bit in the PMCiCON2 register becomes 1 (counter overflow) and holds 1 until the next measurement timing.

22.3.5 Input Capture Mode (Simultaneous Count Operation of PMC0 and PMC1)

Table 22.18 lists Specifications in Input Capture Mode (Simultaneous Count Operation) and Table 22.19 and Table 22.20 list registers and setting values in input capture mode (simultaneous count operation).

Table 22.18 Specifications in Input Capture Mode (Simultaneous Count Operation)

Item		Content	
		PMC0 Circuit	PMC1 Circuit
Count sources	Clock sources	Count source of PMC1	One of the following: • fC • f1 • Timer B1 underflow • Timer B2 underflow
	Division	No division	No division, divided-by-8, divided-by-32, or divided-by-64
Count operation		Increment	
Measurement items		One of the following: Pulse period (between rising edge and rising edge) Pulse period (between falling edge and falling edge) Pulse width (both high level and low level)	
Interrupt request generation timing		• Timer measurement • Counter overflow	
Selectable functions		• Input signal inversion • Digital filter	

Table 22.19 Registers and Setting Values in Input Capture Mode (Simultaneous Count Operation) (1/2)

Register	Bit	Function	
		PMC0	PMC1
PMCiCON0	EN	1. (Refer to 22.3.5.1 “Setting Procedure”)	1. (Refer to 22.3.5.1 “Setting Procedure”)
	SINV	Select input signal polarity	Select input signal polarity
	FIL	Select filter enabled/disabled	Select filter enabled/disabled
	EHOLD	0	-
	HDEN	0	0
	SDEN	0	-
	DRINT0	00b	-
	DRINT1		
PMCiCON1	TYP0	Select measuring object	Select measuring object
	TYP1		
	CSS	1	-
	EXSDEN	0	-
	EXHDEN	0	-
PMCiCON2	ENFLG	Flag indicating PMCi operated/ stopped	Flag indicating PMCi operated/ stopped
	INFLG	Input signal flag	Input signal flag
	CEFLG	Counter overflow flag	Counter overflow flag
	CEINT	Set to 1 when using counter overflow interrupt	Set to 1 when using counter overflow interrupt
	PSEL0	01b	10b
	PSEL1		
PMCiCON3	CRE	1	1
	CFR	1	1
	CST	1	1
	PD	1	1
	CSRC0	00b	Select clock source
	CSRC1		
	CDIV0	00b	Select count source divisor
	CDIV1		
PMCiSTS	CPFLG	Not used (read as undefined value)	-
	REFLG	Not used (read as undefined value)	Not used (read as undefined value)
	DRFLG	Not used (read as undefined value)	Not used (read as undefined value)
	BFULFLG	Not used (read as undefined value)	-
	PTHDFLG	Not used (read as undefined value)	Not used (read as undefined value)
	PTD0FLG	Not used (read as undefined value)	Not used (read as undefined value)
	PTD1FLG	Not used (read as undefined value)	Not used (read as undefined value)
	SDFLG	Not used (read as undefined value)	-

i = 0, 1
-: No register bit in PMC1

Table 22.20 Registers and Setting Values in Input Capture Mode (Simultaneous Count Operation) (2/2)

Register	Bit	Function	
		PMC0	PMC1
PMCiINT	CPINT	0	-
	REINT	0	0
	DRINT	0	0
	BFULINT	0	-
	PTHDINT	0	0
	PTDINT	0	0
	TIMINT	Set to 1 when using timer measure interrupt	Set to 1 when using timer measure interrupt
	SDINT	0	-
PMCiCPC	CPN0	000b	-
	CPN1		
	CPN2		
	CPEN	0	-
PMCiCPD	0 to 7	00h	-
PMCiHDPMIN	0 to 10	0000h	0000h
PMCiHDPMAX	0 to 10	0000h	0000h
PMCiD0PMIN	0 to 7	00h	00h
PMCiD0PMAX	0 to 7	00h	00h
PMCiD1PMIN	0 to 7	00h	00h
PMCiD1PMAX	0 to 7	00h	00h
PMCiTIM	0 to 15	Measured value of pulse period or width can be read	Measured value of pulse period or width can be read
PMCiBC	0 to 15	Counter value can be read	Counter value can be read
PMCiDAT0 to PMCiDAT5	0 to 7	Not used	Not used
PMC0RBIT	0 to 5	Not used	Not used

i = 0, 1
-: No register bit in PMC1

22.3.5.1 Setting Procedure

To start or stop counting, follow procedures below:
(1) Set the EN bit in the PMC0CON0 register to 1 (0 to stop).
(2) Set the EN bit in the PMC1CON0 register to 1 (1 to stop).
(3) Wait for two cycles of count source.
(4) Confirm that the ENFLG bit in the PMC0CON2 register is 1 (0 to stop). (The ENFLG bit in the PMC1CON2 register is disabled)

22.3.5.2 Count Operation

In input capture mode, the counter counts from 0000h to FFFFh, and then return to 0000h to continue counting.
When the counter becomes 0000h after FFFFh, the CEFLG bit in the PMCiCON2 register becomes 1 (counter overflow) and holds 1.

22.4 Interrupt

The remote control signal receiver has remote control signal receiver 0 interrupt and remote control signal receiver 1 interrupt. The remote control signal receiver 0 interrupt and remote control signal receiver 1 interrupt are interrupts in PMC0 and PMC1 respectively.

A remote control signal receiver i interrupt request signal is generated every time the conditions are met. If the interrupt enable bit in the PMCiCON2 or PMCiINT register is 1, the IR bit in the PMCiIC register becomes 1 (interrupt request) when the corresponding interrupt request signal is generated. Table 22.21 lists Interrupt Source of Remote Control Signal Receiver i Interrupt (i = 0, 1).

Table 22.21 Interrupt Source of Remote Control Signal Receiver i Interrupt (i = 0, 1)

Mode	Interrupt Source	Interrupt Request Generating Condition	Interrupt enable bit	
			Register	Bit
Pattern match mode	Completion of data reception	Counter value is larger than values of registers PMCiHDPMAX, PMCiD0PMAX, and PMCiD1PMAX	PMCiINT	DRINT
	Header match	The measured result is within the range set by registers PMCiHDPMIN and PMCiHDPMAX (when header is enabled)	PMCiINT	PTHDINT
	Data 0/1 match	The measured result is within the range set by registers PMCiD0PMIN and PMCiD0PMAX or registers PMCiD1PMIN and PMCiD1PMAX	PMCiINT	PTDINT
	Special data match	The measured result is within the range set by registers PMCiHDPMIN and PMCiHDPMAX (when special data is enabled)	PMC0INT	SDINT
	Receive error	Input signal width is none of header, data 0, data 1, and special data Data 0 or data 1 is detected before detecting header when the HDEN bit is 1	PMCiINT	REINT
	Receive buffer full	The value of the PMC0RBIT register is 48	PMC0INT	BFULINT
	Compare match	The values of registers PMC0CPD and PMC0DAT0 are matched (only bits selected by the CPN bit in the PMC0CPC register are compared)	PMC0INT	CPINT
	Timer measurement	Measurement end edge of PMCi internal input signal	PMCiINT	TIMINT
Input capture mode	Timer measurement	Measurement end edge of PMCi internal input signal	PMCiINT	TIMINT
	Counter overflow	Counter overflow (counter value exceeds FFFFh and becomes 0000h)	PMCiCON2	CEINT

Measured result: Content of the PMCiTIM register

Figure 22.10 shows Interrupt of Remote Control Signal Receiver.

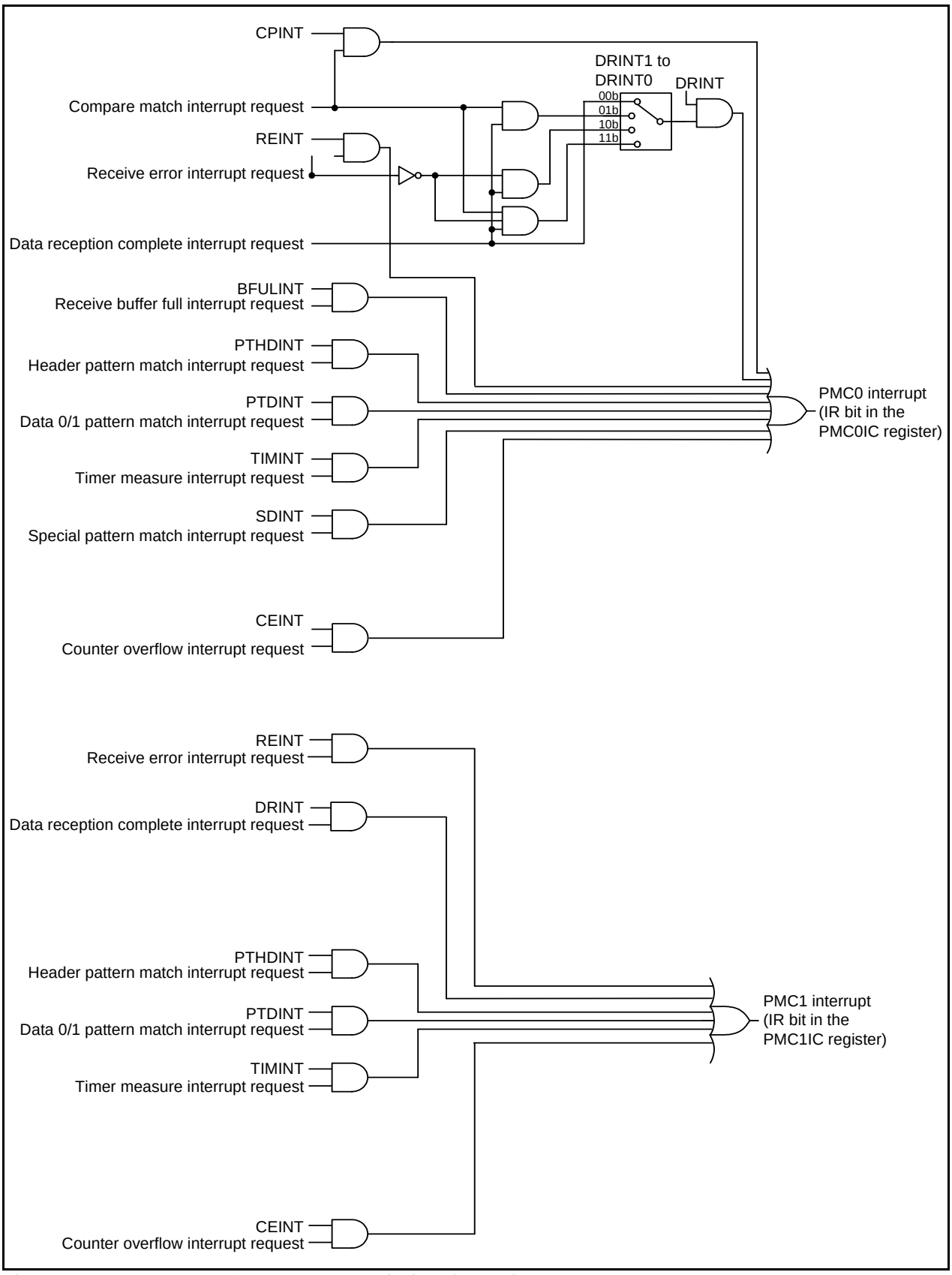


Figure 22.10 Interrupt of Remote Control Signal Receiver

Refer to 14.7 “Interrupt Control” for details of interrupt control. Table 22.22 lists Registers Associated with Interrupt of Remote Control Signal Receiver.

Table 22.22 Registers Associated with Interrupt of Remote Control Signal Receiver

Address	Register Name	Register Symbol	After Reset
0071h	UART7 Bus Collision Detection Interrupt Control Register Remote Control Signal Receiver 0 Interrupt Control Register	U7BCNIC/ PMC0IC	XXXX X000b
0072h	UART7 Transmit Interrupt Control Register Remote Control Signal Receiver 1 Interrupt Control Register	S7TIC/PMC1IC	XXXX X000b
0206h	Interrupt Source Select Register 2	IFSR2A	00h

The remote control signal receiver shares interrupt vectors or interrupt control registers with other peripheral functions. To use remote control signal receiver 0 interrupt, set the IFSR24 bit in the IFSR2A register to 1 (remote control signal receiver 0). To use remote control signal receiver 1 interrupt, set the IFSR25 bit in the IFSR2A register to 1 (remote control signal receiver 1).

The IR bit in registers PMC0IC and PMC1IC is different from another IR bit in the following respects:

- If the interrupt enable bit in the PMCiCON2 or PMCiINT register is 1, the IR bit in the PMCiIC register becomes 1 (interrupt request) when the corresponding interrupt request signal is generated.
- If multiple interrupts are enabled, IR bit becomes 1 and then remains 1 when another request source is generated.
- The IR bit does not become 0 automatically when the interrupt is accepted. Set the IR bit to 0 within interrupt routine.

22.5 Notes on Remote Control Signal Receiver

22.5.1 Start/Stop of PMCi

The EN bit in the PMCiCON0 register controls start/stop of PMCi. The ENFLG bit in the PMCiCON2 register indicates that the operation starts or stops.
The PMCi circuit starts operating by setting the EN bit to 1 (operation starts) and the ENFLG bit becomes 1. It takes up to two cycles of the count source until the ENFLG bit becomes 1 after setting the EN bit to 1. During this period, do not access registers associated with PMCi (registers listed in Table 22.3 and Table 22.4 “register structure (PMCi circuit)”) excluding the ENFLG bit.
When the EN bit is set to 0 (operation stops), PMCi circuit stops operating and the ENFLG bit becomes 0 (operation stops). It takes up to one cycle of the count source until the ENFLG bit becomes 0 after setting the EN bit to 0.

22.5.2 Register Reading Procedure

If reading the following registers when the data changes, undefined value may be read.
Each flag in registers PMCiCON2 and PMCiSTS
Registers PMCiTIM, PMC0DAT0 to PMC0DAT5, PMCiBC, and PMC0RBIT
Read above registers as follows to avoid reading the undefined value.

In pattern match mode

- Using interrupt
  Set the DRINT bit in the PMCiINT register to 1 (data reception complete interrupt enabled) and read the registers within PMCi interrupt routine.
- Monitoring by a program 1
  Set the DRINT bit in the PMCiINT register to 1 (data reception complete interrupt enabled) and monitor the IR bit in the PMCiIC register by a program. Read the registers when the IR bit becomes 1 (interrupt request is generated).
- Monitoring by a program 2
  (1) Monitor the DRFLG bit in the PMCiSTS register
  (2) When the DRFLG bit becomes 1, monitor the DRFLG bit until it becomes 0.
  (3) Read the necessary content of the registers when the DRFLG bit becomes 0.

In input capture mode

- Using interrupt
  Set the TIMINT bit in the PMCiINT register to 1 (timer measure interrupt enabled) and read the registers within PMCi interrupt routine.
- Monitoring by a program 1
  Set the TIMINT bit in the PMCiINT register to 1 (timer measure interrupt enabled) and monitor the IR bit in the PMCiIC register by a program. Read the registers when the IR bit becomes 1 (interrupt request is generated).

23. Serial Interface UARTi (i = 0 to 2, 5 to 7)

Note

The 80-pin package does not have pins CLK2 and $\overline{CTS2}$/$\overline{RTS2}$ for UART2. Do not use functions associated with these pins. UART6 and UART7 are not included.

23.1 Introduction

Each UARTi has a dedicated timer to generate a transmit/receive clock, so it operates independently of the others.

Table 23.1 lists Specifications of UARTi (i = 0 to 2, 5 to 7), Table 23.2 lists Specification Difference in UART0 to UART2 and UART5 to UART7, Figure 23.1 to Figure 23.3 show UARTi Block Diagram, and Figure 23.4 shows UARTi Transmit/Receive Unit Block Diagram.

Table 23.1 Specifications of UARTi (i = 0 to 2, 5 to 7)

Item	Specification
Operational mode	• Clock synchronous serial I/O mode • Clock asynchronous serial I/O mode (UART mode) • Special mode 1 (I^2C mode) • Special mode 2 The simplified I^2C-bus interface is supported. • Special mode 3 (bus collision detection function, IE mode) A 1-byte wave of the UART mode approximates 1-bit of the IEBus. • Special mode 4 (SIM mode) UART2 is available. The SIM interface is supported.

Table 23.2 Specification Difference in UART0 to UART2 and UART5 to UART7

Mode	UART0	UART1	UART2	UART5	UART6	UART7
Clock synchronous serial I/O mode	Available		Available	Available	Available	
Clock asynchronous serial I/O mode (UART mode)	Available		Available	Available	Available	
Special mode 1 (I^2C mode)	Available		Available	Available	Available	
Special mode 2	Available		Available	Available	Available	
Special mode 3 (IE mode)	Available		Available	Available	Available	
Special mode 4 (SIM mode)	Not available		Available	Not available	Not available	
Memory expansion mode or microprocessor mode	Can be used				Do not use.	

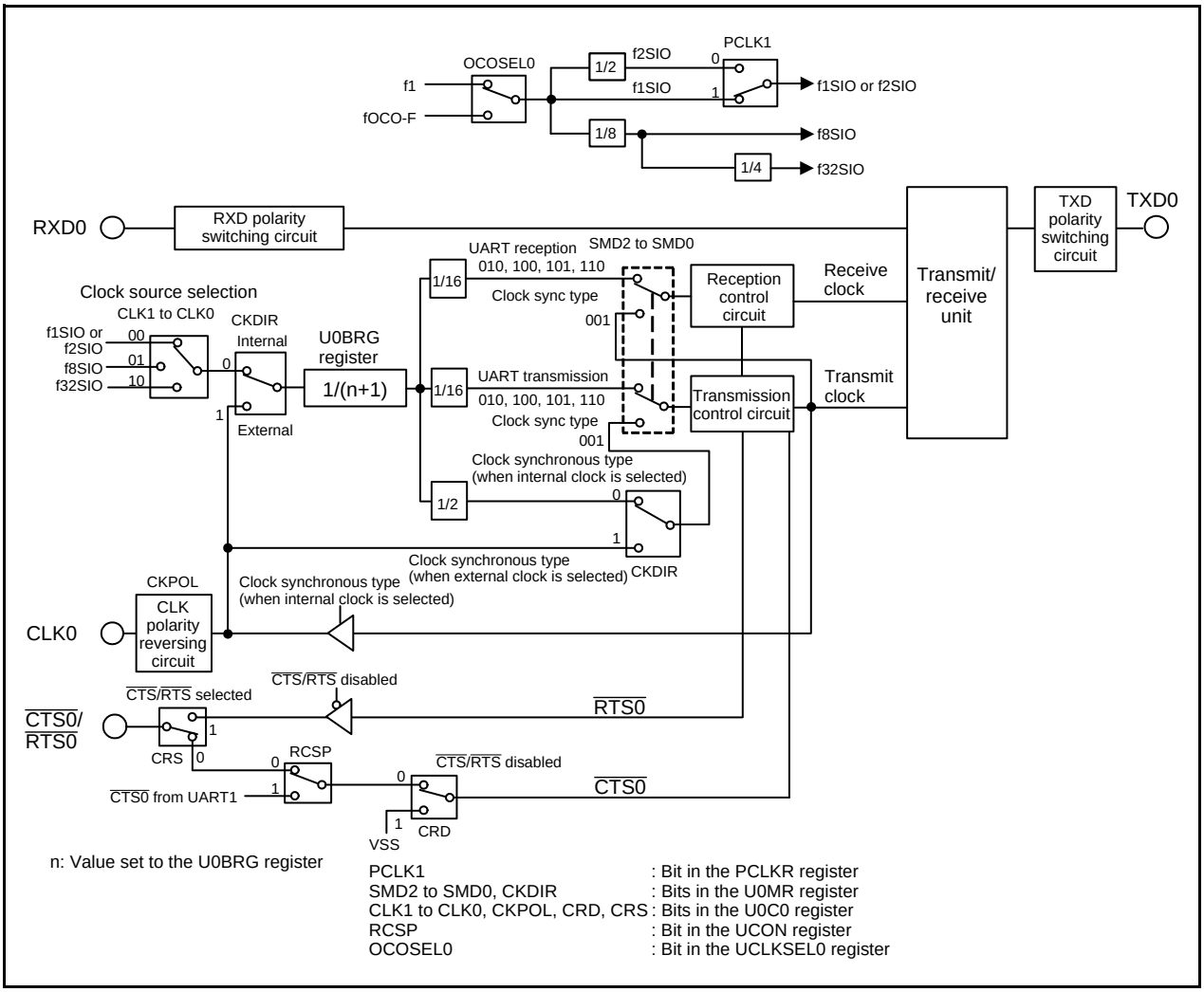


Figure 23.1 UART0 Block Diagram

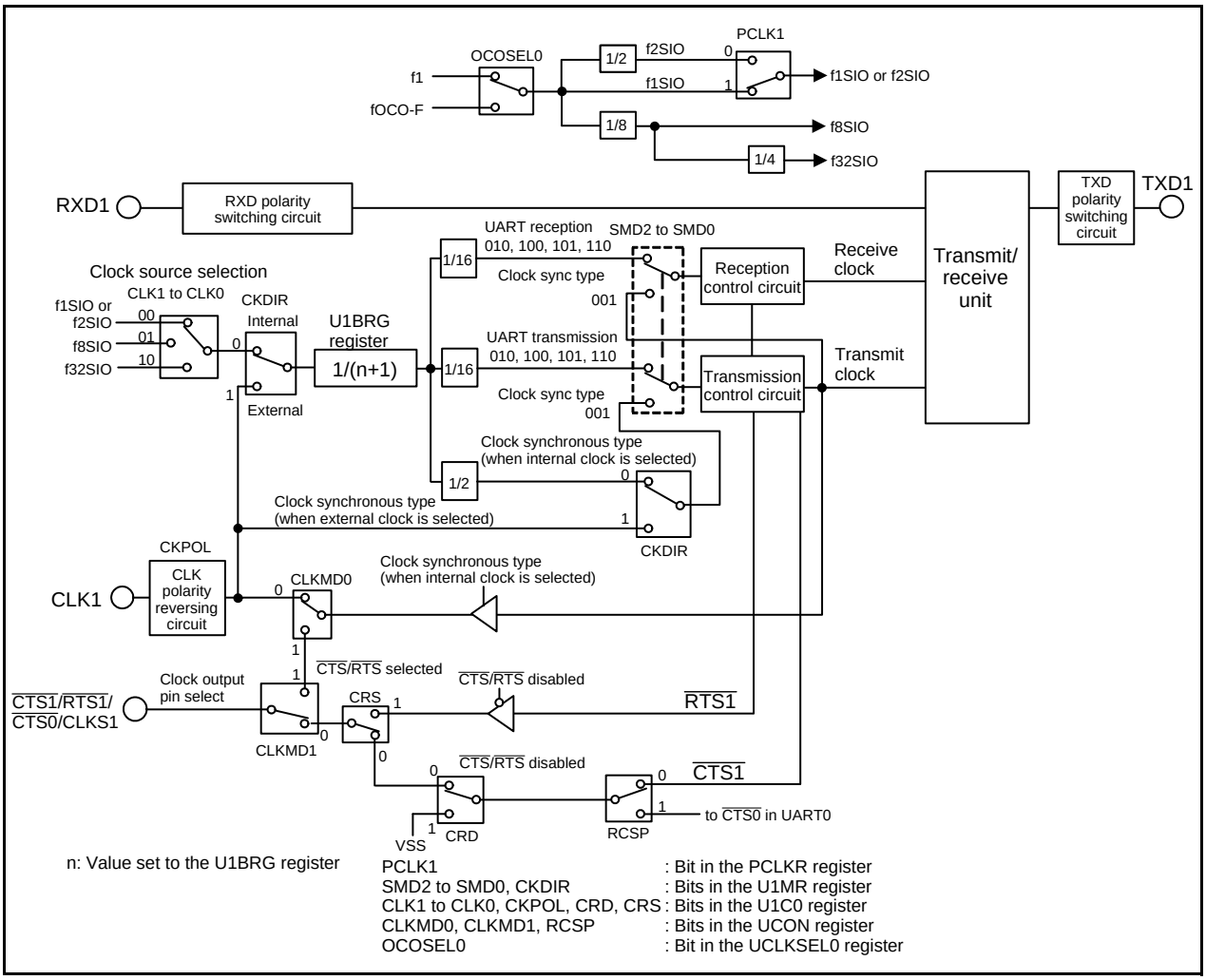
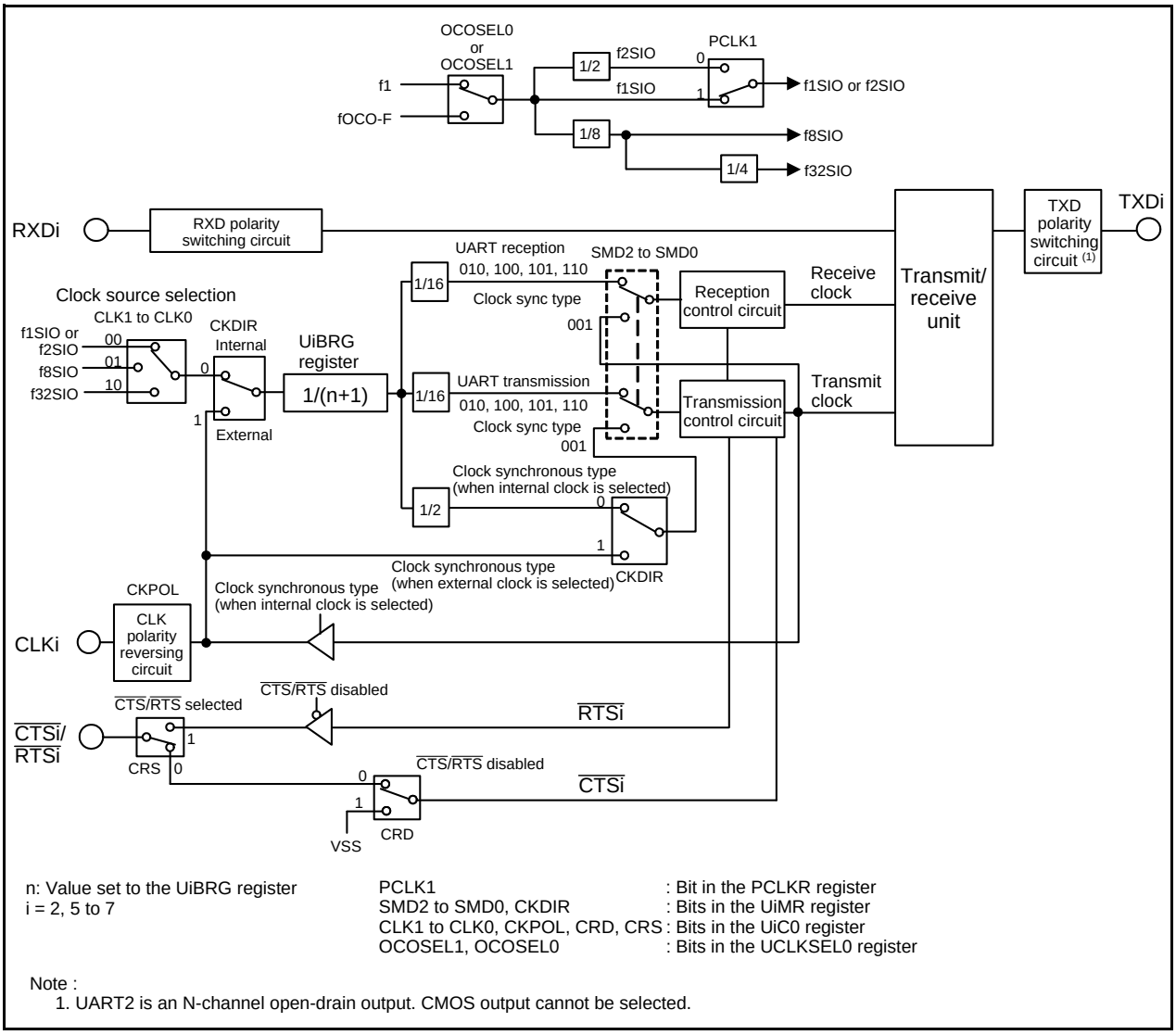


Figure 23.2 UART1 Block Diagram



n: Value set to the UiBRG register
i = 2, 5 to 7

PCLK1 : Bit in the PCLKR register
SMD2 to SMD0, CKDIR : Bits in the UiMR register
CLK1 to CLK0, CKPOL, CRD, CRS : Bits in the UiC0 register
OCOSEL1, OCOSEL0 : Bits in the UCLKSEL0 register

Note :
1. UART2 is an N-channel open-drain output. CMOS output cannot be selected.

Figure 23.3 Block Diagram of UART2, and UART5 to UART7

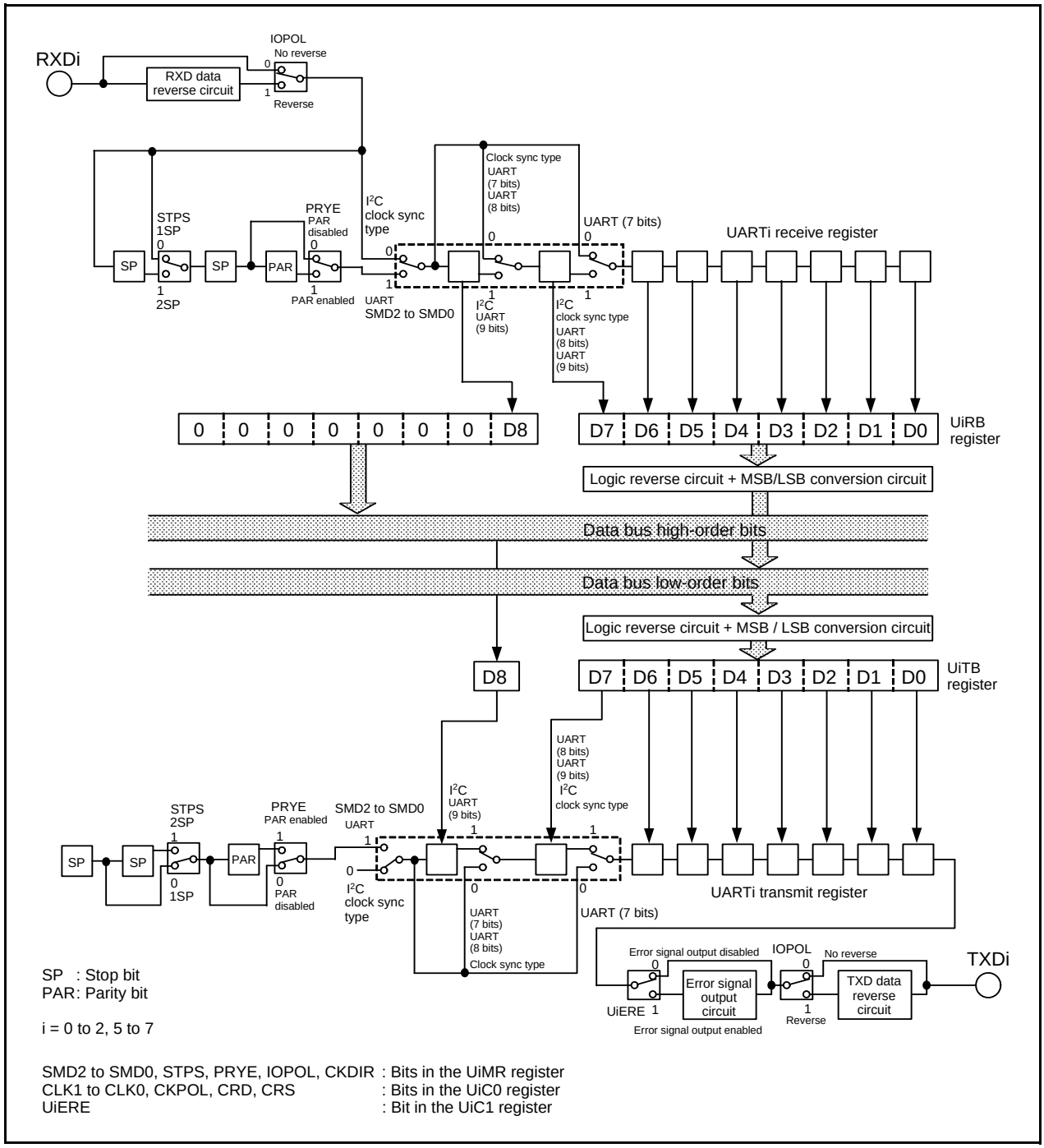


Figure 23.4 UARTi Transmit/Receive Unit Block Diagram

23.2 Registers

Table 23.3 and Table 23.4 list registers associated with UART0 to UART2 and UART5 to UART7.
Set the OCOSEL0 or OCOSEL1 bit in the UCLKSEL0 register before setting other registers associated with UART0 to UART2 and UART5 to UART7. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART5 to UART7 again.
Refer to “Registers Used and Settings” in each mode for the settings of registers and bits.

Table 23.3 Register Structure (1/2)

Address	Register Name	Register Symbol	After Reset
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0244h	UART0 Special Mode Register 4	U0SMR4	00h
0245h	UART0 Special Mode Register 3	U0SMR3	000X 0X0Xb
0246h	UART0 Special Mode Register 2	U0SMR2	X000 0000b
0247h	UART0 Special Mode Register	U0SMR	X000 0000b
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	00XX 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h	UART Transmit/Receive Control Register 2	UCON	X000 0000b
0252h	UART Clock Select Register	UCLKSEL0	X0h
0254h	UART1 Special Mode Register 4	U1SMR4	00h
0255h	UART1 Special Mode Register 3	U1SMR3	000X 0X0Xb
0256h	UART1 Special Mode Register 2	U1SMR2	X000 0000b
0257h	UART1 Special Mode Register	U1SMR	X000 0000b
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	00XX 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh
0284h	UART5 Special Mode Register 4	U5SMR4	00h
0285h	UART5 Special Mode Register 3	U5SMR3	000X 0X0Xb

Table 23.4 Register Structure (2/2)

Address	Register Name	Register Symbol	After Reset
0286h	UART5 Special Mode Register 2	U5SMR2	X000 0000b
0287h	UART5 Special Mode Register	U5SMR	X000 0000b
0288h	UART5 Transmit/Receive Mode Register	U5MR	00h
0289h	UART5 Bit Rate Register	U5BRG	XXh
028Ah 028Bh	UART5 Transmit Buffer Register	U5TB	XXh XXh
028Ch	UART5 Transmit/Receive Control Register 0	U5C0	0000 1000b
028Dh	UART5 Transmit/Receive Control Register 1	U5C1	0000 0010b
028Eh 028Fh	UART5 Receive Buffer Register	U5RB	XXh XXh
0294h	UART6 Special Mode Register 4	U6SMR4	00h
0295h	UART6 Special Mode Register 3	U6SMR3	000X 0X0Xb
0296h	UART6 Special Mode Register 2	U6SMR2	X000 0000b
0297h	UART6 Special Mode Register	U6SMR	X000 0000b
0298h	UART6 Transmit/Receive Mode Register	U6MR	00h
0299h	UART6 Bit Rate Register	U6BRG	XXh
029Ah 029Bh	UART6 Transmit Buffer Register	U6TB	XXh XXh
029Ch	UART6 Transmit/Receive Control Register 0	U6C0	0000 1000b
029Dh	UART6 Transmit/Receive Control Register 1	U6C1	0000 0010b
029Eh 029Fh	UART6 Receive Buffer Register	U6RB	XXh XXh
02A4h	UART7 Special Mode Register 4	U7SMR4	00h
02A5h	UART7 Special Mode Register 3	U7SMR3	000X 0X0Xb
02A6h	UART7 Special Mode Register 2	U7SMR2	X000 0000b
02A7h	UART7 Special Mode Register	U7SMR	X000 0000b
02A8h	UART7 Transmit/Receive Mode Register	U7MR	00h
02A9h	UART7 Bit Rate Register	U7BRG	XXh
02AAh 02ABh	UART7 Transmit Buffer Register	U7TB	XXh XXh
02ACh	UART7 Transmit/Receive Control Register 0	U7C0	0000 1000b
02ADh	UART7 Transmit/Receive Control Register 1	U7C1	0000 0010b
02AEh 02AFh	UART7 Receive Buffer Register	U7RB	XXh XXh

23.2.1 UART Clock Select Register (UCLKSEL0)

UART Clock Select Register

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
X	X	X	X			0	0	UCLKSEL0	0252h	X0h

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
OCOSEL0	Clock select prior to UART0 to UART2 division bit	0 : f1 1 : fOCO-F	RW
OCOSEL1	Clock select prior to UART5 to UART7 division bit	0 : f1 1 : fOCO-F	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value		—

OCOSEL0 (Clock Select Prior to UART0 to UART2 Division Bit) (b2)
OCOSEL1 (Clock Select Prior to UART5 to UART 7 Division Bit) (b3)

Set bits OCOSEL0 and OCOSEL1 while transmission/reception of UART0 to UART2 and UART5 to UART7 stops.
Set the OCOSEL0 or OCOSEL1 bit before setting other registers associated with UART0 to UART2 and UART5 to UART7. After changing the OCOSEL0 or OCOSEL1 bit, set other registers associated with UART0 to UART2 and UART5 to UART7 again.

23.2.2 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register

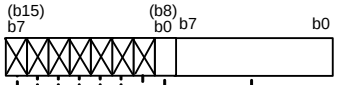
b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
0	0		0	0	0			PCLKR	0012h	0000 0011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A and B clock select bit (clock source for timers A and B, the dead time timer, and muliti-master I^2C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART2, UART5 to UART7, SI/O3, and SI/O4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0	RW
PCLK5	Clock output function extension bit (valid in single-chip mode)	0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1	RW
— (b7-b6)	Reserved bits	Set to 0	RW

Set the PRC0 bit in the PRCR register to 1 (write enabled) before the PCLKR register is rewritten.

23.2.3 UARTi Transmit Buffer Register (UiTB) (i = 0 to 2, 5 to 7)

UARTi Transmit Buffer Register (i = 0 to 2, 5 to 7)



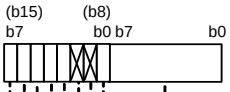
Symbol	Address	After Reset
U0TB	024Bh to 024Ah	Undefined
U1TB	025Bh to 025Ah	Undefined
U2TB	026Bh to 026Ah	Undefined
U5TB	028Bh to 028Ah	Undefined
U6TB	029Bh to 029Ah	Undefined
U7TB	02ABh to 02AAh	Undefined

Function	RW
Transmit data	WO
No register bits. If necessary, set to 0. Read as undefined value	—

Use MOV instruction to write to this register.
When character bit is 9 bits long, write in 16-bit units, or write in 8-bit units in the order of high-order bytes to low-order bytes.

23.2.4 UARTi Receive Buffer Register (UiRB) (i = 0 to 2, 5 to 7)

UARTi Receive Buffer Register (i = 0 to 2, 5 to 7)



Symbol	Address	After Reset
U0RB	024Fh to 024Eh	Undefined
U1RB	025Fh to 025Eh	Undefined
U2RB	026Fh to 026Eh	Undefined
U5RB	028Fh to 028Eh	Undefined
U6RB	029Fh to 029Eh	Undefined
U7RB	02AFh to 02AEh	Undefined

Bit Symbol	Bit Name	Function	RW
— (b7-b0)	——	Receive data (D7 to D0)	RO
— (b8)	——	Receive data (D8)	RO
— (b10-b9)	No register bits. If necessary, set to 0. Read as undefined value		—
ABT	Arbitration lost detect flag	0 : Not detected 1 : Detected	RW
OER	Overrun error flag	0 : No overrun error 1 : Overrun error found	RO
FER	Framing error flag	0 : No framing error 1 : Framing error found	RO
PER	Parity error flag	0 : No parity error 1 : Parity error found	RO
SUM	Error sum flag	0 : No error 1 : Error found	RO

When bits SMD2 to SMD0 in the UiMR register is 100b, 101b or 110b, read in 16-bit units, or read in 8-bit units in the order of high-order bytes to low-order bytes.
Bits FER and PER arranged in the high-order bytes become 0 when the lower bytes of the UiRB register are read.
If an overrun error occurs, the receive data of the UiRB register will be undefined.

ABT (Arbitration Lost Detect Flag) (b11)

The ABT bit is set to 0 by a program. (It remains unchanged even if 1 is written.)

OER (Overrun Error Flag) (b12)

Condition to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).

Condition to become 1:

- The RI bit in the UiC1 register is 1 (data present in UiRB register), and the last bit of the next data is received.

FER (Framing Error Flag) (b13)

The FER bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). Read as undefined value.

Condition to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- The lower bytes of the UiRB register are read.

Condition to become 1:

- The set number of stop bits is not detected.
  (detected when the received data is transferred from the UARTi receive register to the UiRB register.)

PER (Parity Error Flag) (b14)

The PER bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). Read as undefined value.

Condition to become 0:

- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- The lower bytes of the UiRB register are read.

Condition to become 1:

- The number of 1s of the parity bit and character bit does not match the set value of the PRY bit in the UiMR register.
  (detected when the received data is transferred from the UARTi receive register to the UiRB register.)

SUM (Error Sum Flag) (b15)

The SUM bit is disabled when bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). Read as undefined value.

Condition to become 0:

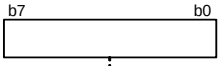
- Bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
- The RE bit in the UiC1 register is 0 (reception disabled).
- All of bits PER, FER and OER are 0 (no error).

Condition to become 1:

- More than one of bits PER, FER or OER is 1 (error found).

23.2.5 UARTi Bit Rate Register (UiBRG) (i = 0 to 2, 5 to 7)

UARTi Bit Rate Register (i = 0 to 2, 5 to 7)



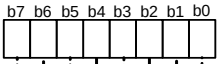
Symbol	Address	After Reset
U0BRG, U1BRG, U2BRG	0249h, 0259h, 0269h	Undefined
U5BRG, U6BRG, U7BRG	0289h, 0299h, 02A9h	Undefined

Function	Setting Range	RW
If set value is n, UiBRG divides the count source by n + 1	00h to FFh	WO

Write to the UiBRG register while serial interface is neither transmitting nor receiving.
Use MOV instruction to write to the UiBRG register.
Write to the UiBRG register after setting bits CLK1 to CLK0 in the UiC0 register.

23.2.6 UARTi Transmit/Receive Mode Register (UiMR) (i = 0 to 2, 5 to 7)

UARTi Transmit/Receive Mode Register (i = 0 to 2, 5 to 7)

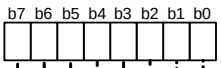


Symbol	Address	After Reset
U0MR, U1MR, U2MR	0248h, 0258h, 0268h	00h
U5MR, U6MR, U7MR	0288h, 0298h, 02A8h	00h

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 0 1 0 : I^2C mode 1 0 0 : UART mode character bit length is 7 bits 1 0 1 : UART mode character bit length is 8 bits 1 1 0 : UART mode character bit length is 9 bits Do not set values other than the above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bits	RW
PRY	Odd/even parity select bit	Valid when PRYE is 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
IOPOL	TXD, RXD I/O polarity reverse bit	0 : No reverse 1 : Reverse	RW

23.2.7 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 to 2, 5 to 7)

UARTi Transmit/Receive Control Register 0 (i = 0 to 2, 5 to 7)



Symbol	Address	After Reset
U0C0, U1C0, U2C0 U5C0, U6C0, U7C0	024Ch, 025Ch, 026Ch 028Ch, 029Ch, 02ACh	0000 1000b 0000 1000b

Bit Symbol	Bit Name	Function	RW
CLK0	UiBRG count source select bit	b1 b0 0 0 : f1SIO or f2SIO selected 0 1 : f8SIO selected 1 0 : f32SIO selected 1 1 : Do not set	RW
CLK1			RW
CRS	$\overline{CTS}/\overline{RTS}$ function select bit	Valid when CRD is 0 0 : $\overline{CTS}$ function selected 1 : $\overline{RTS}$ function selected	RW
TXEPT	Transmit register empty flag	0 : Data present in transmit register (transmission in progress) 1 : No data present in transmit register (transmission completed)	RO
CRD	$\overline{CTS}/\overline{RTS}$ disable bit	0 : $\overline{CTS}/\overline{RTS}$ function enabled 1 : $\overline{CTS}/\overline{RTS}$ function disabled	RW
NCH	Data output select bit	0 : Pins TXDi/SDAi and SCLi are CMOS output 1 : Pins TXDi/SDAi and SCLi are N-channel open-drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge 1 : Transmit data is output at the rising edge of transmit/receive clock and receive data is input at the falling edge	RW
UFORM	Bit order select bit	0 : LSB first 1 : MSB first	RW

CLK1 to CLK0 (UiBRG Count Source Select Bit) (b1-b0)

When bits CLK1 to CLK0 are 00b (f1SIO or f2SIO selected), select f1SIO or f2SIO by the PCLK1 bit in the PCLKR register.
Set bits CLK1 to CLK0 after setting registers UCLKSEL0 and PCLKR.
If bits CLK1 to CLK0 are changed, set the UiBRG register.

CRS ($\overline{CTS}/\overline{RTS}$ Function Select Bit) (b2)

$\overline{CTS1}/\overline{RTS1}$ can be used when the CLKMD1 bit in the UCON register is 0 (CLK output is only from CLK1) and the RCSP bit in the UCON register is 0 ($\overline{CTS0}/\overline{RTS0}$ not separated).

CRD ($\overline{CTS}/\overline{RTS}$ Disable Bit) (b4)

When the CRD bit is 1 ($\overline{CTS}/\overline{RTS}$ function disabled), the $\overline{CTSi}/\overline{RTSi}$ pin can be used as an input/output port.

NCH (Data Output Select Bit) (b5)

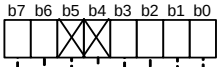
TXD2/SDA2 and SCL2 are N-channel open-drain outputs. They cannot be set to CMOS output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.
This function is used to set P-channel transistor of the COMS output buffer always off, but not to change pins TXDi/SDAi and SCLi to open-drain output completely.
Check electrical characteristics for the input voltage range.

UFORM (Bit Order Select Bit) (b7)

The UFORM bit is enabled when bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), or 101b (UART mode, 8-bit character data).
Set the UFORM bit to 1 when bits SMD2 to SMD0 are 010b (I^2C mode), and to 0 when bits SMD2 to SMD0 are 100b (UART mode, 7-bit character data) or 110b (UART mode, 9-bit character data).

23.2.8 UARTi Transmit/Receive Control Register 1 (UiC1) (i = 0 to 2, 5 to 7)

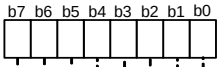
UARTi Transmit/Receive Control Register 1 (i = 0, 1)



Symbol	Address	After Reset
U0C1, U1C1	024Dh, 025Dh	00XX 0010b

Bit Symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RO
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag	0 : No data present in UiRB register 1 : Data present in UiRB register	RO
— (b5-b4)	No register bits. If necessary, set to 0. Read as undefined value		—
UiLCH	Data logic select bit	0 : No reverse 1 : Reverse	RW
UiERE	Error signal output enable bit	0 : Output disabled 1 : Output enabled	RW

UARTi Transmit/Receive Control Register 1 (i = 2, 5 to 7)



Symbol	Address	After Reset
U2C1	026Dh	0000 0010b
U5C1, U6C1, U7C1	028Dh, 029Dh, 02ADh	0000 0010b

Bit symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RO
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag	0 : No data present in UiRB register 1 : Data present in UiRB register	RO
UiIRS	UARTi transmit interrupt source select bit	0 : UiTB register empty (TI = 1) 1 : Transmit completed (TXEPT = 1)	RW
UiRRM	UARTi continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
UiLCH	Data logic select bit	0 : No reverse 1 : Reverse	RW
UiERE	Error signal output enable bit	0 : Output disabled 1 : Output enabled	RW

Bits UiIRS and UiRRM of UART0 and UART1 are bits in the UCON register.

UiLCH (Data Logic Select Bit) (b6)

The UiLCH bit enabled when bits SMD2 to SMD0 in the UiMR register are 001b (clock synchronous serial I/O mode), 100b (UART mode, 7-bit character data), or 101b (UART mode, 8-bit character data). Set this bit to 0 when bits SMD2 to SMD0 are set to 010b (I^2C mode) or 110b (UART mode, 9-bit character data).

23.2.9 UART Transmit/Receive Control Register 2 (UCON)

UART Transmit/Receive Control Register 2

b7	b6	b5	b4	b3	b2	b1	b0
X							

Symbol	Address	After Reset
UCON	0250h	X000 0000b

Bit symbol	Bit Name	Function	RW
U0IRS	UART0 transmit interrupt source select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U1IRS	UART1 transmit interrupt source select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	RW
U0RRM	UART0 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
U1RRM	UART1 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
CLKMD0	UART1CLK, CLKS select bit 0	Valid when CLKMD1 is 1 0 : Clock output from CLK1 1 : Clock output from CLKS1	RW
CLKMD1	UART1CLK, CLKS select bit 1	0 : CLK output is only from CLK1 1 : Transmit/receive clock output from multiple-pin output function selected	RW
RCSP	Separate UART0 $\overline{CTS}/\overline{RTS}$ bit	0 : $\overline{CTS}/\overline{RTS}$ shared pin 1 : $\overline{CTS}/\overline{RTS}$ separated	RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value		—

Bits UiIRS and UiRRM of UART2 and UART5 to UART7 are bits in the UiC1 register.

CLKMD1 (UART1CLK, CLKS Select Bit 1) (b5)

When using multiple transmit/receive clock output pins, make sure the following condition is met:
the CKDIR bit in the U1MR register = 0 (internal clock)

23.2.10 UARTi Special Mode Register (UiSMR) (i = 0 to 2, 5 to 7)

UARTi Special Mode Register (i = 0 to 2, 5 to 7)

b7	b6	b5	b4	b3	b2	b1	b0
X				0			

Symbol	Address	After Reset
U0SMR, U1SMR, U2SMR U5SMR, U6SMR, U7SMR	0247h, 0257h, 0267h 0287h, 0297h, 02A7h	X000 0000b X000 0000b

Bit Symbol	Bit Name	Function	RW
IICM	I^2C mode select bit	0 : Other than I^2C mode 1 : I^2C mode	RW
ABC	Arbitration lost detect flag control bit	0 : Update per bit 1 : Update per byte	RW
BBS	Bus busy flag	0 : Stop-condition detected 1 : Start-condition detected (busy)	RW
— (b3)	Reserved bit	Set to 0	RW
ABSCS	Bus collision detect sampling clock select bit	0 : Rising edge of transmit/receive clock 1 : Underflow signal of timer Aj	RW
ACSE	Auto clear function select bit of transmit enable bit	0 : No auto clear function 1 : Auto clear at occurrence of bus collision	RW
SSS	Transmit start condition select bit	0 : Not synchronized to RXDi 1 : Synchronized to RXDi	RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value		—

BBS (Bus Busy Flag) (b2)

The BBS bit is set to 0 by a program. (It remains unchanged even if 1 is written.)

ABSCS (Bus Collision Detect Sampling Clock Select Bit) (b4)

When the ABSCS bit is 1, the combinations of UARTi and timer Aj are as follows:

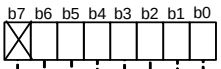
UART0, UART6: Underflow signal of timer A3
UART1, UART7: Underflow signal of timer A4
UART2, UART5: Underflow signal of timer A0

SSS (Transmit Start Condition Select Bit) (b6)

When a transmit starts, the SSS bit is set to 0 (not synchronized to RXDi).

23.2.11 UARTi Special Mode Register 2 (UiSMR2) (i = 0 to 2, 5 to 7)

UARTi Special Mode Register 2 (i = 0 to 2, 5 to 7)

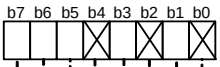


Symbol	Address	After Reset
U0SMR2, U1SMR2, U2SMR2 U5SMR2, U6SMR2, U7SMR2	0246h, 0256h, 0266h 0286h, 0296h, 02A6h	X000 0000b X000 0000b

Bit Symbol	Bit Name	Function	RW
IICM2	I^2C mode select bit 2	See table 23.18 "I^2C Mode Functions"	RW
CSC	Clock synchronization bit	0 : Disabled 1 : Enabled	RW
SWC	SCL wait output bit	0 : Disabled 1 : Enabled	RW
ALS	SDA output stop bit	0 : Disabled 1 : Enabled	RW
STAC	UARTi initialization bit	0 : Disabled 1 : Enabled	RW
SWC2	SCL wait output bit 2	0: Transmit/receive clock 1: Low-level output	RW
SDHI	SDA output disable bit	0: Enabled 1: Disabled (high-impedance)	RW
— (b7)	No register bit. If necessary, set to 0. Read as undefined value		—

23.2.12 UARTi Special Mode Register 3 (UiSMR3) (i = 0 to 2, 5 to 7)

UARTi Special Mode Register 3 (i = 0 to 2, 5 to 7)



Symbol	Address	After Reset
U0SMR3, U1SMR3, U2SMR3 U5SMR3, U6SMR3, U7SMR3	0245h, 0255h, 0265h 0285h, 0295h, 02A5h	000X 0X0Xb 000X 0X0Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. Read as undefined value		—
CKPH	Clock phase set bit	0 : No clock delay 1 : With clock delay	RW
— (b2)	No register bit. If necessary, set to 0. Read as undefined value		—
NODC	Clock output select bit	0 : CLKi is CMOS output 1 : CLKi is N-channel open drain output	RW
— (b4)	No register bit. If necessary, set to 0. Read as undefined value		—
DL0	SDAi digital delay setup bit	b7 b6 b5 0 0 0 : No delay 0 0 1 : 1 to 2 cycle(s) of UiBRG count source 0 1 0 : 2 to 3 cycles of UiBRG count source 0 1 1 : 3 to 4 cycles of UiBRG count source 1 0 0 : 4 to 5 cycles of UiBRG count source 1 0 1 : 5 to 6 cycles of UiBRG count source 1 1 0 : 6 to 7 cycles of UiBRG count source 1 1 1 : 7 to 8 cycles of UiBRG count source	RW
DL1			RW
DL2			RW

NODC (Clock Output Select Bit) (b3)

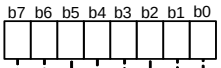
This function is used to set P-channel transistor of the COMS output buffer always off, but not to change the CLKi pin to open-drain output completely.
Check electrical characteristics for the input voltage range.

DL2-DL0 (SDAi Digital Delay Setup Bit) (b7-b5)

Bits DL2 to DL0 are used to generate a delay in SDAi output by digital means in I^2C mode. Except for I^2C mode, set these bits to 000b (no delay).
The amount of delay varies with the load on pins SCLi and SDAi. Also, when using an external clock, the amount of delay increases by about 100 ns.

23.2.13 UARTi Special Mode Register 4 (UiSMR4) (i = 0 to 2, 5 to 7)

UARTi Special Mode Register 4 (i = 0 to 2, 5 to 7)



Symbol	Address	After Reset
U0SMR4, U1SMR4, U2SMR4	0244h, 0254h, 0264h	00h
U5SMR4, U6SMR4, U7SMR4	0284h, 0294h, 02A4h	00h

Bit Symbol	Bit Name	Function	RW
STAREQ	Start condition generate bit	0 : Clear 1 : Start	RW
RSTAREQ	Restart condition generate bit	0 : Clear 1 : Start	RW
STPREQ	Stop condition generate bit	0 : Clear 1 : Start	RW
STSPSEL	SCL, SDA output select bit	0 : Start and stop conditions not output 1 : Start and stop conditions output	RW
ACKD	ACK data bit	0 : ACK 1 : NACK	RW
ACKC	ACK data output enable bit	0 : Serial interface data output 1 : ACK data output	RW
SCLHI	SCL output stop enable bit	0 : Disabled 1 : Enabled	RW
SWC9	SCL wait bit 3	0 : SCL low hold disabled 1 : SCL low hold enabled	RW

STAREQ (Start Condition Generate Bit) (b0)

The STAREQ bit becomes 0 when the start condition is generated.

RSTAREQ (Restart Condition Generate Bit) (b1)

The RSTAREQ bit becomes 0 when the restart condition is generated.

STPREQ (Stop Condition Generate Bit) (b2)

The STPREQ bit becomes 0 when the stop condition is generated.

23.3 Operations

23.3.1 Clock Synchronous Serial I/O Mode

The clock synchronous serial I/O mode uses a transmit/receive clock to transmit/receive data. Table 23.5 lists the Clock Synchronous Serial I/O Mode Specifications.

Table 23.5 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Data format	Character bit length: 8 bits
Transmit/receive clock	• CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{2(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n = Setting value of UiBRG register 00h to FFh • CKDIR bit = 1 (external clock): Input from CLKi pin
Transmission and reception control	Selectable from $\overline{CTS}$ function, $\overline{RTS}$ function or $\overline{CTS}$/$\overline{RTS}$ function disabled
Transmission start conditions	To start transmission, satisfy the following requirements (1) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in UiTB register) • If $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low.
Reception start conditions	To start reception, satisfy the following requirements (1) • The RE bit in the UiC1 register = 1 (reception enabled) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in the UiTB register)
Interrupt request generation timing	Transmit interrupt: One of the following can be selected. • The UiIRS bit = 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission) • The UiIRS bit =1 (transmission completed): When the serial interface completed sending data from the UARTi transmit register Receive interrupt: • When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error detection	Overrun error (2) This error occurs if the serial interface started receiving the next unit of data before reading the UiRB register and received the 7th bit of the next unit of data
Selectable functions	• CLK polarity selection Data input/output can be selected to occur synchronously with the rising or the falling edge of the transmit/receive clock • LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected • Continuous receive mode selection Reception is enabled immediately by reading the UiRB register • Switching serial data logic This function reverses the logic value of the transmit/receive data • Transmit/receive clock output from multiple pins selection (UART1) The output pin can be selected by a program by setting two UART1 transmit/receive clock pins. • Separate $\overline{CTS}$/$\overline{RTS}$ pins (UART0) $\overline{CTS0}$ and $\overline{RTS0}$ are input/output from separate pins

i = 0 to 2, 5 to 7

Notes:

1. When an external clock is selected, either of the following conditions must be met: If the CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transmit/receive clock), the external clock is in the high state; if the CKPOL bit in the UiC0 register is 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transmit/receive clock), the external clock is in the low state.
2. If an overrun error occurs, the receive data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 23.6 lists Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transmit/Receive Clock Output Pin Function Not Selected). Table 23.7 lists P6_4 Pin Functions in Clock Synchronous Serial I/O Mode.
Note that for a period from when UARTi operating mode is selected to when transmission starts, the TXDi pin outputs a high-level signal. (If N-channel open-drain output is selected, this pin is in high-impedance state.)

Table 23.6 Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transmit/Receive Clock Output Pin Function Not Selected)

Pin Name	I/O	Function	Method of Selection
TXDi	Output	Serial data output	(Outputs dummy data when performing reception only.)
RXDi	Input	Serial data input	Set the port direction bits sharing pins to 0.
	Input	Input port	Set the port direction bits to 0. (can be used as an input port when performing transmission only)
CLKi	Output	Transmit/receive clock output	The CKDIR bit in the UiMR register = 0
	Input	Transmit/receive clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bits sharing pins to 0.
$\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$	Input	$\overline{\text{CTS}}$ input	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 0 Set the port direction bits sharing pins to 0.
	Output	$\overline{\text{RTS}}$ output	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 1
	Input/ output	I/O port	The CRD bit in the UiC0 register = 1

i = 0 to 2, 5 to 7

Table 23.7 P6_4 Pin Functions in Clock Synchronous Serial I/O Mode

Pin Function	Bit Set Value					
	U1C0 Register		UCON Register			PD6 Register
	CRD	CRS	RCSP	CLKMD1	CLKMD0	PD6_4
P6_4	1	-	0	0	-	Input: 0, Output: 1
$\overline{\text{CTS1}}$	0	0	0	0	-	0
$\overline{\text{RTS1}}$	0	1	0	0	-	-
$\overline{\text{CTS0}}$ (1)	0	0	1	0	-	0
CLKS1	-	-	-	1 (2)	1	-

- indicates either 0 or 1

Notes:
1. In addition to this, set the CRD bit in the U0C0 register to 0 ($\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$ enabled) and the CRS bit in the U0C0 register to 1 ($\overline{\text{RTS0}}$ selected).
2. When the CLKMD1 bit is 1 and the CLKMD0 bit is 0, the following logic levels are output.
   - High if the CLKPOL bit in the U1C0 register is 0
   - Low if the CLKPOL bit in the U1C0 register is 1

Table 23.8 lists Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 23.8 Registers Used and Settings in Clock Synchronous Serial I/O Mode

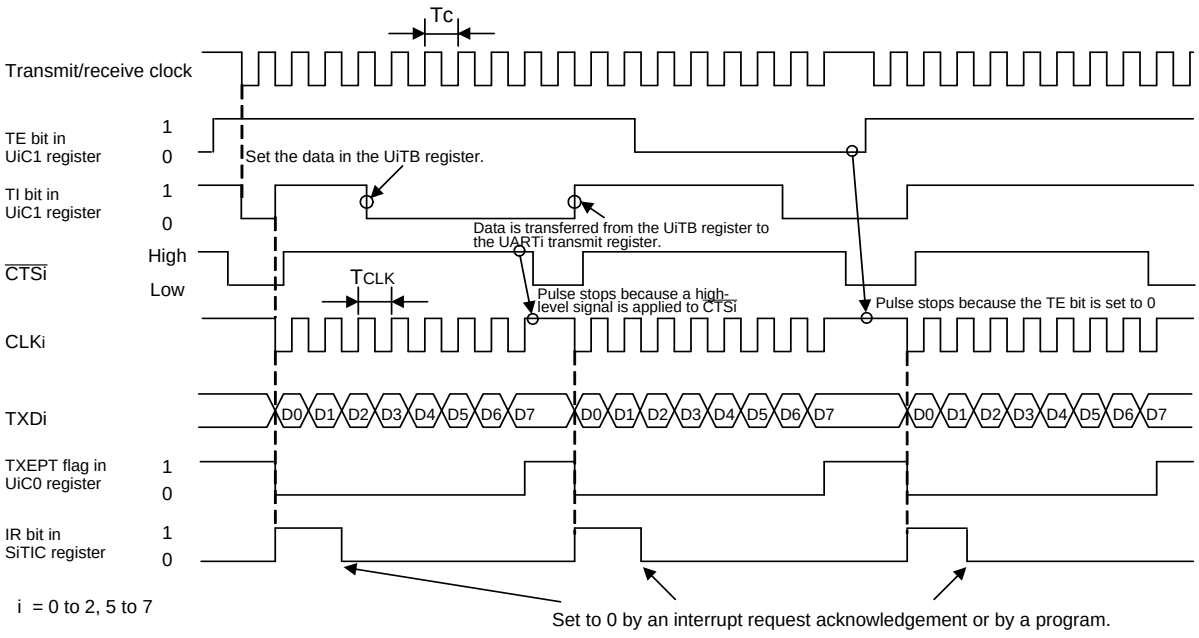
Register	Bits	Function
UiTB (2)	0 to 7	Set transmission data
UiRB (2)	0 to 7	Reception data can be read.
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate.
UiMR (2)	SMD2 to SMD0	Set to 001b.
	CKDIR	Select the internal clock or external clock.
	IOPOL	Set to 0.
UiC0	CLK1 to CLK0	Select the count source for the UiBRG register.
	CRS	If $\overline{CTS}$ or $\overline{RTS}$ is used, select which function to use.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{CTS}$ or $\overline{RTS}$ function.
	NCH	Select TXDi pin output mode. (1)
	CKPOL	Select the transmit/receive clock polarity.
	UFORM	Select LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UjIRS	Select source of UARTj transmit interrupt.
	UjRRM	Set to 1 to use continuous receive mode.
	UiLCH	Set to 1 to use inverted data logic.
	UiERE	Set to 0.
UiSMR	0 to 7	Set to 0.
UiSMR2	0 to 7	Set to 0.
UiSMR3	0 to 2	Set to 0.
	NODC	Select clock output mode.
	4 to 7	Set to 0.
UiSMR4	0 to 7	Set to 0.
UCON	U0IRS	Select source of UART0 transmit interrupt.
	U1IRS	Select source of UART1 transmit interrupt.
	U0RRM	Set to 1 to use continuous receive mode.
	U1RRM	Set to 1 to use continuous receive mode.
	CLKMD0	Select the transmit/receive clock output pin when CLKMD1 is 1.
	CLKMD1	Set to 1 to output UART1 transmit/receive clock from two pins.
	RCSP	Set to 1 to separate the $\overline{CTS0}$/$\overline{RTS}$ signal of UART0.
	7	Set to 0.
IFSR3A	IFSR34	Set to 0 to use UART5 transmit interrupt.
	IFSR36	Set to 0 to use UART6 transmit interrupt.
IFSR2A	IFSR25	Set to 0 to use UART7 transmit interrupt.

i = 0 to 2, 5 to 7 j = 2, 5 to 7

Notes:

1. The TXD2 pin is N channel open-drain output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.
2. Set bits not listed above to 0 when writing to the registers in clock synchronous serial I/O mode.

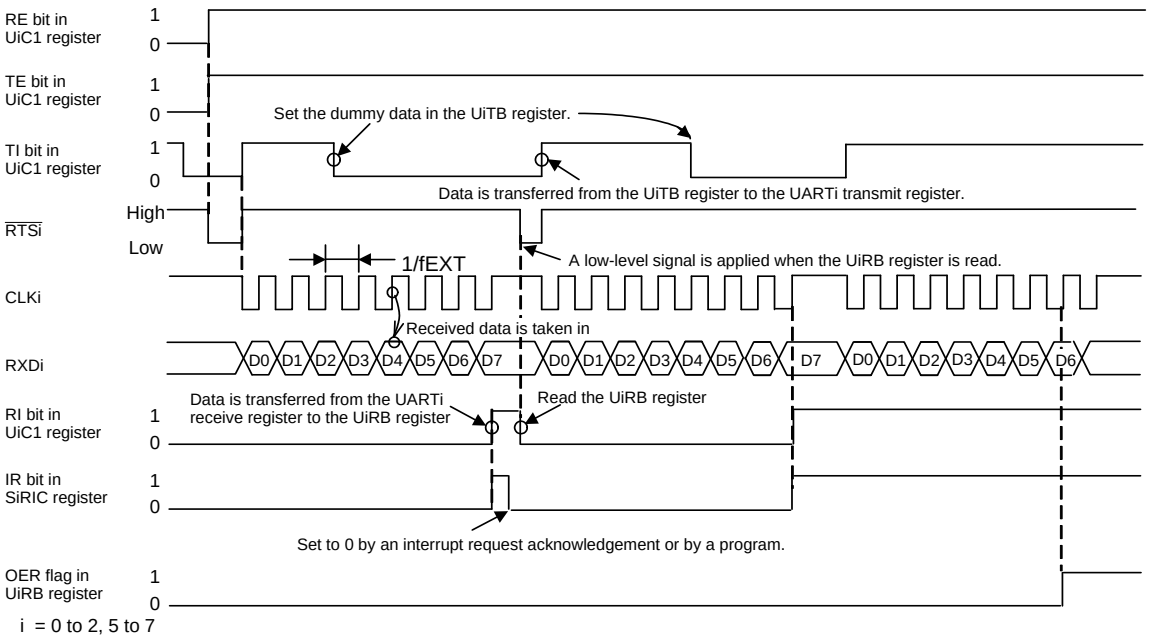
(1) Example of Transmit Timing (Internal Clock Selected)



The above timing diagram applies when the register bits are set as follows:
- The CKDIR bit in the UiMR register = 0 (internal clock)
- The CRD bit in the UiC0 register = 0 (CTS/RTS enabled), the CRS bit = 0 (CTS selected)
- The CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transmit/receive clock)
- The UiIRS bit in the UiC1 register = 0 (an interrupt request occurs when the UiTB register becomes empty)

$T_C = T_{CLK} = 2(n + 1)/fj$
fj: Frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
n: Value set to the UiBRG register

(2) Example of Receive Timing (External Clock Selected)



The above timing diagram applies to the case where the register bits are set as follows:
- The CKDIR bit in the UiMR register = 1 (external clock)
- The CRD bit in the UiC0 register = 0 (CTS/RTS enabled), the CRS bit = 1 (RTS selected)
- The CKPOL bit in the UiC0 register = 0 (transmit data output at the falling edge and receive data taken in at the rising edge of the transmit/receive clock)

fEXT: Frequency of the external clock

Make sure the following conditions are met when input to the CLKi pin before receiving data is high:
- The TE bit in the UiC1 register = 1 (transmit enabled)
- The RE bit in the UiC1 register = 1 (receive enabled)
- Write dummy data to the UiTB register

Figure 23.5 Transmit/Receive Operation during Clock Synchronous Serial I/O Mode

23.3.1.1 Transmit/Receive Register Initialization

When the transmit/receive register needs to be initialized due to an interrupted transmission/reception, follow the procedures below.

- Initializing the UiRB register (i = 0 to 2, 5 to 7)
  (1) Set the RE bit in the UiC1 register to 0 (reception disabled).
  (2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
  (3) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
  (4) Set the RE bit in the UiC1 register to 1 (reception enabled).

- Initializing the UiTB register (i = 0 to 2, 5 to 7)
  (1) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
  (2) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
  (3) Write a 1 to the RE bit in the UiC1 register (transmission enabled), regardless of the value of the TE bit in the UiCi register.

23.3.1.2 CLK Polarity Select Function

Use the CKPOL bit in the UiC0 register (i = 0 to 2, 5 to 7) to select the transmit/receive clock polarity. Figure 23.6 shows the Transmit/Receive Clock Polarity.

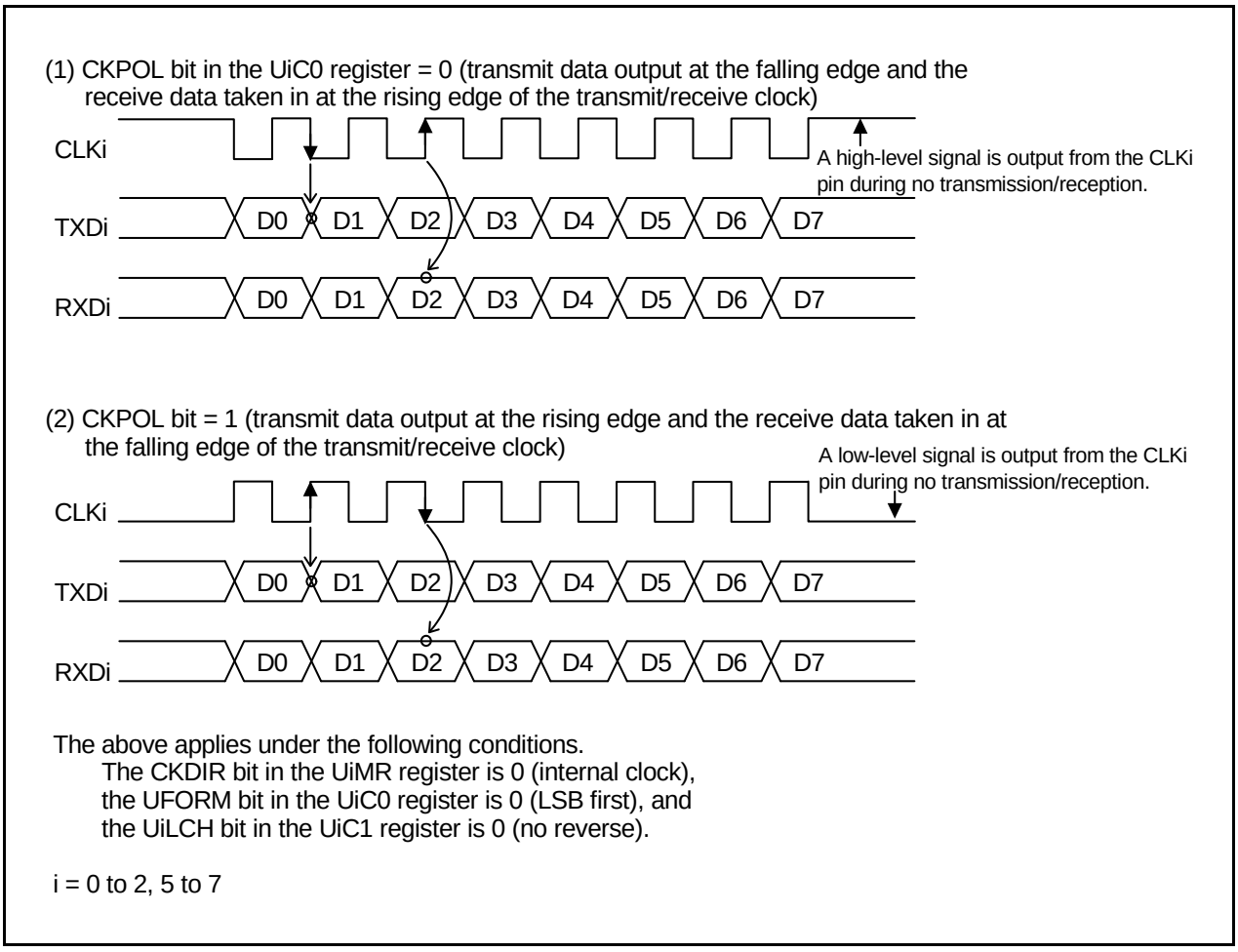
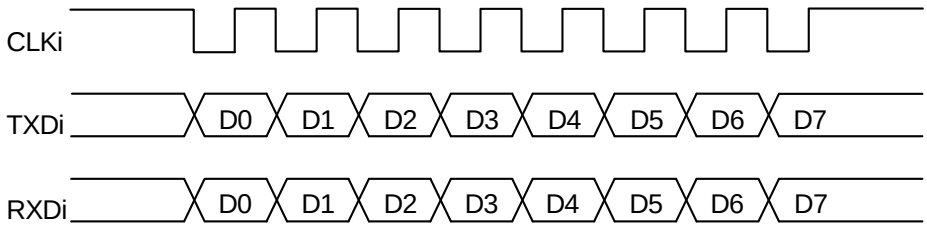


Figure 23.6 Transmit/Receive Clock Polarity

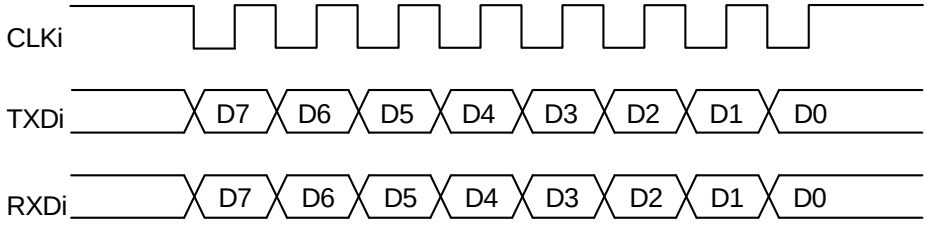
23.3.1.3 LSB First/MSB First Select Function

Use the UFORM bit in the UiC0 register (i = 0 to 2, 5 to 7) to select the bit order. Figure 23.7 shows the Bit Order.

(1) UFORM bit in the UiC0 register = 0 (LSB first)



(2) UFORM bit in the UiC0 register = 1 (MSB first)



The above applies under the following conditions.
The CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transmit/receive clock), and the UiLCH bit in the UiC1 register is 0 (no reverse).

i = 0 to 2, 5 to 7

Figure 23.7 Bit Order

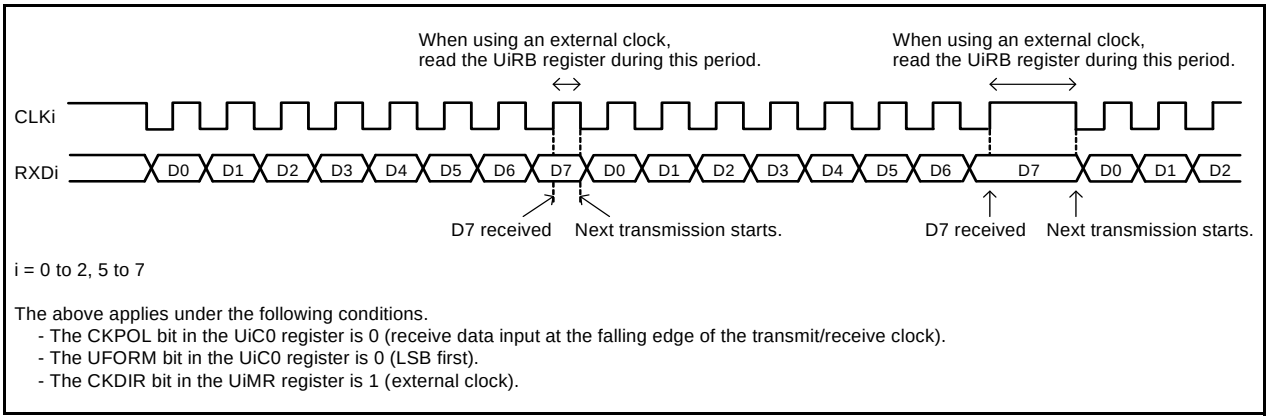
23.3.1.4 Continuous Receive Mode

In continuous receive mode, receive operation is enabled when the receive buffer register is read. It is not necessary to write dummy data to the transmit buffer register to enable receive operation in this mode. However, a dummy read of the receive buffer register is required when starting the operating mode.

When the UiRRM bit (i = 0 to 2, 5 to 7) is 1 (continuous receive mode), the TI bit in the UiC1 register is set to 0 (data present in the UiTB register) by reading the UiRB register. In this case (UiRRM bit = 1), do not write dummy data to the UiTB register by a program.

When using an external clock, read the UiRB register between the eighth bit of data is received and the next transmission starts.

Figure 23.8 shows Operation Example in Continuous Receive Mode.



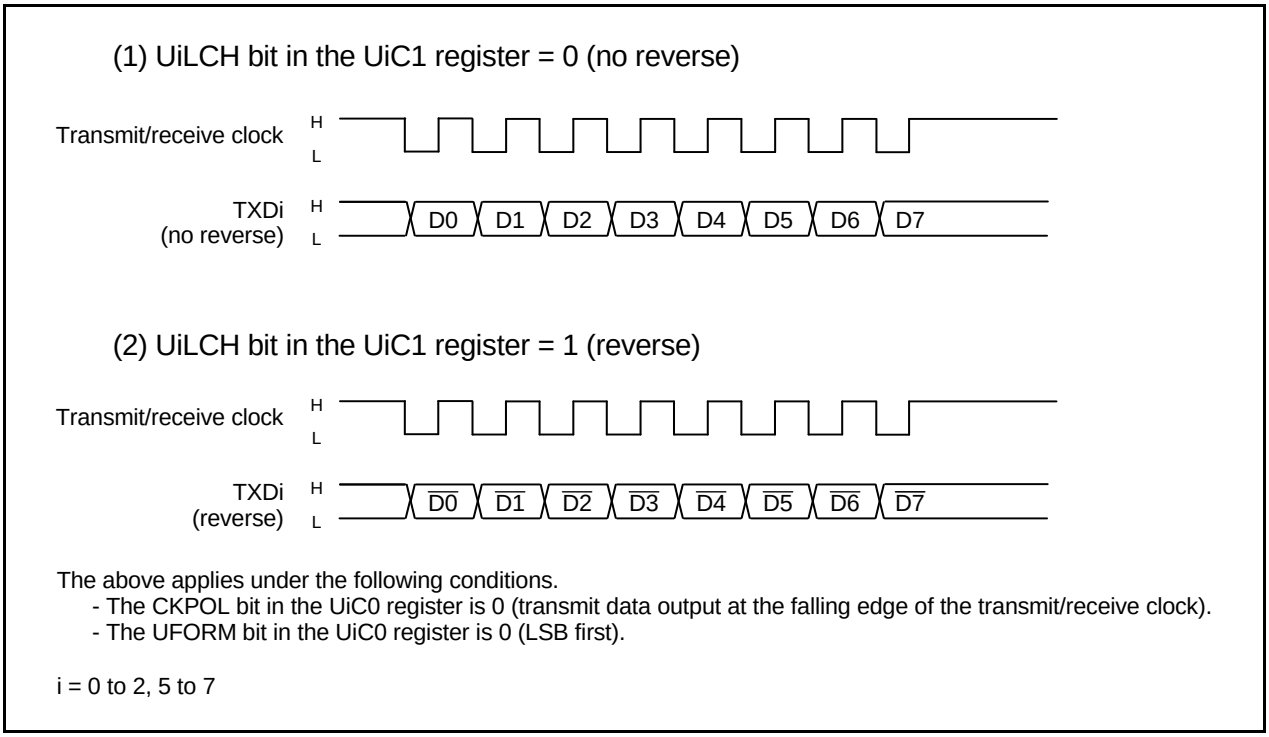
i = 0 to 2, 5 to 7

The above applies under the following conditions.
- The CKPOL bit in the UiC0 register is 0 (receive data input at the falling edge of the transmit/receive clock).
- The UFORM bit in the UiC0 register is 0 (LSB first).
- The CKDIR bit in the UiMR register is 1 (external clock).

Figure 23.8 Operation Example in Continuous Receive Mode

23.3.1.5 Serial Data Logic Switching Function

When the UiLCH bit in the UiC1 register (i = 0 to 2, 5 to 7) is 1 (reverse), the data written to the UiTB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the UiRB register. Figure 23.9 shows Serial Data Logic.



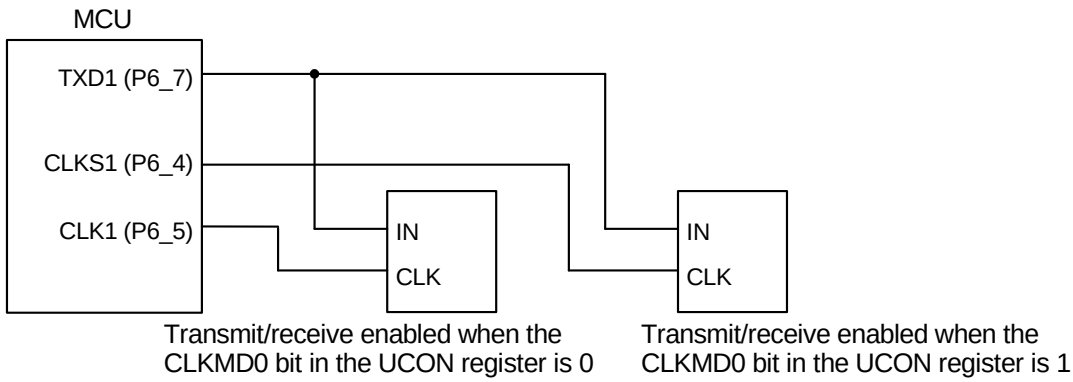
The above applies under the following conditions.
- The CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge of the transmit/receive clock).
- The UFORM bit in the UiC0 register is 0 (LSB first).

i = 0 to 2, 5 to 7

Figure 23.9 Serial Data Logic

23.3.1.6 Transmit/Receive Clock Output from Multiple Pins (UART1)

Use bits CLKMD1 to CLKMD0 in the UCON register to select one of the two transmit/receive clock output pins (see Figure 23.10). This function can be used when the selected transmit/receive clock for UART1 is an internal clock.



The above applies under the following conditions.
- The CKDIR bit in the U1MR register is 0 (internal clock).
- The CLKMD1 bit in the UCON register is 1 (transmit/receive clock output from multiple pins).

Figure 23.10 Transmit/Receive Clock Output from Multiple Pins

23.3.1.7 $\overline{CTS}/\overline{RTS}$ Function

The $\overline{CTS}$ function is used to start transmit/receive operation when a low-level signal is applied to the $\overline{CTSi}/\overline{RTSi}$ (i = 0 to 2, 5 to 7) pin. Transmit/receive operation begins when input to the $\overline{CTSi}/\overline{RTSi}$ pin becomes low. If the low-level signal is switched to high during a transmit or receive operation, the operation stops before the next data.

For the $\overline{RTS}$ function, the $\overline{CTSi}/\overline{RTSi}$ pin outputs a low-level signal when the MCU is ready to receive. The output level goes high on the first falling edge of the CLKi pin.

Refer to Table 23.6 “Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transmit/Receive Clock Output Pin Function Not Selected)”.

23.3.1.8 $\overline{CTS}/\overline{RTS}$ Separate Function (UART0)

This function separates $\overline{CTS0}/\overline{RTS0}$, outputs $\overline{RTS0}$ from the P6_0 pin, and inputs $\overline{CTS0}$ from the P6_4 pin. To use this function, set the register bits as shown below.

- The CRD bit in the U0C0 register= 0 (enable $\overline{CTS}/\overline{RTS}$ of UART0)
- The CRS bit in the U0C0 register= 1 (output $\overline{RTS}$ of UART0)
- The CRD bit in the U1C0 register= 0 (enable $\overline{CTS}/\overline{RTS}$ of UART1)
- The CRS bit in the U1C0 register= 0 (input $\overline{CTS}$ of UART1)
- The RCSP bit in the UCON register= 1 (inputs $\overline{CTS0}$ from the P6_4 pin)
- The CLKMD1 bit in the UCON register= 0 (CLKS1 not used)

Note that when using the $\overline{CTS}/\overline{RTS}$ separate function, $\overline{CTS}/\overline{RTS}$ of UART1 function cannot be used.

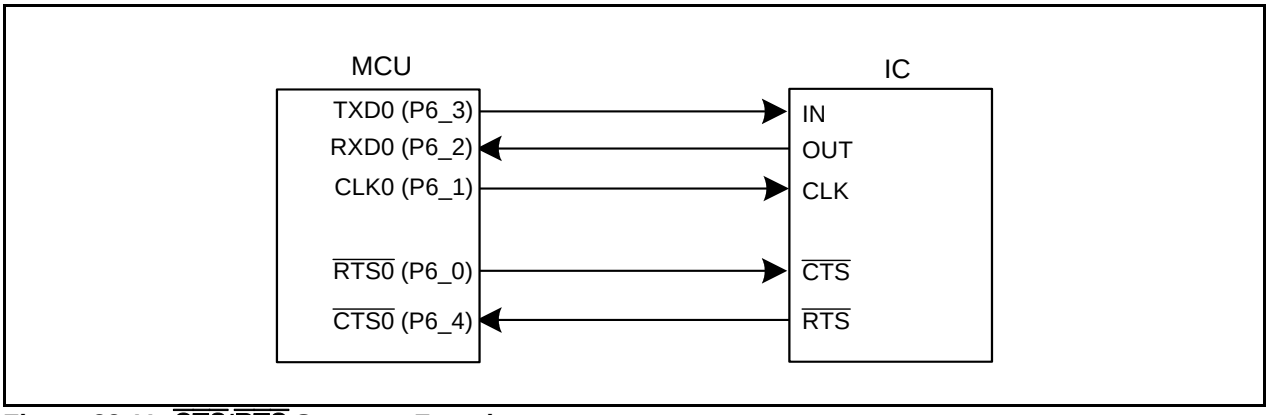


Figure 23.11 $\overline{CTS}/\overline{RTS}$ Separate Function

23.3.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows transmitting and receiving data after setting the desired bit rate and bit order. Table 23.9 lists the UART Mode Specifications.

Table 23.9 UART Mode Specifications

Item	Specification
Data format	• Character bits : Selectable from 7, 8, or 9 bits • Start bit : 1 bit • Parity bit : Selectable from odd, even, or none • Stop bit : Selectable from 1 bit or 2 bits
Transmit/receive clock	• The CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{16(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of UiBRG register 00h to FFh • CKDIR bit = 1 (external clock): $\frac{fEXT}{16(n+1)}$ fEXT: Input from CLKi pin n: Setting value of UiBRG register 00h to FFh
Transmission and reception control	Selectable from $\overline{CTS}$ function, $\overline{RTS}$ function or $\overline{CTS}/\overline{RTS}$ function disabled
Transmission start conditions	To start transmission, satisfy the following requirements. • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in the UiTB register) • If $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low.
Reception start conditions	To start reception, satisfy the following requirements. • The RE bit in the UiC1 register = 1 (reception enabled) • Start bit detection
Interrupt request generation timing	Transmit interrupt: One of the following can be selected. • The UiIRS bit = 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission) • The UiIRS bit =1 (transmission completed): When the serial interface completes sending data from the UARTi transmit register Receive interrupt: • When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the bit one before the last stop bit of the next unit of data. • Framing error This error occurs when the number of stop bits set is not detected • Parity error This error occurs when the number of 1s of the parity bit and character bit does not match the set value of the PRY bit in the UiMR register. • Error sum flag This flag is set to 1 when an overrun, framing, or parity error occurs.
Selectable functions	• LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected • Serial data logic switch This function reverses the logic of the transmit/receive data. The start and stop bits are not reversed. • TXD, RXD I/O polarity switch This function reverses the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are reversed. • Separate $\overline{CTS}/\overline{RTS}$ pins (UART0) $\overline{CTS0}$ and $\overline{RTS0}$ are input/output from separate pins.

i = 0 to 2, 5 to 7

Note:

1. If an overrun error occurs, the receive data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 23.10 lists I/O Pin Functions in UART Mode. Table 23.11 lists the P6_4 Pin Functions in UART Mode. Note that for a period from when the UARTi operating mode is selected to when transmission starts, the TXDi pin outputs a high-level signal. (If N-channel open-drain output is selected, this pin is in high-impedance state.)

Table 23.10 I/O Pin Functions in UART Mode

Pin Name	I/O	Function	Method of Selection
TXDi	Output	Serial data output	(High-level output when performing reception only.)
RXDi	Input	Serial data input	Set the port direction bits sharing pins to 0.
	Input	Input port	Set the port direction bits sharing pins to 0. (can be used as an input port when performing transmission only)
CLKi	Input/ output	Input/output port	The CKDIR bit in the UiMR register = 0
	Input	Transmit/receive clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bits sharing pins to 0.
$\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$	Input	$\overline{\text{CTS}}$ input	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 0 Set the port direction bits sharing pins to 0.
	Output	$\overline{\text{RTS}}$ output	The CRD bit in the UiC0 register = 0 The CRS bit in the UiC0 register = 1
	Input/ output	I/O port	The CRD bit in the UiC0 register = 1

i = 0 to 2, 5 to 7

Table 23.11 P6_4 Pin Functions in UART Mode

Pin Function	Bit Set Value				
	U1C0 Register		UCON Register		PD6 Register
	CRD	CRS	RCSP	CLKMD1	PD6_4
P6_4	1	-	0	0	Input: 0, Output: 1
$\overline{\text{CTS1}}$	0	0	0	0	0
$\overline{\text{RTS1}}$	0	1	0	0	-
$\overline{\text{CTS0}}$ (1)	0	0	1	0	0

– indicates either 0 or1.

Note:

1. In addition to this, set the CRD bit in the U0C0 register to 0 ($\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$ enabled) and the CRS bit in the U0C0 register to 1 ($\overline{\text{RTS0}}$ selected).

Table 23.12 lists Registers Used and Settings in UART Mode.

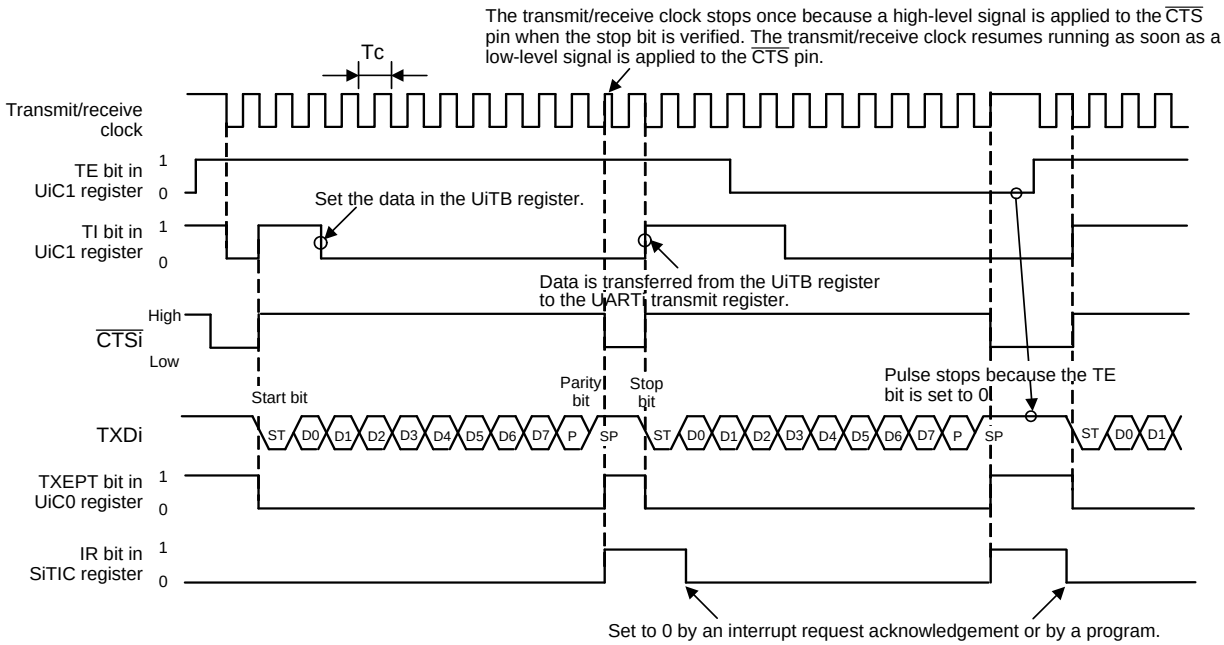
Table 23.12 Registers Used and Settings in UART Mode

Register	Bits	Function
UiTB	0 to 8	Set transmission data. (1), (3)
UiRB	0 to 8	Reception data can be read. (1)
	OER, FER, PER, SUM	Error flag
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 100b when character bit length is 7 bits.
		Set to 101b when character bit length is 8 bits.
		Set to 110b when character bit length is 9 bits.
	CKDIR	Select the internal clock or external clock.
	STPS	Select number of stop bits.
	PRY, PRYE	Select whether parity is included and whether odd or even.
	IOPOL	Select the TXD/RXD input/output polarity.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	CRS	If $\overline{CTS}$ or $\overline{RTS}$ is used, select which function to use.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{CTS}$ or $\overline{RTS}$ function.
	NCH	Select TXDi pin output mode. (2)
	CKPOL	Set to 0.
	UFORM	LSB first or MSB first can be selected when character bit length is 8 bits. Set to 0 when character bit length is 7 or 9 bits.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UjIRS	Select source of UARTj transmit interrupt.
	UjRRM	Set to 0.
	UiLCH	Set to 1 to use reversed data logic.
	UiERE	Set to 0.
UiSMR	0 to 7	Set to 0.
UiSMR2	0 to 7	Set to 0.
UiSMR3	0 to 7	Set to 0.
UiSMR4	0 to 7	Set to 0.
UCON	U0IRS	Select source of UART0 transmit interrupt.
	U1IRS	Select source of UART1 transmit interrupt.
	U0RRM	Set to 0.
	U1RRM	Set to 0.
	CLKMD0	Invalid because CLKMD1 is 0
	CLKMD1	Set to 0.
	RCSP	Set to 1 to input $\overline{CTS0}$ signal of UART0 from the P6_4 pin.
	7	Set to 0.
IFSR3A	IFSR34	Set to 0 to use UART5 transmit interrupt.
	IFSR36	Set to 0 to use UART6 transmit interrupt.
IFSR2A	IFSR25	Set to 0 to use UART7 transmit interrupt.

i = 0 to 2, 5 to 7 j = 2, 5 to 7

Notes:
1. The bits used for transmit/receive data are as follows: Bits 0 to 6 when character bit length is 7 bits; bits 0 to 7 when character bit length is 8 bits; bits 0 to 8 when character bit length is 9 bits.
2. TXD2 pin is N channel open-drain output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.
3. The contents of bits 7 and 8 are undefined when character bit length is 7 bits.
The contents of bit 8 is undefined when character bit length is 8 bits.

(1) 8-bit Data Transmit Timing (with a Parity and 1 Stop Bit)

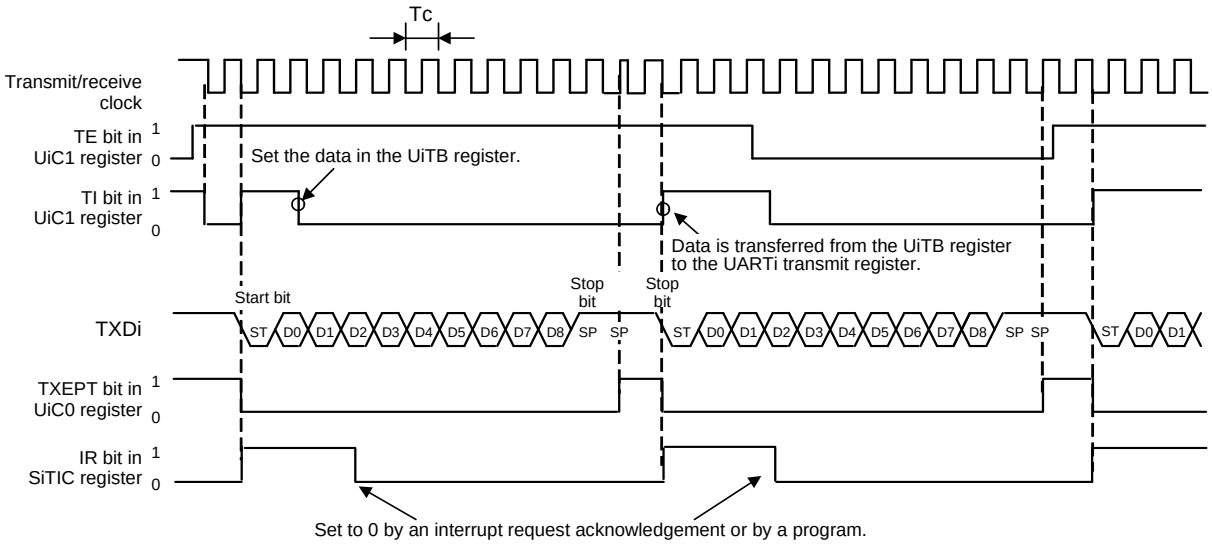


i = 0 to 2, 5 to 7

The above timing diagram applies when the register bits are set as follows:
- The PRYE bit in the UiMR register = 1 (parity enabled)
- The STPS bit in the UiMR register = 0 (1 stop bit)
- The CRD bit in the UiC0 register = 0 (CTS/RTS enabled)
- The CRS bit in the UiC0 register = 0 (CTS selected)
- The UiIRS bit in the UiC1 register = 1 (an interrupt request occurs when transmit completed)

Tc = 16(n + 1)/fj or 16(n + 1)/fEXT
fj : Frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT : Frequency of UiBRG count source (external clock)
n : Value set to UiBRG

(2) 9-bit Data Transmit Timing (with No Parity and 2 Stop Bits)

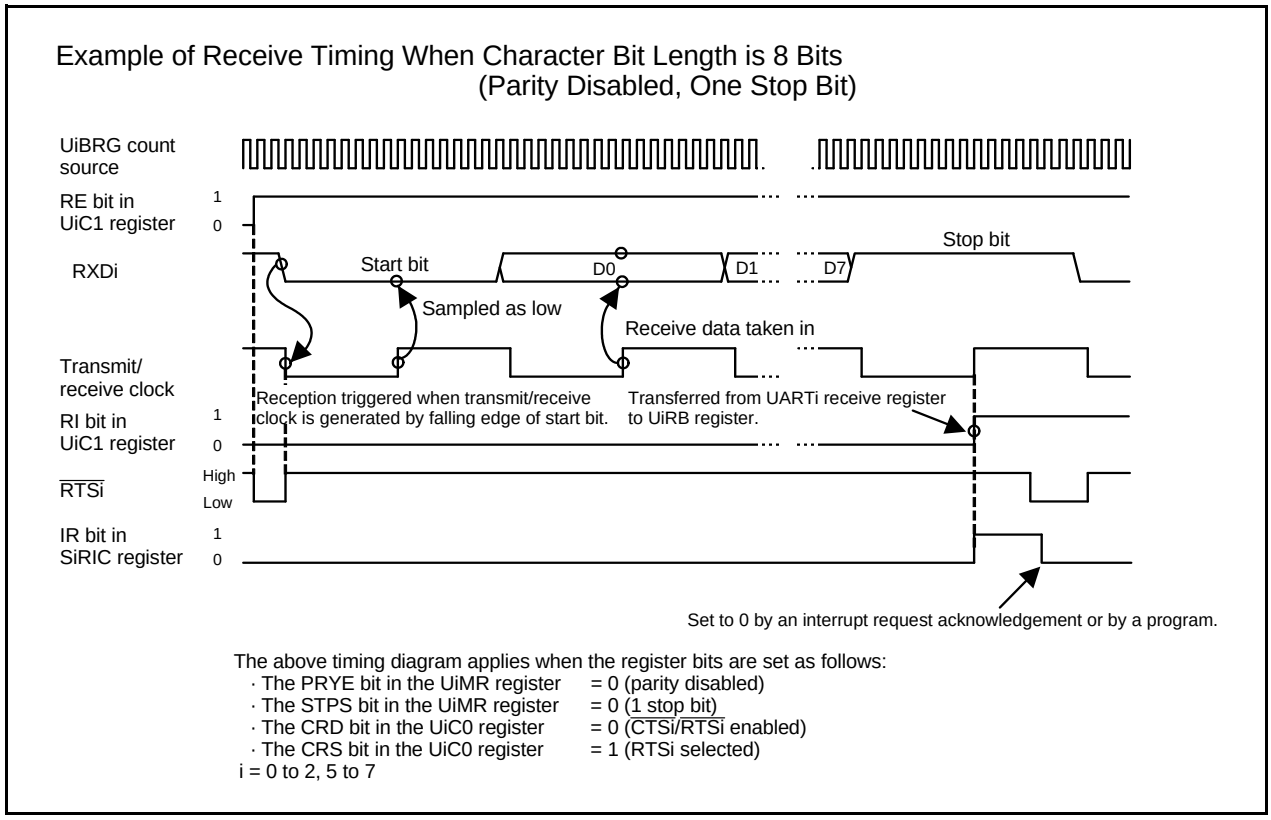


i = 0 to 2, 5 to 7

The above timing diagram applies when the register bits are set as follows:
- The PRYE bit in the UiMR register = 0 (parity disabled)
- The STPS bit in the UiMR register = 1 (2 stop bits)
- The CRD bit in the UiC0 register = 1 (CTS/RTS disabled)
- The UiIRS bit in the UiC1 register = 0 (an interrupt request occurs when transmit buffer becomes empty)

TC = 16(n + 1)/fj or 16(n + 1)/fEXT
fj : Frequency of UiBRG count source (f1SIO, f2SIO, f8SIO, f32SIO)
fEXT: Frequency of UiBRG count source (external clock)
n : Value set to UiBRG

Figure 23.12 Transmit Timing in UART Mode



The above timing diagram applies when the register bits are set as follows:
- The PRYE bit in the UiMR register = 0 (parity disabled)
- The STPS bit in the UiMR register = 0 (1 stop bit)
- The CRD bit in the UiC0 register = 0 ($\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$ enabled)
- The CRS bit in the UiC0 register = 1 (RTSi selected)

i = 0 to 2, 5 to 7

Figure 23.13 Receive Timing in UART Mode

23.3.2.1 Bit Rate

In UART mode, the frequency set by the UiBRG register (i = 0 to 2, 5 to 7) divided by 16 become the bit rate.

The setting value (n) of the UiBRG register is calculated by the following formula.

$$n = \frac{fj}{bitrate(bps) \times 16} - 1$$

fj = f1SIO, f2SIO, f8SIO, f32SIO

n = 00h to FFh

Table 23.13 lists Example Bit Rates and Settings.

Table 23.13 Example Bit Rates and Settings

Bit Rate (bps)	Count Source of UiBRG	Peripheral Function Clock f1: 16 MHz		Peripheral Function Clock f1: 24 MHz	
		Set Value of UiBRG: n	Bit Rate (bps)	Set value of UiBRG: n	Bit Rate (bps)
1200	f8SIO	103 (67h)	1202	155 (9Bh)	1202
2400	f8SIO	51 (33h)	2404	77 (4Dh)	2404
4800	f8SIO	25 (19h)	4808	38 (26h)	4808
9600	f1SIO	103 (67h)	9615	155 (9Bh)	9615
14400	f1SIO	68 (44h)	14493	103 (67h)	14423
19200	f1SIO	51 (33h)	19231	77 (4Dh)	19231
28800	f1SIO	34 (22h)	28571	51 (33h)	28846
31250	f1SIO	31 (1Fh)	31250	47 (2Fh)	31250
38400	f1SIO	25 (19h)	38462	38 (26h)	38462
51200	f1SIO	19 (13h)	50000	28 (1Ch)	51724

Note:

1. This applies when the OCOSEL0 bit or OCOSEL1 bit in the UCLKSEL0 register is 0 (f1).

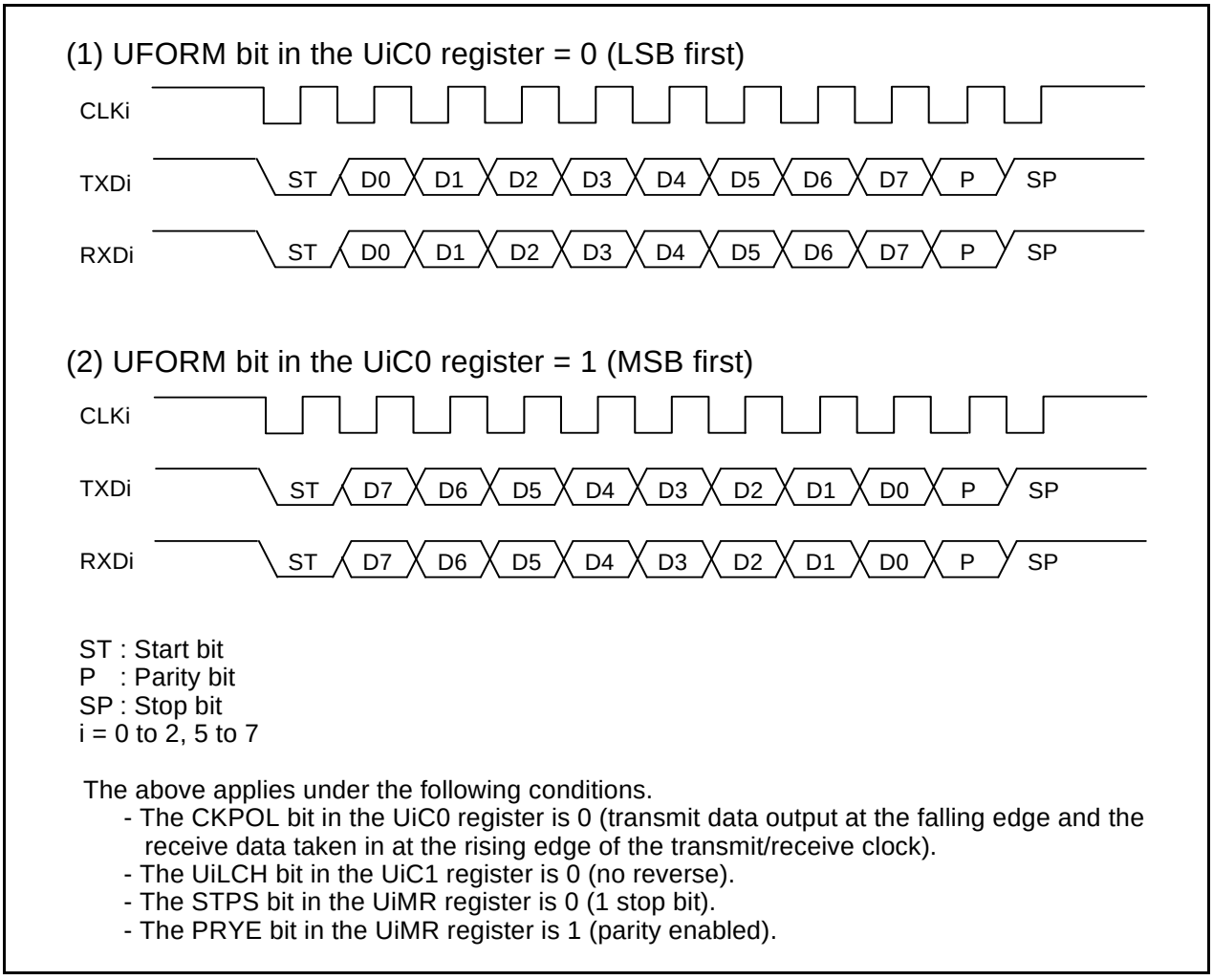
23.3.2.2 Transmit/Receive Register Initialization

When the transmit/receive register needs to be initialized due to an interrupted transmission/reception, follow the procedures below.

- Initializing the UiRB register (i = 0 to 2, 5 to 7)
  (1) Set the RE bit in the UiC1 register to 0 (reception disabled).
  (2) Set the RE bit in the UiC1 register to 1 (reception enabled).
- Initializing the UiTB register
  (1) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
  (2) Reset bits SMD2 to SMD0 in the UiMR register to 001b, 101b, and 110b.
  (3) Set 1 (transmission enabled), regardless of the set value of the TE bit in the UiC1 register.

23.3.2.3 LSB First/MSB First Select Function

As shown in Figure 23.14, the bit order can be selected by using the UFORM bit in the UiC0 register. This function is valid when the character bit length is 8 bits.



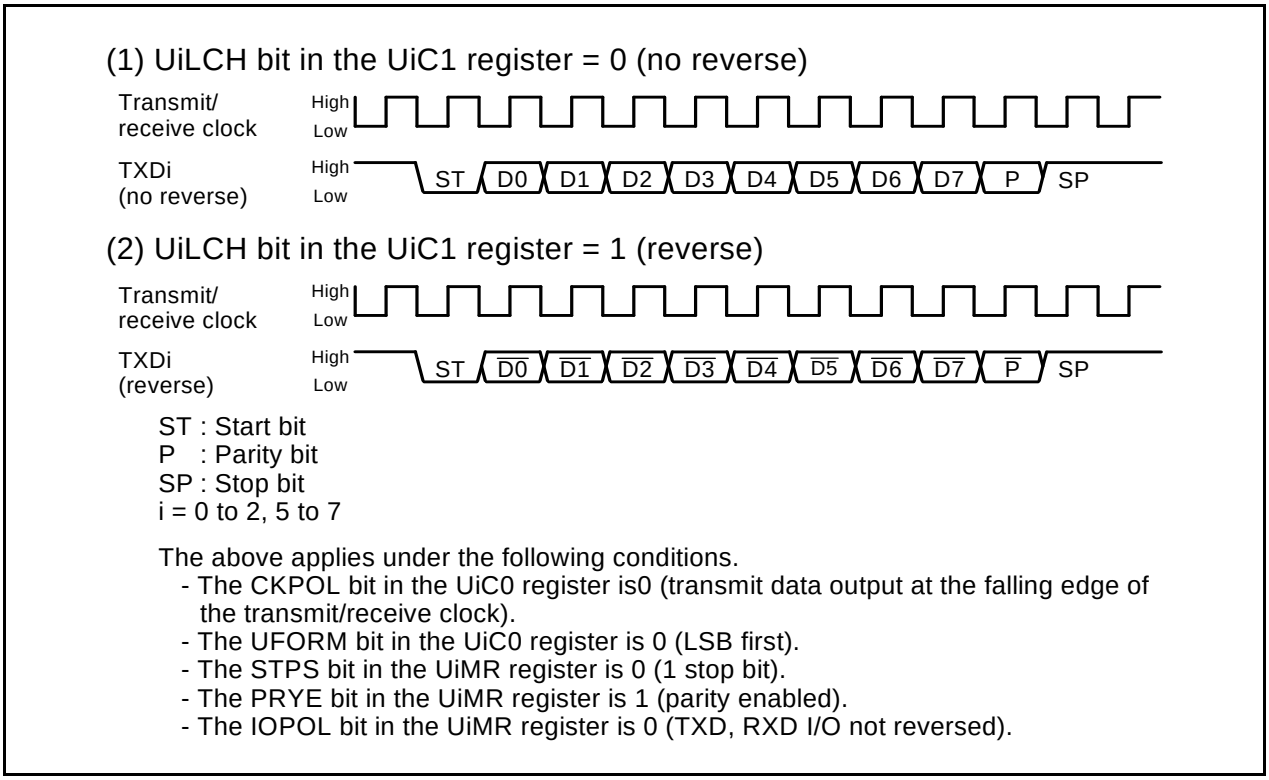
ST : Start bit
P : Parity bit
SP : Stop bit
i = 0 to 2, 5 to 7

The above applies under the following conditions.
- The CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transmit/receive clock).
- The UiLCH bit in the UiC1 register is 0 (no reverse).
- The STPS bit in the UiMR register is 0 (1 stop bit).
- The PRYE bit in the UiMR register is 1 (parity enabled).

Figure 23.14 Bit Order

23.3.2.4 Serial Data Logic Switching Function

The logic of the data written to the UiTB register is reversed and then transmitted. Similarly, the reversed logic of the received data is read when the UiRB register is read. Figure 23.15 shows Serial Data Logic.



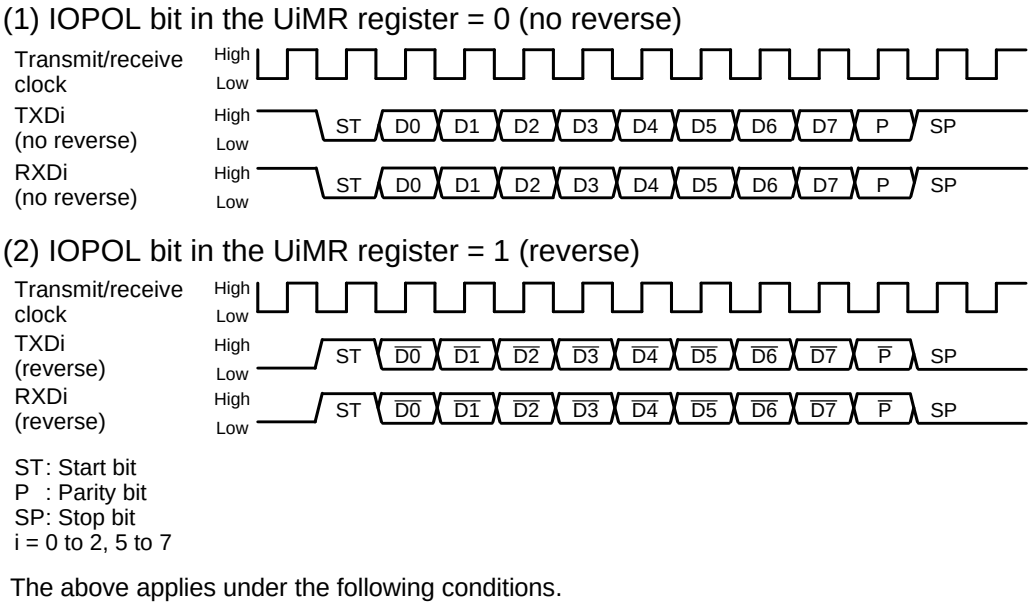
ST : Start bit
P : Parity bit
SP : Stop bit
i = 0 to 2, 5 to 7

The above applies under the following conditions.
- The CKPOL bit in the UiC0 register is0 (transmit data output at the falling edge of the transmit/receive clock).
- The UFORM bit in the UiC0 register is 0 (LSB first).
- The STPS bit in the UiMR register is 0 (1 stop bit).
- The PRYE bit in the UiMR register is 1 (parity enabled).
- The IOPOL bit in the UiMR register is 0 (TXD, RXD I/O not reversed).

Figure 23.15 Serial Data Logic

23.3.2.5 TXD and RXD I/O Polarity Reverse Function

This function reverses the polarities of the TXDi pin output and RXDi pin input. The logic levels of all input/output data (including bits for start, stop, and parity) are reversed. Figure 23.16 shows TXD and RXD I/O Polarity Reversal.



ST: Start bit
P : Parity bit
SP: Stop bit
i = 0 to 2, 5 to 7

The above applies under the following conditions.
- The UFORM bit in the UiC0 register is 0 (LSB first).
- The STPS bit in the UiMR register is 0 (1 stop bit).
- The PRYE bit in the UiMR register is 1 (parity enabled).
- The UiLCH bit in the UiC1 register is 0 (serial data logic not reversed).

Figure 23.16 TXD and RXD I/O Polarity Reversal

23.3.2.6 $\overline{CTS}/\overline{RTS}$ Function

The $\overline{CTS}$ function is used to start transmit operation when a low-level signal is applied to the $\overline{CTSi}$/$\overline{RTSi}$ (i = 0 to 2, 5 to 7) pin. Transmit operation begins when input to the $\overline{CTSi}/\overline{RTSi}$ pin becomes low. If the low-level signal is switched to high during a transmit operation, the operation stops after the ongoing transmit/receive operation is completed.

When the $\overline{RTS}$ function is used, the $\overline{CTSi}/\overline{RTSi}$ pin outputs a low-level signal when the MCU is ready to receive. The output level goes high when a start bit is detected.

Refer to Table 23.10 “I/O Pin Functions in UART Mode”.

23.3.2.7 $\overline{CTS}/\overline{RTS}$ Separate Function (UART0)

This function separates $\overline{CTS0}$ and $\overline{RTS0}$, outputs $\overline{RTS0}$ from the P6_0 pin, and inputs $\overline{CTS0}$ from the P6_4 pin. To use this function, set the register bits as shown below.

- The CRD bit in the U0C0 register= 0 (enable $\overline{CTS}/\overline{RTS}$ of UART0)
- The CRS bit in the U0C0 register= 1 (output $\overline{RTS}$ of UART0)
- The CRD bit in the U1C0 register= 0 (enable $\overline{CTS}/\overline{RTS}$ of UART1)
- The CRS bit in the U1C0 register= 0 (input $\overline{CTS}$ of UART1)
- The RCSP bit in the UCON register= 1 (inputs $\overline{CTS0}$ from the P6_4 pin)
- The CLKMD1 bit in the UCON register= 0 (CLKS1 not used)

Note that when using the $\overline{CTS}/\overline{RTS}$ separate function, $\overline{CTS}/\overline{RTS}$ of UART1 function cannot be used.

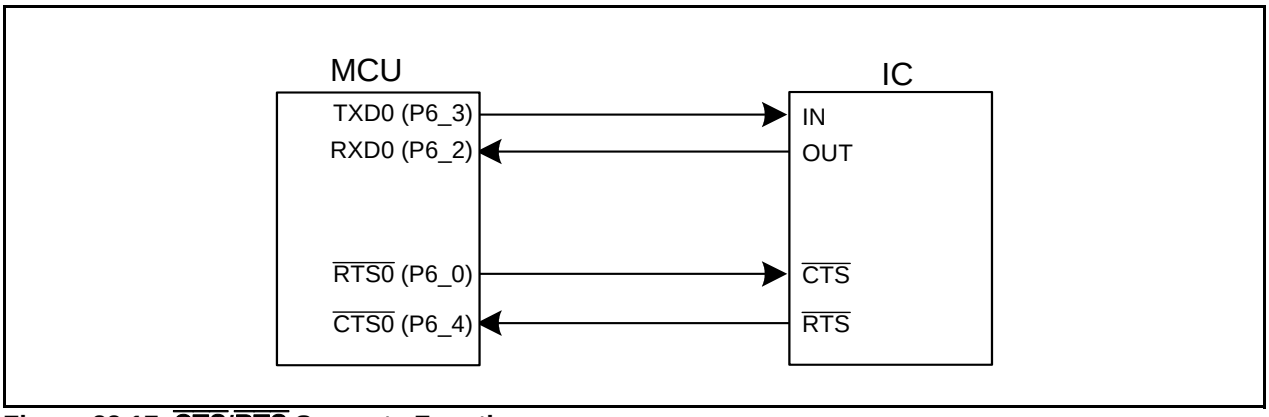


Figure 23.17 $\overline{CTS}/\overline{RTS}$ Separate Function

23.3.3 Special Mode 1 (I^2C mode)

I^2C mode supports the simplified I^2C interface. Table 23.14 lists the specifications of I^2C mode. Table 23.16 and Table 23.17 list the registers used in I^2C mode and the register settings. Table 23.18 lists the I^2C Mode Specifications. Figure 23.18 shows I^2C Mode Block Diagram. Figure 23.19 shows Transfer to UiRB Register and Interrupt Timing.

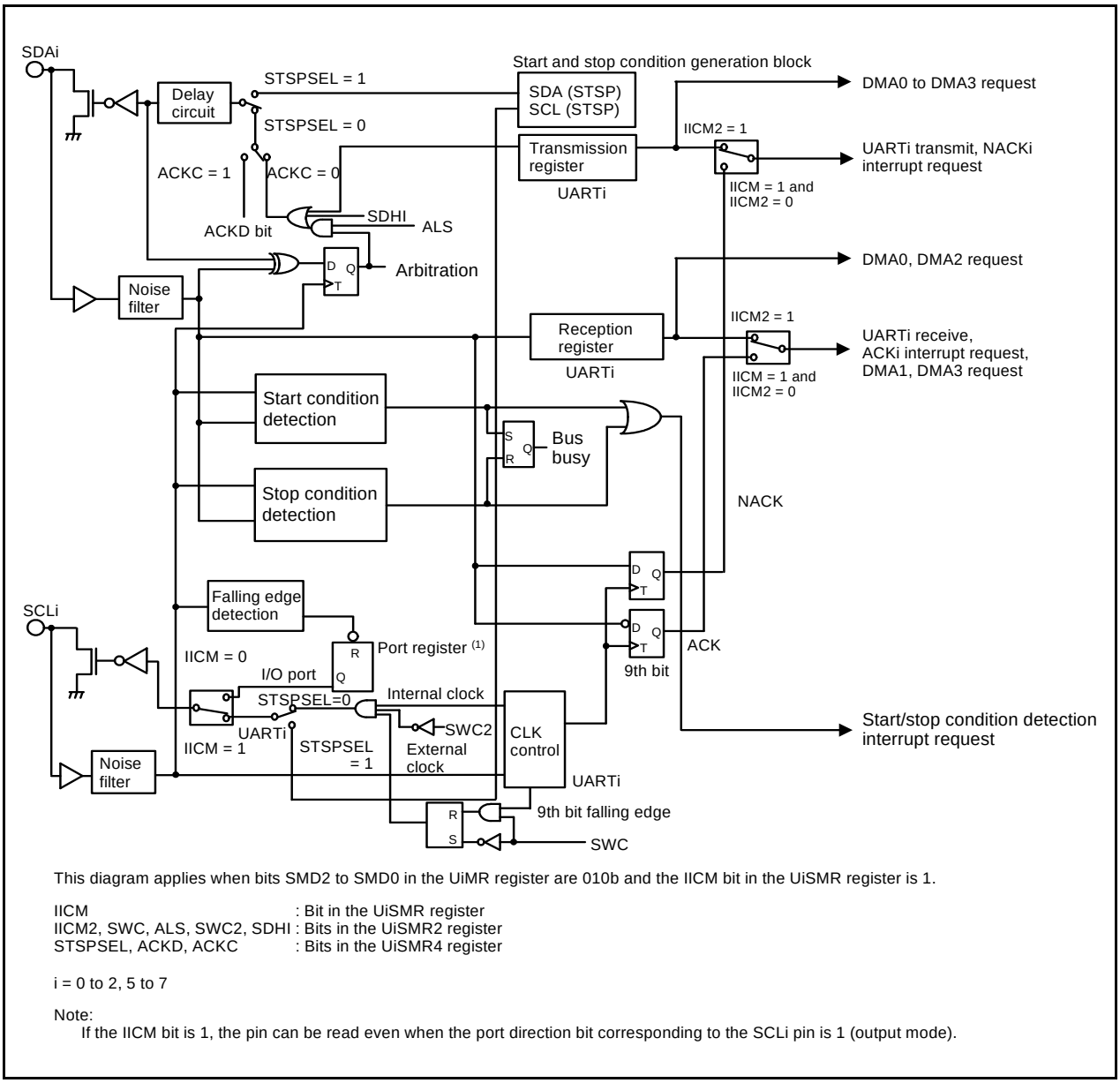
As shown in Table 23.18, the MCU is placed in I^2C mode by setting bits SMD2 to SMD0 to 010b and the IICM bit to 1. Because SDAi transmit output has a delay circuit attached, SDAi output changes its state after SCLi goes low and remains stably low.

Table 23.14 I^2C Mode Specifications

Item	Specification
Data format	Character bit length: 8 bits
Transmit/receive clock	• Master mode CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{2(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n = setting value of the UiBRG register 00h to FFh • Slave mode CKDIR bit = 1 (external clock): Input from the SCLi pin
Transmission start conditions	To start transmission, satisfy the following requirements. (1) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in UiTB register)
Reception start conditions	To start reception, satisfy the following requirements. (1) • The RE bit in the UiC1 register = 1 (reception enabled) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in the UiTB register)
Interrupt request generation timing	Transmission interrupt • Acknowledge undetected or transmit Reception interrupt • Acknowledge undetected or receive Start/stop condition detection interrupt • Start or stop condition detected
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the 8th bit of the unit of next data.
Selectable functions	• Arbitration lost Timing that the ABT bit in the UiRB register is updated can be selected. • SDAi digital delay No digital delay or a delay of 2 to 8 UiBRG count source clock cycles can be selected. • Clock phase setting With or without clock delay can be selected.

i = 0 to 2, 5 to 7

Notes:
1. When an external clock is selected, the conditions must be met while the external clock is in the high state.
2. If an overrun error occurs, the received data of the UiRB register will be undefined.



This diagram applies when bits SMD2 to SMD0 in the UiMR register are 010b and the IICM bit in the UiSMR register is 1.

IICM : Bit in the UiSMR register
IICM2, SWC, ALS, SWC2, SDHI : Bits in the UiSMR2 register
STSPSEL, ACKD, ACKC : Bits in the UiSMR4 register

i = 0 to 2, 5 to 7

Note:
If the IICM bit is 1, the pin can be read even when the port direction bit corresponding to the SCLi pin is 1 (output mode).

Figure 23.18 I²C Mode Block Diagram

Table 23.15 I/O Pin Functions in I²C Mode

Pin Name	I/O	Function
SCLi	Input/output	Clock Input or output
SDAi	Input/output	Data Input or output

i = 0 to 2, 5 to 7

Note:
1. Pins CLKi and $\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$ are not used. (They can be used as I/O ports.)

Table 23.16 Registers Used and Settings in I²C Mode (1/2)

Register	Bits	Function	
		Master	Slave
UiTB	0 to 7	Set transmission data.	Set transmission data.
UiRB (2)	0 to 7	Reception data can be read.	Reception data can be read.
	8	ACK or NACK is set in this bit.	ACK or NACK is set in this bit.
	ABT	Arbitration lost detection flag	Invalid
	OER	Overrun error flag	Overrun error flag
UiBRG	0 to 7	Set a bit rate.	Invalid
UiMR (2)	SMD2 to SMD0	Set to 010b.	Set to 010b.
	CKDIR	Set to 0.	Set to 1.
	IOPOL	Set to 0.	Set to 0.
UiC0	CLK1, CLK0	Select the count source for the UiBRG register.	Invalid
	CRS	Invalid because CRD is 1	Invalid because CRD is 1
	TXEPT	Transmit register empty flag	Transmit register empty flag
	CRD (3)	Set to 1.	Set to 1.
	NCH	Set to 1. (1)	Set to 1. (1)
	CKPOL	Set to 0.	Set to 0.
	UFORM	Set to 1.	Set to 1.
UiC1	TE	Set to 1 to enable transmission.	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag	Transmit buffer empty flag
	RE	Set to 1 to enable reception.	Set to 1 to enable reception.
	RI	Reception complete flag	Reception complete flag
	UjIRS	Set to 1.	Set to 1.
	UjRRM, UiLCH, UiERE	Set to 0.	Set to 0.
UiSMR	IICM	Set to 1.	Set to 1.
	ABC	Select the timing that arbitration lost is detected.	Invalid
	BBS	Bus busy flag	Bus busy flag
	3 to 7	Set to 0.	Set to 0.
UiSMR2	IICM2	See Table 23.18 “I²C Mode Functions”.	See Table 23.18 “I²C Mode Functions”.
	CSC	Set to 1 to enable clock synchronization.	Set to 0.
	SWC	Set to 1 to fix SCLi output to low at the falling edge of the 9th bit of clock.	Set to 1 to fix SCLi output to low at the falling edge of the 9th bit of clock.
	ALS	Set to 1 to stop SDAi output when arbitration lost is detected.	Set to 0.
	STAC	Set to 0.	Set to 1 to initialize UARTi at start condition detection.
	SWC2	Set to 1 to forcibly pull SCLi output low.	Set to 1 to forcibly pull SCLi output low.
	SDHI	Set to 1 to disable SDAi output.	Set to 1 to disable SDAi output.
	7	Set to 0.	Set to 0.

i = 0 to 2, 5 to 7 j = 2, 5 to 7

Notes:
1. The TXD2 pin is N channel open-drain output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.
2. Set the bits not listed above to 0 when writing in I²C mode.
3. when using UART1 in I²C mode, to enable the $\overline{CTS}/\overline{RTS}$ separate function of UART0, set the CRD bit in the U1C0 register to 0 ($\overline{CTS}/\overline{RTS}$ enabled) and the CRS bit to 0 ($\overline{CTS}$ input).

Table 23.17 Registers Used and Settings in I²C Mode (2/2)

Register	Bits	Function	
		Master	Slave
UiSMR3	0, 2, 4 NODC	Set to 0.	Set to 0.
	CKPH	See Table 23.18 "I²C Mode Functions".	See Table 23.18 "I²C Mode Functions".
	DL2 to DL0	Set the amount of SDAi digital delay.	Set the amount of SDAi digital delay.
UiSMR4	STAREQ	Set to 1 to generate start condition.	Set to 0.
	RSTAREQ	Set to 1 to generate restart condition.	Set to 0.
	STPREQ	Set to 1 to generate stop condition.	Set to 0.
	STSPSEL	Set to 1 to output each condition.	Set to 0.
	ACKD	Select ACK or NACK.	Select ACK or NACK.
	ACKC	Set to 1 to output ACK data.	Set to 1 to output ACK data.
	SCLHI	Set to 1 to stop SCLi output when stop condition is detected.	Set to 0.
	SWC9	Set to 0.	Set to 1 to set the SCLi to remain low at the falling edge of the 9th bit of clock.
UCON	U0IRS	Set to 1.	Set to 1.
	U1IRS	Set to 1.	Set to 1.
	U0RRM	Set to 0.	Set to 0.
	U1RRM	Set to 0.	Set to 0.
	CLKMD0	Set to 0.	Set to 0.
	CLKMD1	Set to 0.	Set to 0.
	RCSP	Set to 0.	Set to 0.
	7	Set to 0.	Set to 0.
IFSR3A	IFSR33	Set to 0 when UART5 start and stop condition detection interrupts are used.	Set to 0 when UART5 start and stop condition detection interrupts are used.
	IFSR34	Set to 0 when UART5 NACK interrupt is used.	Set to 0 when UART5 NACK interrupt is used.
	IFSR35	Set to 0 when UART6 start and stop condition detection interrupts are used.	Set to 0 when UART6 start and stop condition detection interrupts are used.
	IFSR36	Set to 0 when UART6 NACK interrupt is used.	Set to 0 when UART6 NACK interrupt is used.
IFSR2A	IFSR24	Set to 0 when UART7 start and stop condition detection interrupts are used.	Set to 0 when UART7 start and stop condition detection interrupts are used.
	IFSR25	Set to 0 when UART7 NACK interrupt is used.	Set to 0 when UART7 NACK interrupt is used.
	IFSR26	Set to 1 when UART0 start and stop condition detection interrupts are used.	Set to 1 when UART0 start and stop condition detection interrupts are used.
	IFSR27	Set to 1 when UART1 start and stop condition detection interrupts are used.	Set to 1 when UART1 start and stop condition detection interrupts are used.

i = 0 to 2, 5 to 7

In I2C mode, the functions and timings vary depending on the combination of the IICM2 bit in the UiSMR2 register and CKPH bit in the UiSMR3 register. Figure 23.19 shows Transfer to UiRB Register and Interrupt Timing. Refer to Figure 23.19 for the timing of transferring to the UiRB register, the bit position of the data stored in the UiRB register, types of interrupts, interrupt requests and DMA request generation timing.

Table 23.18 “I2C Mode Functions” lists comparison of other functions in clock synchronous serial I/O mode with I2C mode.

Table 23.18 I2C Mode Functions

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0 = 001b, IICM = 0)	I2C Mode (SMD2 to SMD0 = 010b, IICM = 1)			
		IICM2 = 0 (NACK/ACK Interrupt)		IICM2 = 1 (UART Transmit/Receive Interrupt)	
		CKPH = 0 (No clock delay)	CKPH = 1 (Clock delay)	CKPH = 0 (No clock delay)	CKPH = 1 (Clock delay)
Start and stop condition detection interrupts	-	Start condition detection or stop condition detection (See Figure 23.21 “STSPSEL Bit Functions”)			
Transmission, NACK interrupt (2)	UARTi transmission Transmission started or completed (selected by UiIRS)	No acknowledgment detection (NACK) Rising edge of SCLi 9th bit		UARTi transmission Rising edge of SCLi 9th bit	UARTi transmission Falling edge of SCLi next to the 9th bit
Reception, ACK interrupt (2)	UARTi reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment detection (ACK) Rising edge of SCLi 9th bit		UARTi reception Falling edge of SCLi 9th bit	
Timing for transferring data from UART reception shift register to UiRB register	CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Rising edge of SCLi 9th bit		Falling edge of SCLi 9th bit	Falling and rising edges of SCLi 9th bit
UARTi transmission output delay	Not delayed	Delayed			
Noise filter width	15 ns	200 ns			
Read RXDi and SCLi pin levels	Possible when the corresponding port direction bit = 0	Always possible no matter how the corresponding port direction bit is set			
Initial value of TXDi and SDAi outputs	CKPOL = 0 (high) CKPOL = 1 (low)	The value set in the port register before setting I2C mode (1)			
Initial and end values of SCLi	-	High	Low	High	Low
DMA1, DMA3 Factor (2)	UARTi reception	Acknowledgment detection (ACK)		UARTi reception Falling edge of SCLi 9th bit	
Read received data	1st to 8th bits of the received data are stored in bits 0 to 7 in the UiRB register.	1st to 8th bits of the received data are stored in bits 7 to 0 in the UiRB register.		1st to 7th bits of the received data are stored in bits 6 to 0 in the UiRB register. 8th bit is stored into bit 8 in the UiRB register.	When reading by reception interrupt, 1st to 7th bits of the received data are stored in bits 6 to 0 in the UiRB register. 8th bit is stored into bit 8 in the UiRB register. When reading by transmission interrupt, 1st to 8th bits are stored into bits 7 to 0 in the UiRB register.

i = 0 to 2, 5 to 7

Notes:

1. Set the initial value of SDAi output while bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).
2. See Figure 23.19 “Transfer to UiRB Register and Interrupt Timing”.

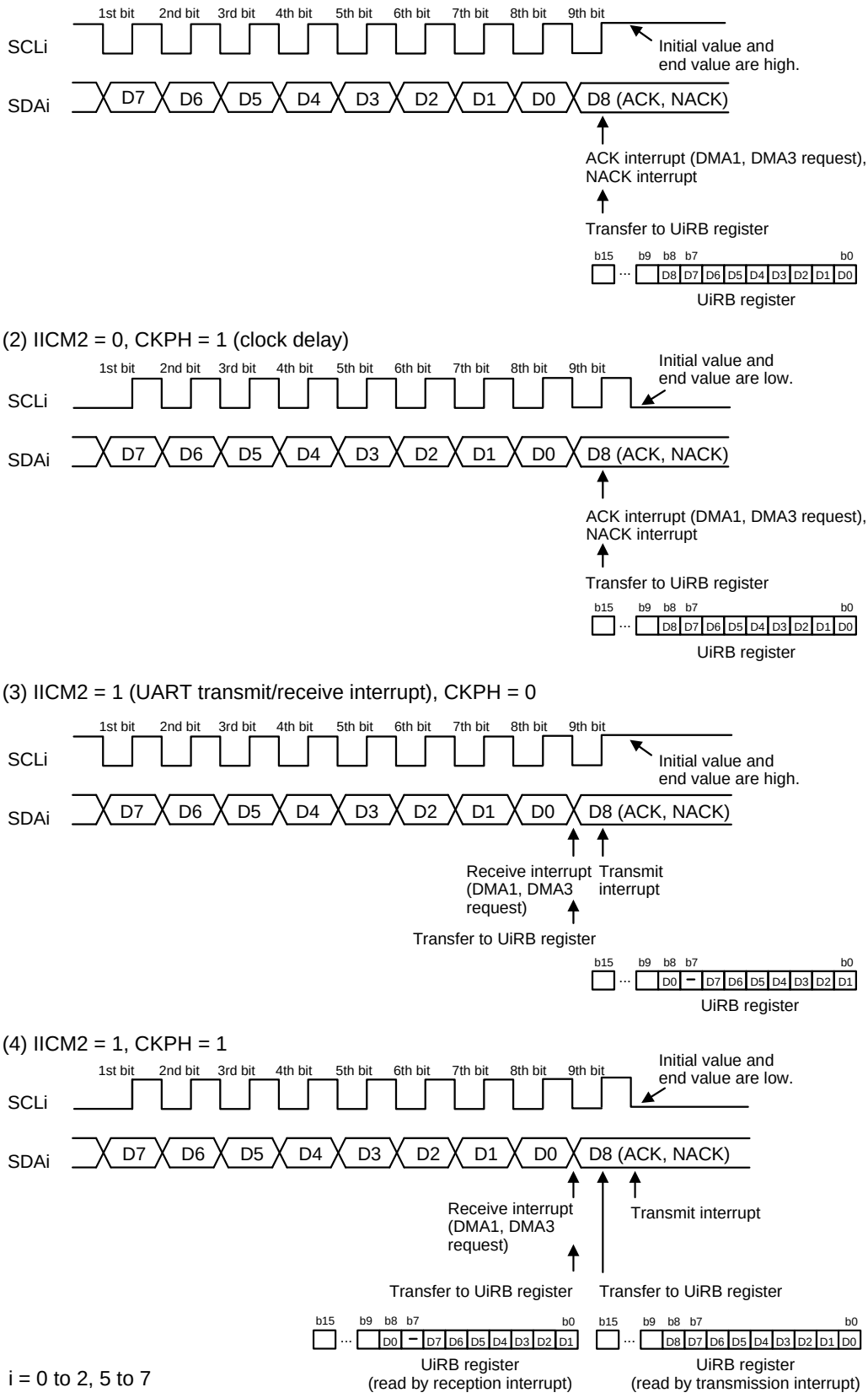


Figure 23.19 Transfer to UiRB Register and Interrupt Timing

23.3.3.1 Detection of Start and Stop Conditions

Whether a start or a stop condition has been detected is determined.
A start condition detect interrupt request is generated when the SDAi pin changes state from high to low while the SCLi pin is in the high state. A stop condition detect interrupt request is generated when the SDAi pin changes state from low to high while the SCLi pin is in the high state.
Because the start and stop condition detect interrupts share an interrupt control register and vector, check the BBS bit in the UiSMR register to determine which interrupt source is requesting the interrupt.

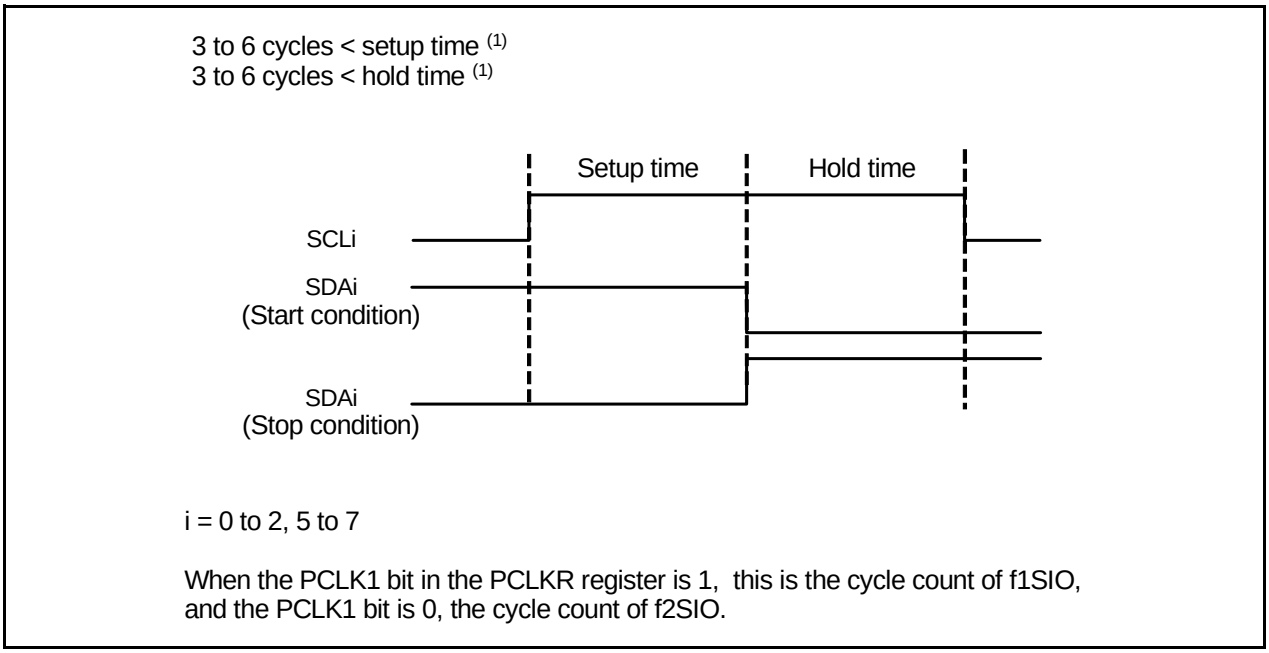


Figure 23.20 Detection of Start and Stop Conditions

23.3.3.2 Output of Start and Stop Conditions

A start condition is generated by setting the STAREQ bit in the UiSMR4 register (i = 0 to 2, 5 to 7) to 1 (start).
A restart condition is generated by setting the RSTAREQ bit in the UiSMR4 register to 1 (start).
A stop condition is generated by setting the STPREQ bit in the UiSMR4 register to 1 (start).
The output procedure is as follows.

(1) Set the STAREQ bit, RSTAREQ bit, or STPREQ bit to 1 (start).
(2) Set the STSPSEL bit in the UiSMR4 register to 1 (output).

The functions of the STSPSEL bit are shown in Table 23.19 and Figure 23.21.

Table 23.19 STSPSEL Bit Functions

Function	STSPSEL = 0	STSPSEL = 1
Output of pins SCLi and SDAi	Output of transmit/receive clock and data Output of start/stop condition is accomplished by a program using ports (not automatically generated in hardware).	Output of a start/stop condition according to bits STAREQ, RSTAREQ, and STPREQ
Start/stop condition interrupt request generation timing	Detection of start/stop condition	Completion of start/stop condition generation

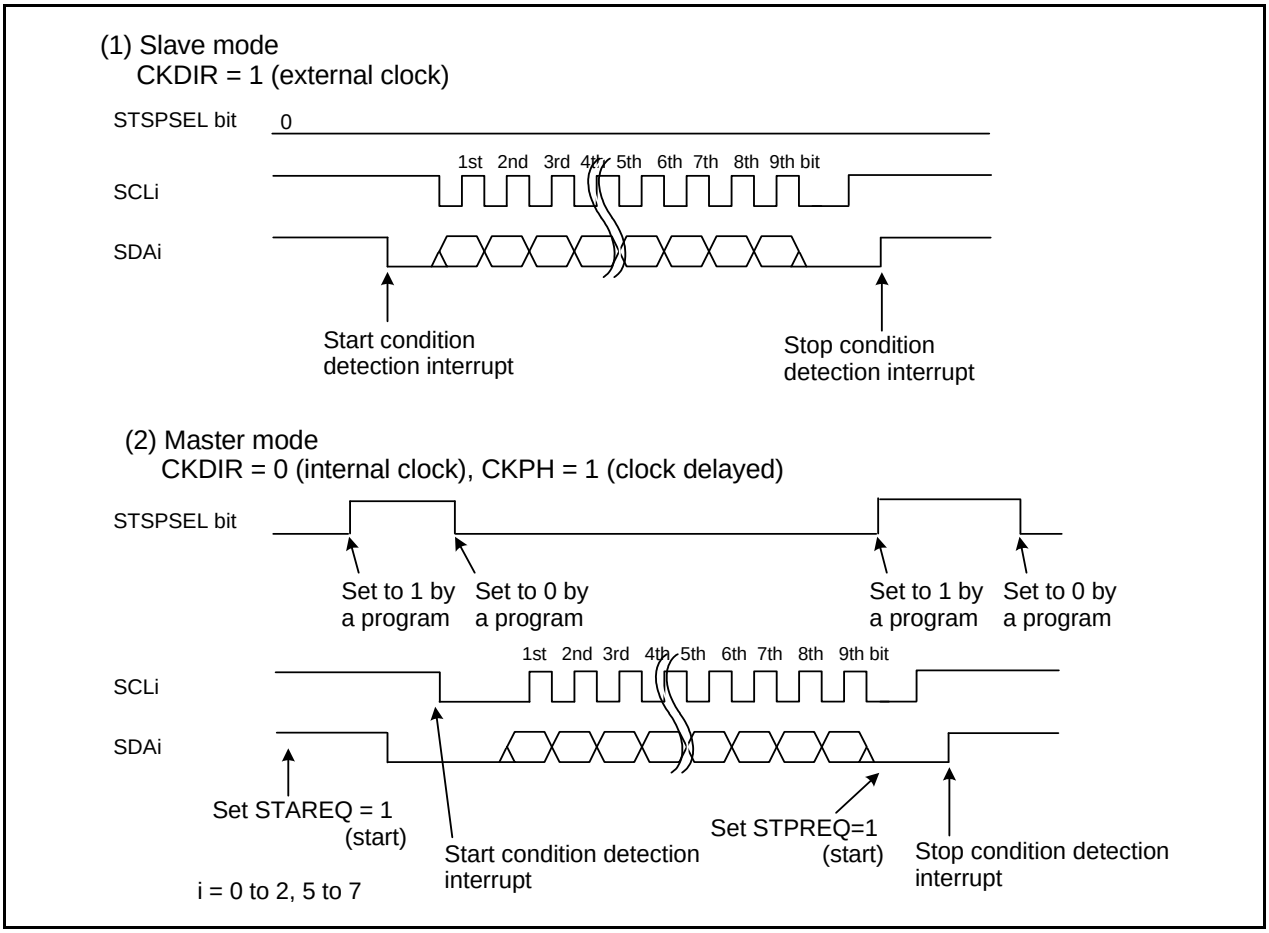


Figure 23.21 STSPSEL Bit Functions

23.3.3.3 Arbitration

Unmatching of the transmit data and SDAi pin input data is checked in synchronization with the rising edge of SCLi. Use the ABC bit in the UiSMR register to select the point at which the ABT bit in the UiRB register is updated. If the ABC bit is 0 (update per bit), the ABT bit is set to 1 at the same time unmatching is detected during check, and is set to 0 when not detected. If the ABC bit is set to 1, if unmatching is ever detected, the ABT bit is set to 1 (unmatching detected) at the falling edge of the clock pulse of the 9th bit. If the ABT bit needs to be updated per byte, set the ABT bit to 0 (undetected) after detecting acknowledge for the first byte, before transmitting/receiving the next byte.

Setting the ALS bit in the UiSMR2 register to 1 (SDA output stop enabled) causes an arbitration-lost to occur, in which case the SDAi pin is placed in the high-impedance state at the same time the ABT bit is set to 1 (unmatching detected).

23.3.3.4 Transmit/Receive Clock

The transmit/receive clock is used to transmit/receive data as is shown in Figure 23.19.

The CSC bit in the UiSMR2 register is used to synchronize an internally generated clock (internal SCLi) and an external clock supplied to the SCLi pin. If the CSC bit is set to 1 (clock synchronization enabled), if a falling edge on the SCLi pin is detected while the internal SCLi is high, the internal SCLi goes low, at which time the value of the UiBRG register is reloaded with and starts counting the low-level intervals. If the internal SCLi changes state from low to high while the SCLi pin is low, counting stops, and when the SCLi pin goes high, counting restarts.

In this way, the UARTi transmit/receive clock is equivalent to AND of the internal SCLi and the clock signal applied to the SCLi pin. The transmit/receive clock works from a half cycle before the falling edge of the internal SCLi 1st bit to the rising edge of the 9th bit. To use this function, select an internal clock for the transmit/receive clock.

The SWC bit in the UiSMR2 register determines whether the SCLi pin is fixed low or freed from low-level output at the falling edge of the 9th clock pulse.

If the SCLHI bit in the UiSMR4 register is set to 1 (enabled), SCLi output is turned off (placed in the high-impedance state) when a stop condition is detected.

When the SWC2 bit in the UiSMR2 register is set to 1 (0 output), a low-level signal can be forcibly output from the SCLi pin even while transmitting or receiving data. When the SWC2 bit is set to 0 (transmit/receive clock), a low-level signal output from the SCLi pin is cancelled, and the transmit/receive clock is input and output.

If the SWC9 bit in the UiSMR4 register is set to 1 (SCL hold low enabled) when the CKPH bit in the UiSMR3 register is 1, the SCLi pin is fixed low at the falling edge of the clock pulse next to the 9th. Setting the SWC9 bit to 0 (SCL hold low disabled) frees the SCLi pin from low-level output.

23.3.3.5 SDA Output

The data written to bits 7 to 0 (D7 to D0) in the UiTB register is output in descending order from D7. The 9th bit (D8) is ACK or NACK.

Set the initial value of SDAi transmit output when IICM is 1 (I^2C mode) and bits SMD2 to SMD0 in the UiMR register are 000b (serial interface disabled).

Bits DL2 to DL0 in the UiSMR3 register allow addition of no delays or a delay of 2 to 8 UiBRG count source clock cycles to the SDAi output.

Setting the SDHI bit in the UiSMR2 register to 1 (SDA output disabled) forcibly places the SDAi pin in the high-impedance state. Do not write to the SDHI bit at the rising edge of the UARTi transmit/receive clock. This is because the ABT bit may inadvertently be set to 1 (detected).

23.3.3.6 SDA Input

When the IICM2 bit is 0, the 1st to 8th bits (D7 to D0) of received data are stored in bits 7 to 0 in the UiRB register. The 9th bit (D8) is ACK or NACK.

When the IICM2 bit is 1, the 1st to 7th bits (D7 to D1) of received data are stored in bits 6 to 0 in the UiRB register and the 8th bit (D0) is stored in bit 8 in the UiRB register. Even when the IICM2 bit is 1, the same data as when the IICM2 bit is 0 can be read, provided the CKPH bit is 1. To read the data, read the UiRB register after the rising edge of 9th bit of the clock.

23.3.3.7 ACK and NACK

If the STSPSEL bit in the UiSMR4 register is set to 0 (start and stop conditions not generated) and the ACKC bit in the UiSMR4 register is set to 1 (ACK data output), the value of the ACKD bit in the UiSMR4 register is output from the SDAi pin.

If the IICM2 bit is 0, a NACK interrupt request is generated if the SDAi pin remains high at the rising edge of the 9th bit of transmit clock pulse. An ACK interrupt request is generated if the SDAi pin is low at the rising edge of the 9th bit of the transmit clock.

If ACKi is selected to generate a DMA1 or DMA3 request source, a DMA transfer can be activated by detection of an acknowledge.

23.3.3.8 Initialization of Transmission/Reception

If a start condition is detected while the STAC bit is 1 (UARTi initialization enabled), the serial interface operates as described below.

- The transmit shift register is initialized, and the contents of the UiTB register are transferred to the transmit shift register. In this way, the serial interface starts sending data when the next clock pulse is applied. However, the UARTi output value does not change state and remains the same as when a start condition was detected until the first bit of data is output in synchronization with the input clock.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit is set to 1 (SCL wait output enabled). Consequently, the SCLi pin is pulled low at the falling edge of the 9th clock pulse.

Note that when UARTi transmission/reception is started using this function, the TI bit does not change state. Select the external clock as the transmit/receive clock to start UARTi transmission/reception with this setting.

23.3.4 Special Mode 2

Special mode 2 supports serial communication between one or multiple master devices and multiple slaves devices. The transmit/receive clock polarity and phase are selectable. Table 23.20 lists the Special Mode 2 Specifications.

Table 23.20 Special Mode 2 Specifications

Item	Specification
Data format	Character data length: 8 bits
Transmit/receive clock	• Master mode The CKDIR bit in the UiMR register = 0 (internal clock): $\frac{fj}{2(n+1)}$ fj = f1SIO, f2SIO, f8SIO, f32SIO n: Setting value of UiBRG register 00h to FFh • Slave mode The CKDIR bit = 1 (external clock selected): Input from the CLKi pin
Transmit/receive control	Controlled by input/output ports
Transmission start Conditions	To start transmission, satisfy the following requirements. (1) • The TE bit in the UiC1 register = 1 (transmission enabled) • The TI bit in the UiC1 register = 0 (data present in UiTB register)
Reception start Conditions	To start reception, satisfy the following requirements. (1) • The RE bit in the UiC1 register = 1 (reception enabled) • The TE bit = 1 (transmission enabled) • The TI bit = 0 (data present in the UiTB register)
Interrupt request generation timing	Transmit interrupt: One of the following can be selected. • The UiIRS bit in the UiC1 register= 0 (transmit buffer empty): When transferring data from the UiTB register to the UARTi transmit register (at start of transmission) • The UiIRS bit =1 (transmission completed): When the serial interface completed sending data from the UARTi transmit register Receive interrupt: • When transferring data from the UARTi receive register to the UiRB register (at completion of reception)
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Data input/output can be chosen to occur synchronously with the rising or the falling edge of the transmit/receive clock. • LSB first, MSB first selection Whether to start sending/receiving data beginning with bit 0 or beginning with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the UiRB register. • Switching serial data logic This function reverses the logic value of the transmit/receive data. • Clock phase setting Selectable from four combinations of transmit/receive clock polarities and phases

i = 0 to 2, 5 to 7

Notes:

1. When an external clock is selected, either of the following conditions must be met. If the CKPOL bit in the UiC0 register is 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transmit/receive clock), the external clock is in high state; if the CKPOL bit is 1 (transmit data output at the rising edge and the receive data taken in at the falling edge of the transmit/receive clock), the external clock is in low state.
2. If an overrun error occurs, the received data of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

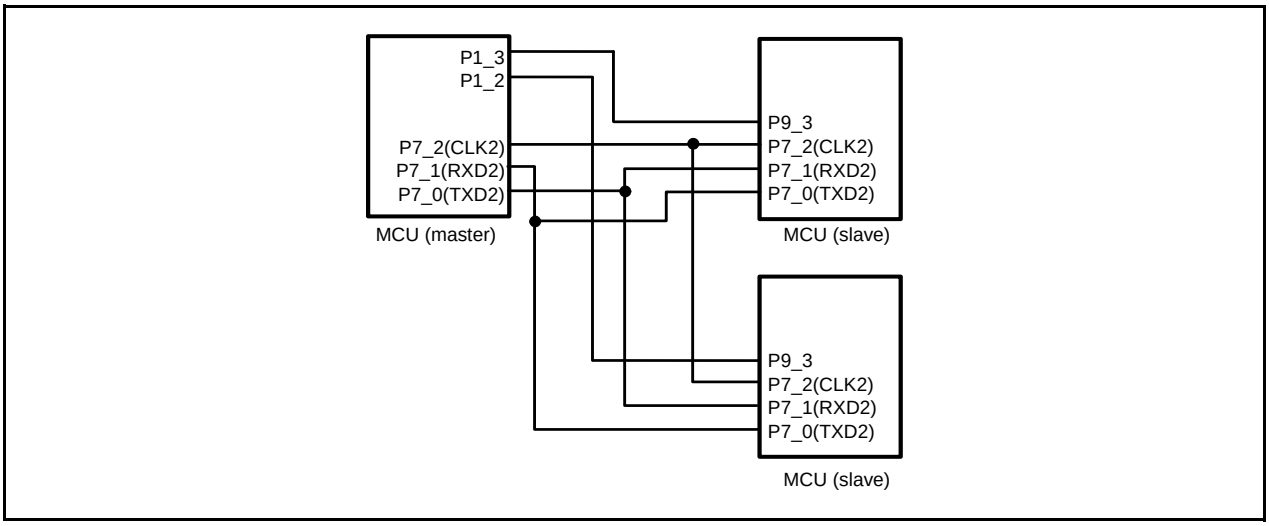


Figure 23.22 Serial Bus Communication Control Example (UART2)

Table 23.21 I/O Pin Functions in Special Mode 2

Pin Name	I/O	Function	Method of Selection
CLKi	Output	Clock output	The CKDIR bit in the UiMR register = 0
	Input	Clock input	The CKDIR bit in the UiMR register = 1 Set the port direction bits sharing pins to 0.
TXDi	Output	Serial data output	(Dummy data output when performing reception only.)
RXDi	Input	Serial data input	Set the port direction bits sharing pins to 0.
	Input	Input port	Set the port direction bits sharing pins to 0. (can be used as an input port when performing transmission only)

i = 0 to 2, 5 to 7

Pins CLKi and $\overline{\text{CTSi}}$/$\overline{\text{RTSi}}$ are not used. (They can be used as I/O ports.)

Table 23.22 Registers Used and Settings in Special Mode 2

Register	Bits	Function
UiTB (1)	0 to 7	Set transmission data.
UiRB (2)	0 to 7	Reception data can be read.
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate.
UiMR (2)	SMD2 to SMD0	Set to 001b.
	CKDIR	Set to 0 in master mode or 1 in slave mode.
	IOPOL	Set to 0.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	CRS	Invalid because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select TXDi pin output format. (1)
	CKPOL	Clock phases can be set in combination with the CKPH bit in the UiSMR3 register.
	UFORM	Select the LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UjIRS	Select UARTj transmit interrupt source.
	UjRRM	Set to 1 to use continuous receive mode.
	UiLCH	Set to 1 to use inverted data logic.
	UiERE	Set to 0.
UiSMR	0 to 7	Set to 0.
UiSMR2	0 to 7	Set to 0.
UiSMR3	CKPH	Clock phases can be set in combination with the CKPOL bit in the UiC0 register.
	NODC	Set to 0.
	0, 2, 4 to 7	Set to 0.
UiSMR4	0 to 7	Set to 0.
UCON	U0IRS	Select UART0 transmit interrupt source.
	U1IRS	Select UART1 transmit interrupt source.
	U0RRM	Set to 1 to use continuous receive mode.
	U1RRM	Set to 1 to use continuous receive mode.
	CLKMD0	Invalid because CLKMD1 is 0
	CLKMD1, RCSP, 7	Set to 0.
IFSR3A	IFSR34	Set to 0 to use UART5 transmit interrupt.
	IFSR36	Set to 0 to use UART6 transmit interrupt.
IFSR2A	IFSR25	Set to 0 to use UART7 transmit interrupt.

i = 0 to 2, 5 to 7 j = 2, 5 to 7

Notes:

1. The TXD2 pin is N channel open-drain output. No NCH bit in the U2C0 register is assigned. Only write 0 to this bit.
2. Set the bits not listed above to 0 when writing to the registers in special mode 2.

23.3.4.1 Clock Phase Setting Function

One of four combinations of transmit/receive clock phases and polarities can be selected using the CKPH bit in the UiSMR3 register and the CKPOL bit in the UiC0 register.

Make sure the transmit/receive clock polarity and phase are the same for the master and salve devices to be used for communication.

Figure 23.23 shows the Transmission and Reception Timing in Master Mode (Internal Clock).

Figure 23.24 shows the Transmission and Reception Timing (CKPH = 0) in Slave Mode (External Clock) while Figure 23.25 shows the Transmission and Reception Timing (CKPH = 1) in Slave Mode (External Clock).

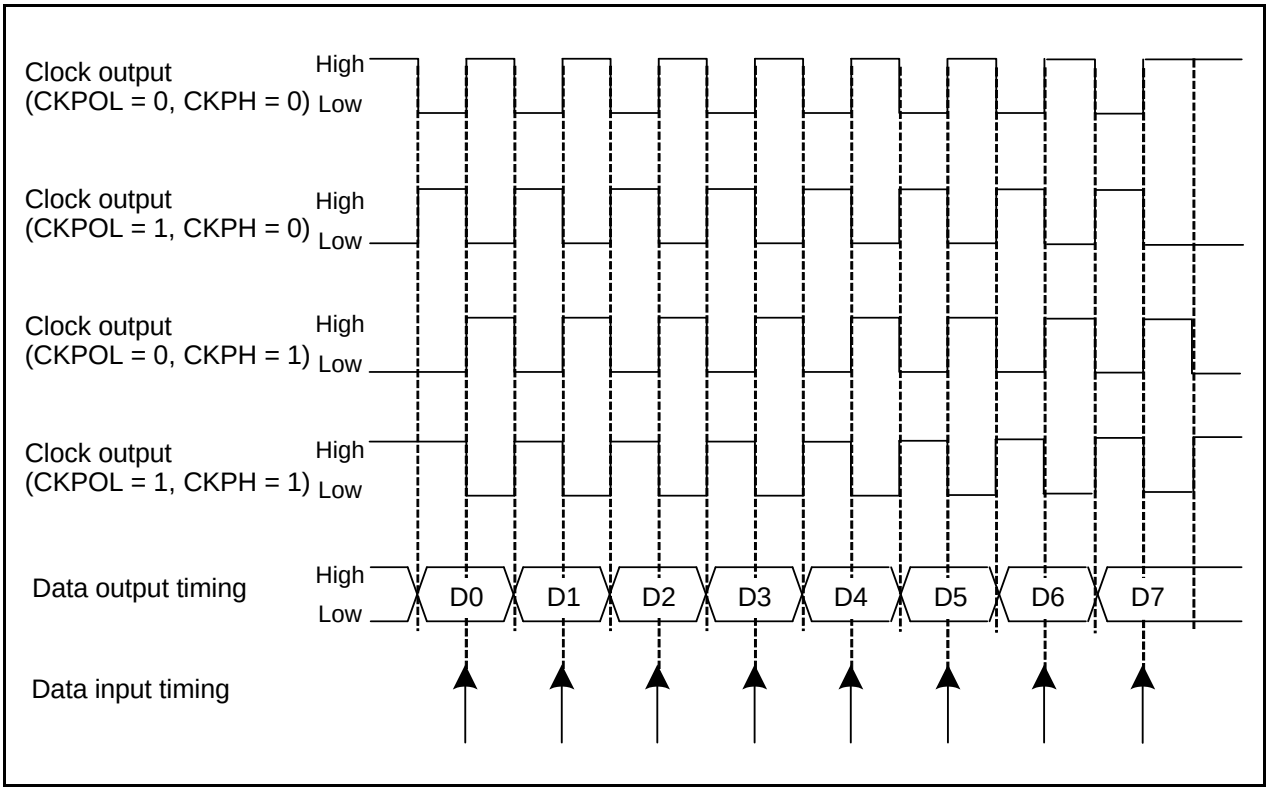
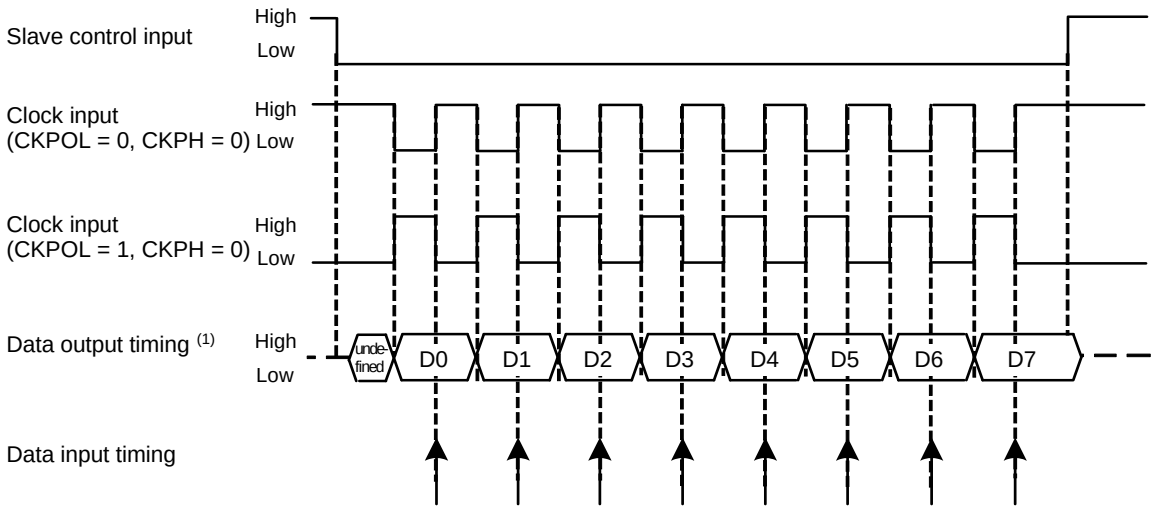
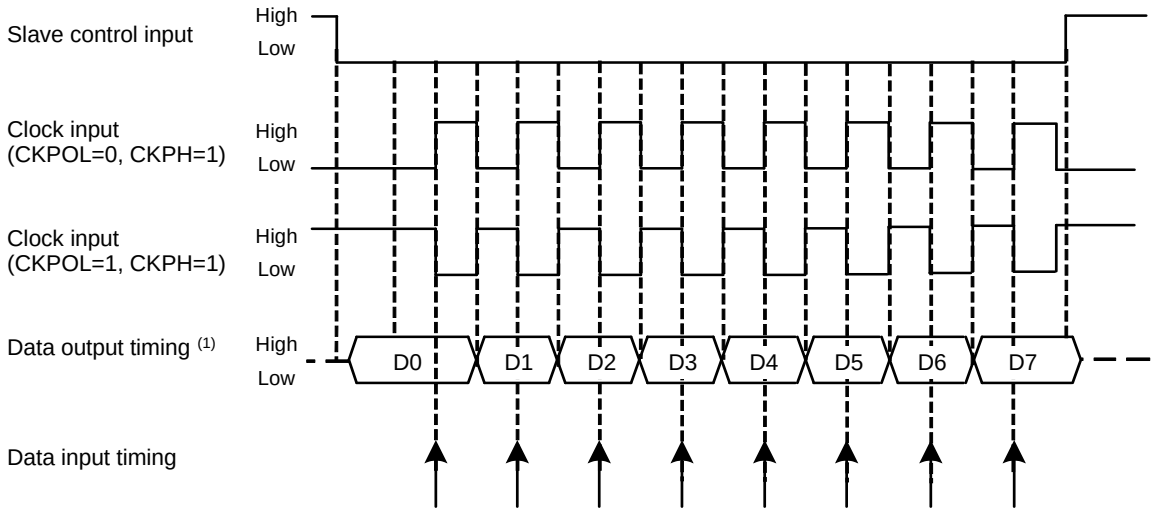


Figure 23.23 Transmission and Reception Timing in Master Mode (Internal Clock)



Note:
1. UART2 output is N-channel open-drain and must be pulled-up externally.

Figure 23.24 Transmission and Reception Timing (CKPH = 0) in Slave Mode (External Clock)



Note:
1. UART2 output is N-channel open-drain and must be pulled-up externally.

Figure 23.25 Transmission and Reception Timing (CKPH = 1) in Slave Mode (External Clock)

23.3.5 Special Mode 3 (IE mode)

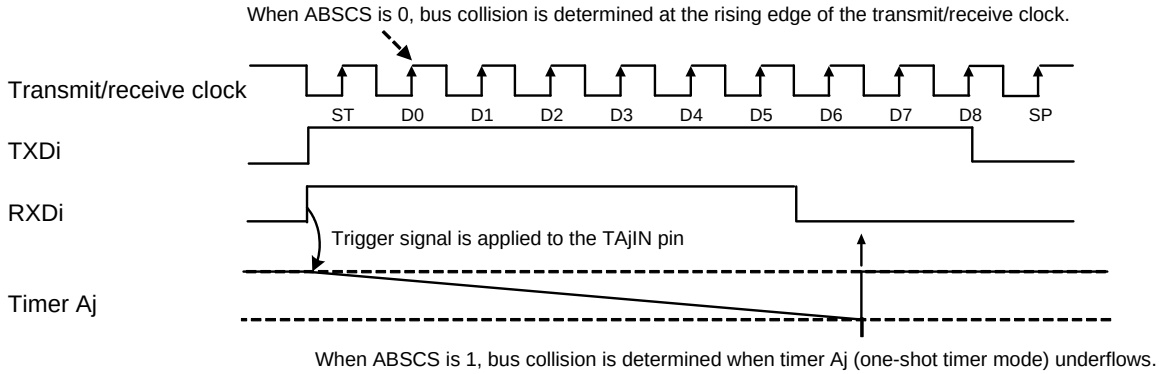
In this mode, one bit of IEBus is approximated by one byte of UART mode waveform.
Table 23.23 lists the Registers Used and Settings in IE Mode. Figure 23.26 shows the Bus Collision Detect Function-Related Bits.
If the TXDi pin (i = 0 to 2, 5 to 7) output level and RXDi pin input level do not match, a UARTi bus collision detect interrupt request is generated.
Use bits IFSR26 and IFSR27 in the IFSR2A register to enable the UART0/UART1 bus collision detect function.

Table 23.23 Registers Used and Settings in IE Mode

Register	Bits	Function
UiTB	0 to 8	Set transmission data.
UiRB (3)	0 to 8	Reception data can be read.
	OER, FER, PER, SUM	Error flag
UiBRG	0 to 7	Set bit rate.
UiMR	SMD2 to SMD0	Set to 110b.
	CKDIR	Select internal clock or external clock.
	STPS	Set to 0.
	PRY	Invalid because PRYE is 0
	PRYE	Set to 0.
	IOPOL	Select the TXD and RXD input/output polarity.
UiC0	CLK1, CLK0	Select the count source for the UiBRG register.
	CRS	Invalid because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select TXDi pin output format. (2)
	CKPOL	Set to 0.
	UFORM	Set to 0.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	UjIRS (1)	Select the source of UARTj transmit interrupt.
	UjRRM (1), UiLCH, UiERE	Set to 0.
UiSMR	0 to 3, 7	Set to 0.
	ABSCS	Select the sampling timing to detect a bus collision.
	ACSE	Set to 1 to use the auto clear function of transmit enable bit.
	SSS	Select the transmit start condition.
UiSMR2	0 to 7	Set to 0.
UiSMR3	0 to 7	Set to 0.
UiSMR4	0 to 7	Set to 0.
IFSR2A	IFSR26, IFSR27	Set to 1.
UCON	U0IRS, U1IRS	Select the source of UART0/UART1 transmit interrupt.
	U0RRM, U1RRM	Set to 0.
	CLKMD0	Invalid because CLKMD1 is 0
	CLKMD1, RCSP, 7	Set to 0.

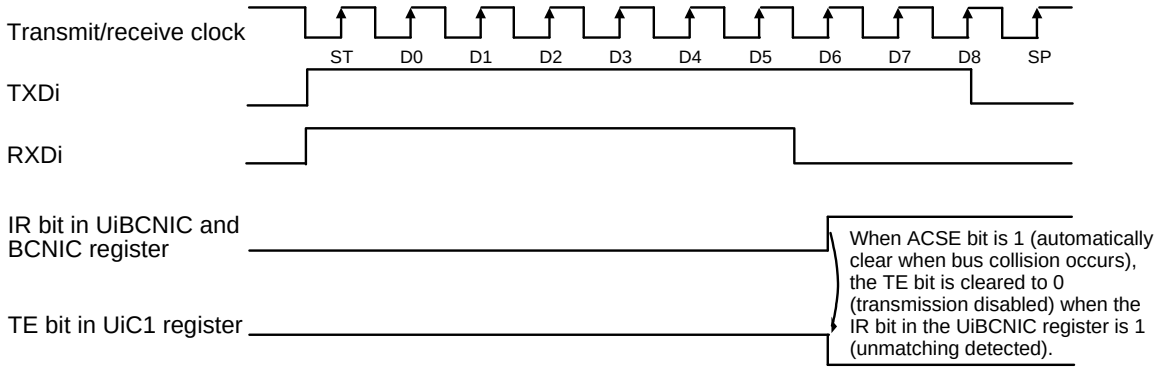
i = 0 to 2, 5 to 7
Notes:
1. Set bits 4 and 5 in registers U0C0 and U1C1 to 0. Bits U0IRS, U1IRS, U0RRM, and U1RRM are in the UCON register.
2. The TXD2 pin is N channel open-drain output. Nothing is assigned in the NCH bit in the U2C0 register. If necessary, set to 0.
3. Set the bits not listed above to 0 when writing to the registers in IE mode.

(1) ABSCS bit in UiSMR register (bus collision detect sampling clock select) (i = 0 to 2, 5 to 7)



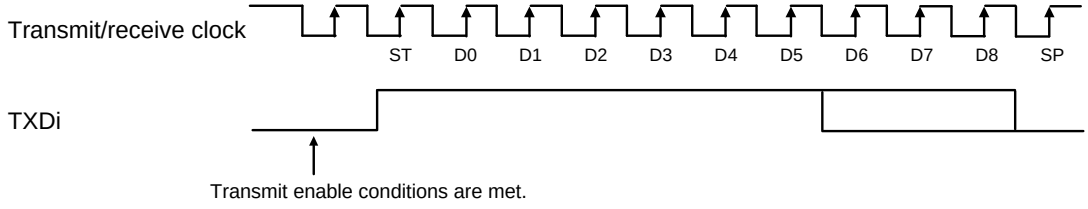
Timer Aj: Timer A3 in UART0; timer A4 in UART1; timer A0 in UART2
timer A0 in UART5; timer A3 in UART6; timer A4 in UART7

(2) ACSE bit in UiSMR register (auto clear of transmit enable bit)

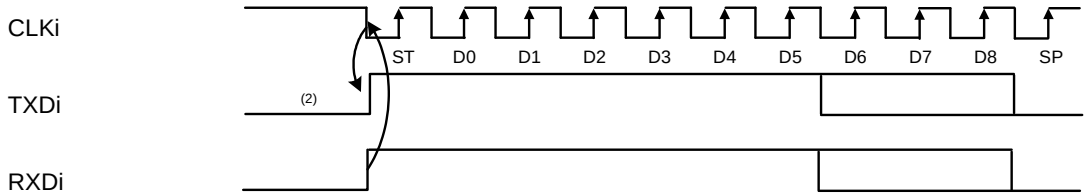


(3) SSS bit in the UiSMR register (transmit start condition select)

When SSS bit is 0, the serial interface starts sending data one transmit/receive clock cycle after the transmission enable condition is met.



When SSS bit is 1, the serial interface starts sending data at the rising edge of RXDi. (1)



Notes :
1. The falling edge of RXDi when IOPOL is 0; the rising edge of RXDi when IOPOL is 1.
2. The transmit conditions must be met before the falling edge of RXD.

The above diagram applies when IOPOL is 1 (reversed). i = 0 to 2, 5 to 7

Figure 23.26 Bus Collision Detect Function-Related Bits

23.3.6 Special Mode 4 (SIM Mode) (UART2)

SIM interface devices can communicate in UART mode. Both direct and inverse formats are available. The TXD2 pin outputs a low-level signal when a parity error is detected.
Table 23.24 lists the SIM Mode Specifications. Table 23.25 lists the Registers Used and Settings in SIM Mode.

Table 23.24 SIM Mode Specifications

Item	Specification
Data formats	• Direct format • Inverse format
Transmit/receive clock	• The CKDIR bit in the U2MR register = 0 (internal clock): fi/(16(n + 1)) fi = f1SIO, f2SIO, f8SIO, f32SIO n = Setting value of the U2BRG register 00h to FFh • The CKDIR bit = 1 (external clock): fEXT/(16(n + 1)) fEXT = input from the CLK2 pin n = Setting value of the U2BRG register 00h to FFh
Transmission start conditions	To start transmission, satisfy the following requirements. • The TE bit in the U2C1 register = 1 (transmission enabled) • The TI bit in the U2C1 register = 0 (data present in the U2TB register)
Reception start conditions	To start reception, satisfy the following requirements. • The RE bit in the U2C1 register = 1 (reception enabled) • Start bit detection
Interrupt request generation timing (2)	• Transmission When the serial interface completed sending data from the UART2 transmit register (the U2IRS bit =1) • Reception When transferring data from the UART2 receive register to the U2RB register (at completion of reception)
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the bit one before the last stop bit of the next unit of data. • Framing error (3) This error occurs when the number of stop bits set is not detected. • Parity error (3) During reception, if a parity error is detected, parity error signal is output from the TXD2 pin. During transmission, a parity error is detected by the level of input to the RXD2 pin when a transmission interrupt occurs. • Error sum flag This flag is set to 1 when an overrun, framing, or parity error occurs.

Notes:
1. If an overrun error occurs, the received data of the U2RB register will be undefined. The IR bit in the S2RIC register remains unchanged.
2. After reset, a transmit interrupt request is generated by setting the U2IRS bit to 1 (transmission completed) and the U2ERE bit to 1 (error signal output) in the U2C1 register. Therefore, when using SIM mode, set the IR bit to 0 (interrupt not requested) after setting the bits.
3. The timing that the framing error flag and the parity error flag are set is detected when data is transferred from the UART2 receive register to the U2RB register.

Table 23.25 Registers Used and Settings in SIM Mode

Register	Bits	Function
U2TB (1)	0 to 7	Set transmission data.
U2RB (1)	0 to 7	Reception data can be read.
	OER,FER,PER,SUM	Error flag
U2BRG	0 to 7	Set bit rate.
U2MR	SMD2 to SMD0	Set to 101b.
	CKDIR	Select the internal clock or external clock.
	STPS	Set to 0.
	PRY	Set to 1 in direct format or 0 in inverse format.
	PRYE	Set to 1.
	IOPOL	Set to 0.
U2C0	CLK0,CLK1	Select the count source for the U2BRG register.
	CRS	Invalid because CRD is 1
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Set to 0.
	CKPOL	Set to 0.
	UFORM	Set to 0 in direct format or 1 in inverse format.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Reception complete flag
	U2IRS	Set to 1.
	U2RRM	Set to 0.
	U2LCH	Set to 0 in direct format or 1 in inverse format.
	U2ERE	Set to 1.
U2SMR (1)	0 to 3	Set to 0.
U2SMR2	0 to 7	Set to 0.
U2SMR3	0 to 7	Set to 0.
U2SMR4	0 to 7	Set to 0.

Note:
1. Set the bits not listed above to 0 when writing to the registers in SIM mode.

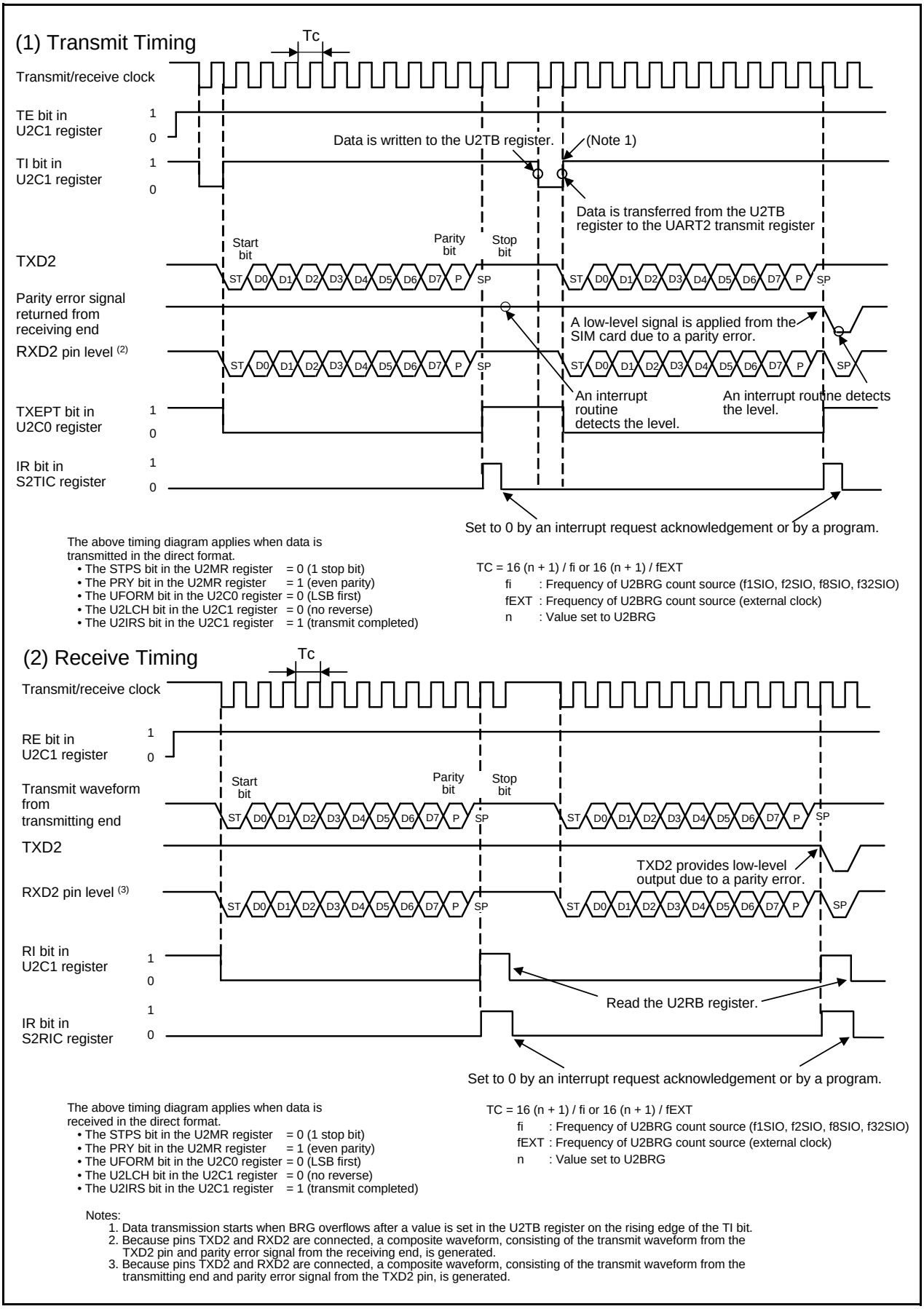


Figure 23.27 Transmit/Receive Timing in SIM Mode

Figure 23.28 shows an Example of SIM Interface Connection. Connect TXD2 and RXD2, and then connect a pull-up resistor.

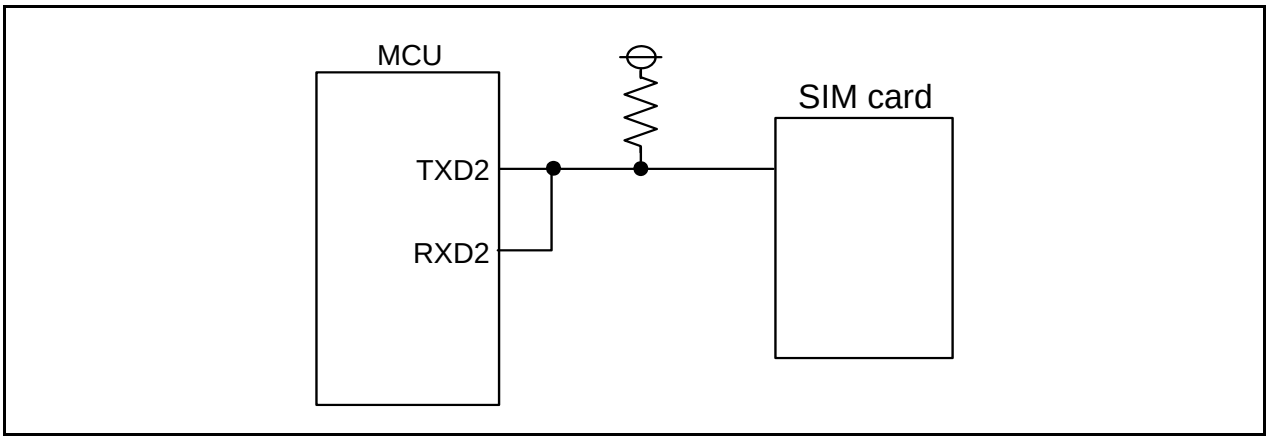


Figure 23.28 Example of SIM Interface Connection

23.3.6.1 Parity Error Signal Output

The parity error signal is enabled by setting the U2ERE bit in the U2C1 register to 1 (error signal output).

The parity error signal is output when a parity error is detected while receiving data. A low-level signal is output from the TXD2 pin in the timing shown in Figure 23.29. If the U2RB register is read while outputting a parity error signal, the PER bit is cleared to 0 (no parity error) and at the same time the TXD2 output again goes high.

When transmitting, a transmission complete interrupt request is generated at the falling edge of the transmit/receive pulse that immediately follows the stop bit. Therefore, whether or not a parity error signal has been returned can be determined by reading the port that shares the RXD2 pin in a transmission complete interrupt routine.

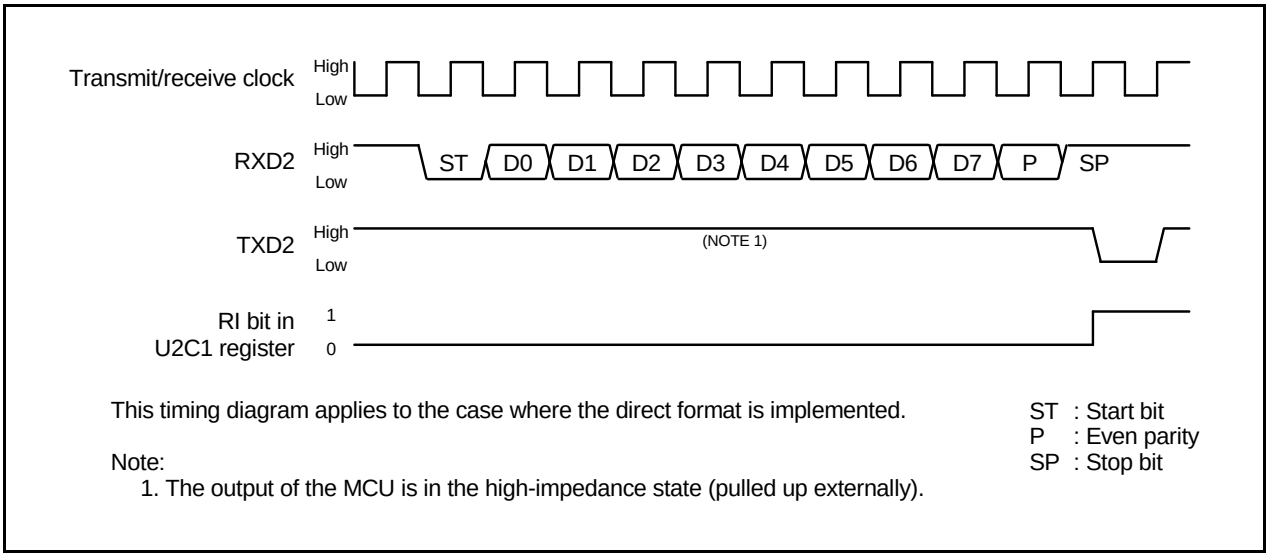


Figure 23.29 Parity Error Signal Output Timing

23.3.6.2 Format

Two formats are available: direct format and inverse format.

For direct format, set the PRYE bit in the U2MR register to 1 (parity enabled), the PRY bit to 1 (even parity), the UFORM bit in the U2C0 register to 0 (LSB first) and the U2LCH bit in the U2C1 register to 0 (not inverted). When data is transmitted, the contents of the U2TB register are transmitted with the even-numbered parity, starting from D0. When data is received, the receive data are stored in the U2RB register, starting from D0. The even-numbered parity is used to determine when a parity error occurs.

For inverse format, set the PRYE bit to 1, the PRY bit to 0 (odd parity), the UFORM bit to 1 (MSB first), and the U2LCH bit to 1 (inverted). When data is transmitted, the contents of the U2TB register are logically inverted and are transmitted with odd-numbered parity, starting from D7. When data is received, the receive data is logically inverted and stored in the U2RB register, starting from D7. The odd-numbered parity is used to determine when a parity error occurs.

Figure 23.30 shows SIM Interface Format.

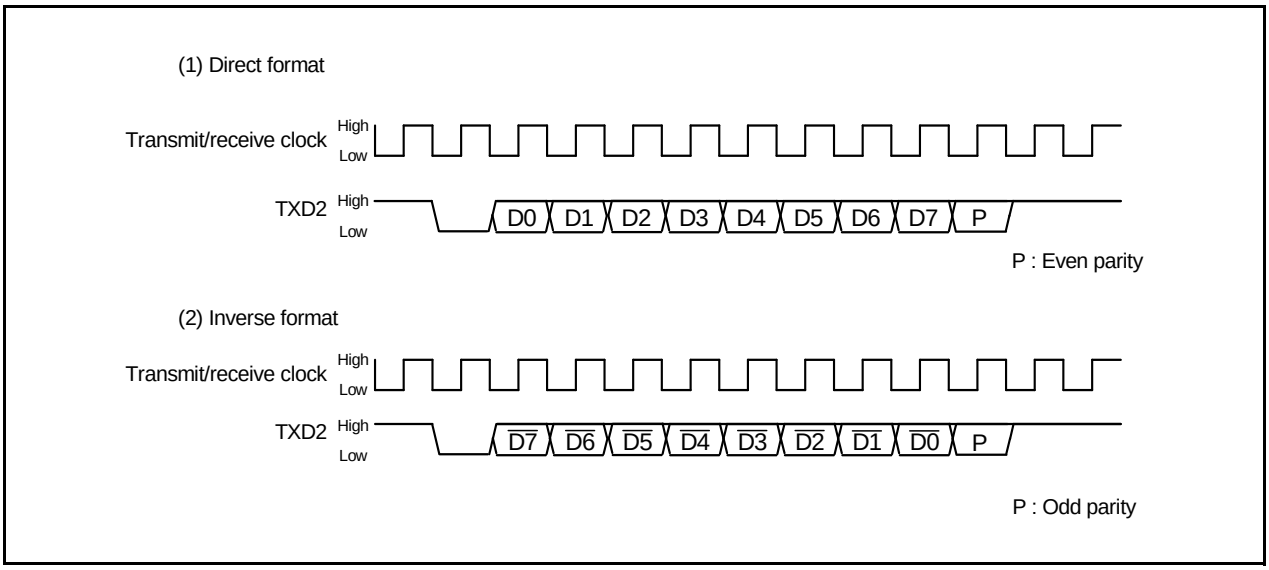


Figure 23.30 SIM Interface Format

23.4 Interrupts

UART0 to UART2 and UART5 to UART7 include interrupts by transmission, reception, ACK, NACK, start/stop condition detection, and bus collision detection.

23.4.1 Interrupt Related Registers

Refer to operation examples in each mode for interrupt sources and interrupt request generation timing. For the details of interrupt control, refer to 14.7 “Interrupt Control”. Table 23.26 lists UART0 to UART2, UART5 to UART7 Interrupt Related Registers.

Table 23.26 UART0 to UART2, UART5 to UART7 Interrupt Related Registers

Address	Register Name	Register Symbol	After Reset
0046h	UART1 Bus Collision Detection Interrupt Control Register	U1BCNIC	XXXX X000b
0047h	UART0 Bus Collision Detection Interrupt Control Register	U0BCNIC	XXXX X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register	BCNIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
006Bh	UART5 Bus Collision Detection Interrupt Control Register	U5BCNIC	XXXX X000b
006Ch	UART5 Transmit Interrupt Control Register	S5TIC	XXXX X000b
006Dh	UART5 Receive Interrupt Control Register	S5RIC	XXXX X000b
006Eh	UART6 Bus Collision Detection Interrupt Control Register	U6BCNIC	XXXX X000b
006Fh	UART6 Transmit Interrupt Control Register	S6TIC	XXXX X000b
0070h	UART6 Receive Interrupt Control Register	S6RIC	XXXX X000b
0071h	UART7 Bus Collision Detection Interrupt Control Register	U7BCNIC	XXXX X000b
0072h	UART7 Transmit Interrupt Control Register	S7TIC	XXXX X000b
0073h	UART7 Receive Interrupt Control Register	S7RIC	XXXX X000b
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h

Some interrupts of UART0 to UART2 and UART5 to UART7 share interrupt vectors and interrupt control registers with other peripheral functions. When using these interrupts, select them by interrupt source select registers. Table 23.27 lists Interrupt Select in UART0 to UART2 and UART5 to UART7.

Table 23.27 Interrupt Select in UART0 to UART2 and UART5 to UART7

Interrupt Source	Interrupt Source Select Register Settings		
	Register	Bit	Setting Value
UART0 start/stop condition detection, bus collision detection	IFSR2A	IFSR26	1
UART1 start/stop condition detection, bus collision detection	IFSR2A	IFSR27	1
UART5 start/stop condition detection, bus collision detection	IFSR3A	IFSR33	0
UART5 transmission, NACK	IFSR3A	IFSR34	0
UART6 start/stop condition detection, bus collision detection	IFSR3A	IFSR35	0
UART6 transmission, NACK	IFSR3A	IFSR36	0
UART7 start/stop condition detection, bus collision detection	IFSR2A	IFSR24	0
UART7 transmission, NACK	IFSR2A	IFSR25	0

An interrupt request may be generated by bit contents change in the following modes.

- Special mode 1 (I^2C mode)
  Set the IR bit in the interrupt control register of UARTi to 0 (interrupt not requested), when the following bits are changed:
  Bits SMD2 to SMD0 in the UiMR register, the IICM bit in the UiSMR register, the IICM2 bit in the UiSMR2 register, the CKPH bit in the UiSMR3 register
- Special mode 4 (SIM mode)
  After reset, when bits U2IRS and U2ERE in the U2C1 register are set to 1 (transmission completed) and 1 (interrupt not requested) respectively, a transmission interrupt request is generated. In SIM mode, set these bits first, and then set the IR bit in the S2TIC register to 0 (interrupt not requested).

23.4.2 Reception Interrupt

- The case that bits SMD2 to SMD0 in the UiMR register are not set to 010b (I^2C mode)
  When the RI bit in the UiC1 register is changed from 0 (no data in the UiRB register) to 1 (data present in the UiRB register), the IR bit in the SiRIC register is automatically set to 1 (interrupt requested).
  If an overrun error occurs (when the RI bit is 1, the next data is received), the RI bit remains 1, and therefore, the IR bit in the SiRIC register remains unchanged.
- The case that bits SMD2 to SMD0 in the UiMR register are set to 010b (I^2C mode)
  When the RI bit in the UiC1 register is changed from 0 (no data in the UiRB register) to 1 (data present in the UiRB register), the IR bit in the SiRIC register is automatically set to 1 (interrupt requested).
  When an overrun error occurs, the IR bit in the SiRIC register also becomes 1.

23.5 Notes on Serial Interface UARTi (i = 0 to 2, 5 to 7)

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins go to high-impedance state:
P7_2/CLK2/TA1OUT/V, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$, P7_4/TA2OUT/W, P7_5/TA2IN/$\overline{W}$, P8_0/TA4OUT/RXD5/SCL5/U, P8_1/TA4IN/$\overline{CTS5}$/$\overline{RTS5}$/$\overline{U}$

23.5.1 Clock Synchronous Serial I/O

23.5.1.1 Transmission/Reception

When the $\overline{RTS}$ function is used with an external clock, $\overline{RTSi}$ pin (i = 0 to 2, 5 to 7) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{RTSi}$ pin outputs a high-level signal when a receive operation starts. Therefore, a transmit timing and receive timing can be synchronized by connecting the $\overline{RTSi}$ pin to the $\overline{CTSi}$ pin of the transmitting side. The $\overline{RTS}$ function is disabled when an internal clock is selected.

23.5.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the UiC0 register (i = 0 to 2, 5 to 7) is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transmit and receive clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transmit and receive clock).

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low.

23.5.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating a transmitter. Set the UARTi-associated registers for a transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXDi pin (i = 0 to 2, 5 to 7) while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the UiC1 register to 1 (transmission enabled) and placing dummy data in the UiTB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the UiTB register, and input an external clock to the CLKi pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RI bit in the UiC1 register is set to 1 (data present in the UiRB register) and the next receive data is received in the UARTi receive register. And then, the OER bit in the UiRB register is set to 1 (overrun error occurred). At this time, the UiRB register is undefined. When an overrun error occurs, program the transmitting and receiving sides to retransmit the previous data. If an overrun error occurs, the IR bit in the SiRIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the UiTB register per each receive operation.

When an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is 0 (transmit data output at the falling edge and receive data input at the rising edge of the serial clock), or while the external clock is held low when the CKPOL bit is 1 (transmit data output at the rising edge and receive data input at the falling edge of the serial clock).

- The RE bit in the UiC1 register is 1 (reception enabled).
- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).

23.5.2 UART (Clock Asynchronous Serial I/O) Mode

23.5.2.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTSi}}$ pin (i = 0 to 2, 5 to 7) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTSi}}$ pin outputs a high-level signal when a receive operation starts. Therefore, a transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTSi}}$ pin to the $\overline{\text{CTSi}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

23.5.2.2 Transmission

When an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the UiC0 register (i = 0 to 2, 5 to 7) is 0 (transmit data output at the falling edge and receive data input at the rising edge of the transmit and receive clock), or while the external clock is held low when the CKPOL bit is 1 (transmit data output at the rising edge and receive data input at the falling edge of the transmit and receive clock).

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTSi}}$ pin is low.

23.5.3 Special Mode 1 (I^2C Mode)

23.5.3.1 Generation of Start and Stop Conditions

When generating start, stop and restart conditions, set the STSPSEL bit in the UiSMR4 register (i = 0 to 2, 5 to 7) to 0 and wait for more than half cycle of the transmit and receive clock. Then set each condition generation bit (STAREQ, RSTAREQ and STPREQ) from 0 to 1.

23.5.3.2 IR Bit

Set the following bits first, and then set the IR bit in the UARTi interrupt control registers to 0 (interrupt not requested).

Bits SMD2 to SMD0 in the UiMR register, the IICM bit in the UiSMR register,
the IICM2 bit in the UiSMR2 register, the CKPH bit in the UiSMR3 register

23.5.4 Special Mode 4 (SIM Mode)

After reset, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed) and 1 (error signal output), respectively. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.

24. Serial Interface SI/O3 and SI/O4

Note

The 80-pin package does not have the SIN3 pin for SI/O3. SI/O3 is used for transmission only. No reception is possible.

24.1 Introduction

SI/O3 and SI/O4 are dedicated clock-synchronous serial I/O ports.
Table 24.1 lists SI/O3 and SI/O4 Specifications.
Figure 24.1 shows SI/O3 and SI/O4 Block Diagram, and Table 24.2 lists the Input/Output Pins.

Table 24.1 SI/O3 and SI/O4 Specifications

Item	Specification
Data format	Character length: 8 bits
Transmit/Receive clocks	• The SMi6 bit in the SiC register = 1 (internal clock): $\frac{fj}{2(n+1)}$ fj = f1SIO, f8SIO, f32SIO n = setting value of the SiBRG register 00h to FFh The SMi6 bit = 0 (external clock): Input from the CLKi pin (1)
Transmission/reception start condition	Before transmission/reception starts, satisfy the following requirements. Write transmit data into the SiTRR register. (2)
Interrupt request generation timing	• SMi4 bit in the SiC register = 0 The rising edge of the last transmit/receive clock • the SMi4 bit = 1 The falling edge of the last transmit/receive clock
Selectable functions	• CLK polarity selection Whether data is output/input at the rising or falling edge of the transmit/receive clock can be selected. • LSB first or MSB first selection Whether to start transmitting/receiving data from bit 0 or from bit 7 can be selected. • SOUTi initial value setting function When the SMi6 bit in the SiC register = 0 (external clock), the SOUTi pin output level while not transmitting can be selected. • SOUTi state selection after transmission Whether to set to high-impedance or retain the last bit level can be selected when the SMi6 bit in the SiC register is 1 (internal clock).

i = 3, 4

Notes:

1. The data is shifted every time the external clock is input. When completing data transmission/reception of the 8th bit, read or write into the SiTRR register before inputting the clock for the next data transmission/reception.
2. When the SMi6 bit in the SiC register is 0 (external clock), follow the procedure described below.
   - If the SMi4 bit in the SiC register is 0, write transmit data into the SiTRR register while input to the CLKi pin is high.
   - If the SMi4 bit is 1, write transmit data into the SiTRR register while input to the CLKi pin is low.

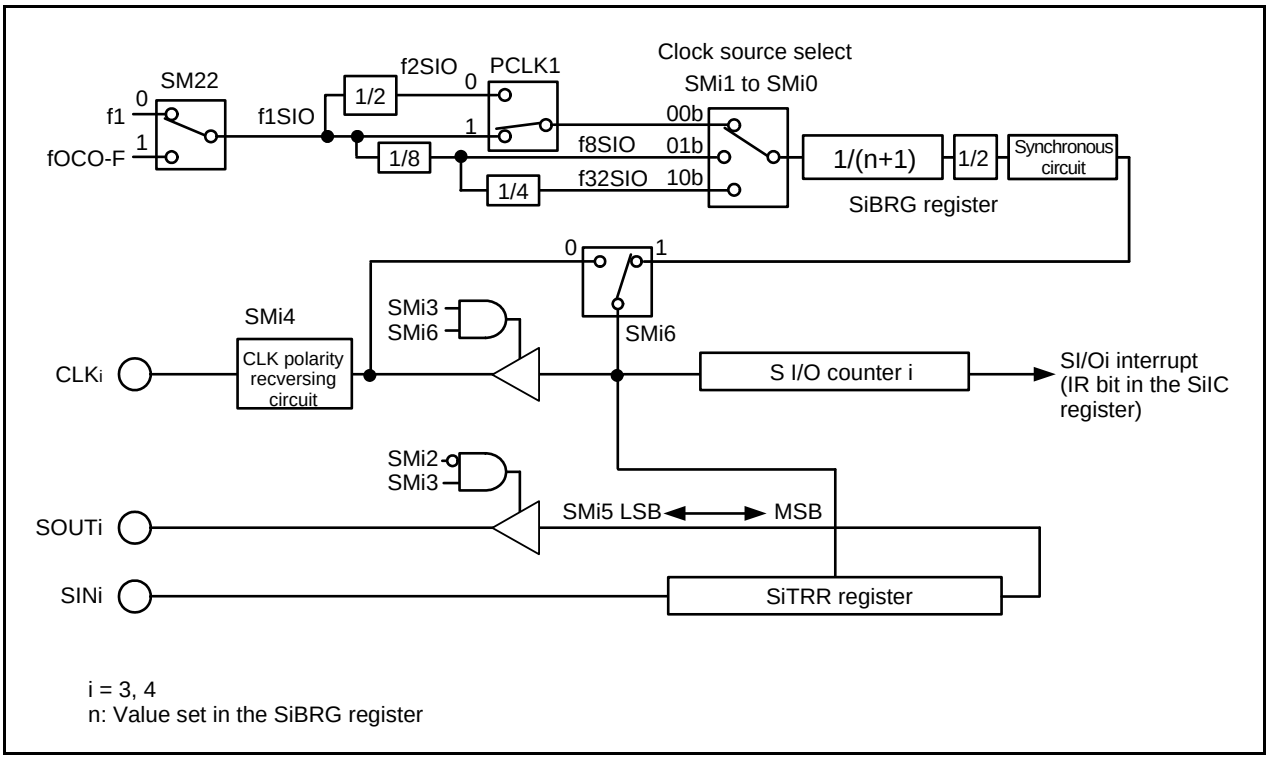


Figure 24.1 SI/O3 and SI/O4 Block Diagram

Table 24.2 Input/Output Pins

Pin Name	Input/Output	Function	Selecting Method
CLKi	Output	Transmit/receive clock output	SMi3 bit in the SiC register = 1 SMi6 bit in the SiC register = 1
	Input	Transmit/receive clock input	SMi3 bit in the SiC register = 1 SMi6 bit in the SiC register = 0 Port direction bits sharing pins = 0
SOUTi	Output	Serial data output	SMi3 bit in the SiC register = 1 SMi2 bit in the SiC register = 0
SINi	Input	Serial data input	SMi3 bit in the SiC register = 1 Port direction bits sharing pins = 0 (Dummy data is input only when transmitting.)

24.2 Registers

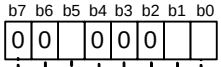
Table 24.3 lists registers associated with SI/O3 and SI/O4.
Set the SM22 bit in the S34C2 register before setting other registers associated with SI/O3 and SI/O4. After changing the SM22 bit, set other registers associated with SI/O3 and SI/O4 again.

Table 24.3 Register Structure

Address	Register Name	Register Symbol	After Reset
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0270h	SI/O3 Transmit/Receive Register	S3TRR	XXh
0272h	SI/O3 Control Register	S3C	0100 0000b
0273h	SI/O3 Bit Rate Register	S3BRG	XXh
0274h	SI/O4 Transmit/Receive Register	S4TRR	XXh
0276h	SI/O4 Control Register	S4C	0100 0000b
0277h	SI/O4 Bit Rate Register	S4BRG	XXh
0278h	SI/O3, 4 Control Register 2	S34C2	00XX X0X0b

24.2.1 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register



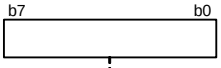
Symbol	Address	After Reset
PCLKR	0012h	0000 0011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A and B clock select bit (clock source for timers A and B, the dead time timer, and muliti-master I^2C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART2, UART5 to UART7, SI/O3, and SI/O4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0	RW
PCLK5	Clock output function extension bit (valid in single-chip mode)	0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1	RW
— (b7-b6)	Reserved bits	Set to 0	RW

Rewrite the PCLKR register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

24.2.2 SI/O Transmit/Receive Register (SiTRR) (i = 3, 4)

SI/Oi Transmit/Receive Register (i = 3, 4)



Symbol	Address	After Reset
S3TRR	0270h	Undefined
S4TRR	0274h	Undefined

Function	RW
Transmission/reception starts by writing transmit data into this register. After transmission/reception completes, receive data can be read.	RW

Write into the SiTRR register while serial interface is neither transmitting nor receiving.
Write the value into the SiTRR register every time one byte data is received even when data is only received.

24.2.3 SI/Oi Control Register (SiC) (i = 3, 4)

SI/Oi Control Register (i = 3, 4)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S3C	0272h	0100 0000b
S4C	0276h	0100 0000b

Bit symbol	Bit Name	Function	RW
SMi0	Internal synchronous clock select bit	b1 b0 0 0 : Selecting f1SIO or f2SIO 0 1 : Selecting f8SIO 1 0 : Selecting f32SIO 1 1 : Do not set	RW
SMi1			
SMi2	SOUTi output disable bit	0 : SOUTi output enabled 1 : SOUTi output disabled (high-impedance)	RW
SMi3	SI/Oi port select bit	0 : Input/output port serial interface disabled 1 : SOUTi output, CLKi function serial interface enabled	RW
SMi4	CLK polarity select bit	0 : Transmit data is output at falling edge of transmit/receive clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transmit/receive clock and receive data is input at falling edge	RW
SMi5	Bit order select bit	0 : LSB first 1 : MSB first	RW
SMi6	Synchronous clock select bit	0 : External clock 1 : Internal clock	RW
SMi7	SOUTi initial output set bit	Valid when SMi6 = 0 0 : Low output 1 : High output	RW

Write into the SiC register by the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enabled).

SMi1-SMi0 (Internal Synchronous Clock Select Bit) (b1-b0)

Select f1SIO or f2SIO by the PCLK1 bit in the PCLKR register.
Set the SiBRG register when changing bits SMi1 to SMi0.

SMi2 (SOUTi Output Disable Bit) (b2)

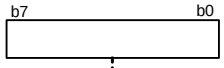
When the SMi2 bit is set to 1 (SOUTi output disabled), the target pin goes to high-impedance state regardless of which function of the pin is being used.

SMi7 (SOUTi Initial Value Set Bit) (b7)

Set the SMi7 bit when the SMi3 bit is 0 (input/output port, serial interface disabled). The level selected by the SMi7 bit is output from the SOUTi pin by setting the SMi3 bit to 1 and SMi2 bit to 0 (SOUTi output).

24.2.4 SI/Oi Bit Rate Register (SiBRG) (i = 3, 4)

SI/Oi Bit Rate Register (i = 3, 4)



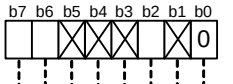
Symbol	Address	After Reset
S3BRG	0273h	Undefined
S4BRG	0277h	Undefined

Function	Setting Range	RW
SiBRG divides the count source by n + 1 where n = set value	00h to FFh	WO

Use MOV instruction to write into the SiBRG register.
Write into the SiBRG register after setting bits SMi1 to SMi0 in the SiC register and while serial interface is neither transmitting nor receiving.

24.2.5 SI/O3, 4 Control Register 2 (S34C2)

SI/O3, 4 Control Register 2



Symbol	Address	After Reset
S34C2	0278h	00XX X0X0b

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	Set to 0	RW
— (b1)	No register bit. If necessary, set to 0. Read as undefined value		—
SM22	SI/O3, SI/O4 before-division clock select bit	0: f1 1: fOCO-F	RW
— (b5-b3)	No register bits. If necessary, set to 0. Read as undefined value		—
SM26	SOUT3 output control bit	SOUT3 state after transmission 0 : High-impedance 1 : Last bit level retained	RW
SM27	SOUT4 output control bit	SOUT4 state after transmission 0 : High-impedance 1 : Last bit level retained	RW

SM22 (SI/O3, SI/O4 Before-division Clock Select Bit) (b2)

Set the SM22 bit while transmission/reception of SI/O3 and SI/O4 stops.
Set the SM22 bit before setting other registers associated with SI/O3 and SI/O4. After changing the SM22 bit, set other registers associated with SI/O3 and SI/O4 again.

SM26 (SOUT3 Output Control Bit) (b6)
SM27 (SOUT4 Output Control Bit) (b7)

Bits SM26 and SM27 are valid when the SMi6 bit in the SiC register is set to 1 (internal clock). Set the SMi3 bit in the SiC register to 1 (serial interface enabled) after setting bits SM26 and SM27.

24.3 Operations

24.3.1 Basic Operations

SI/Oi transmits and receive data simultaneously. The SiTRR register is not divided into the register for transmission/reception and buffer. Write transmit data into the SiTRR register while transmission/reception stops. Read receive data from the SiTRR register while transmission/reception stops.

24.3.2 CLK Polarity Selection

The SMi4 bit in the SiC register allows selection of the polarity of the transmit/receive clock. Figure 24.2 shows Polarity of Transmit/Receive Clock.

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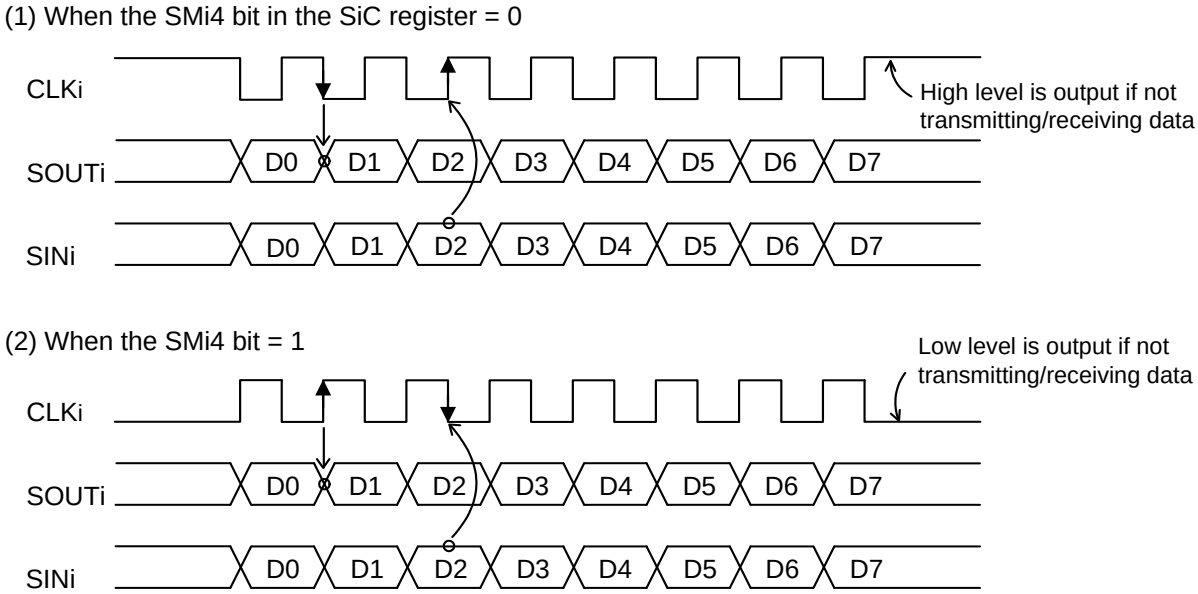
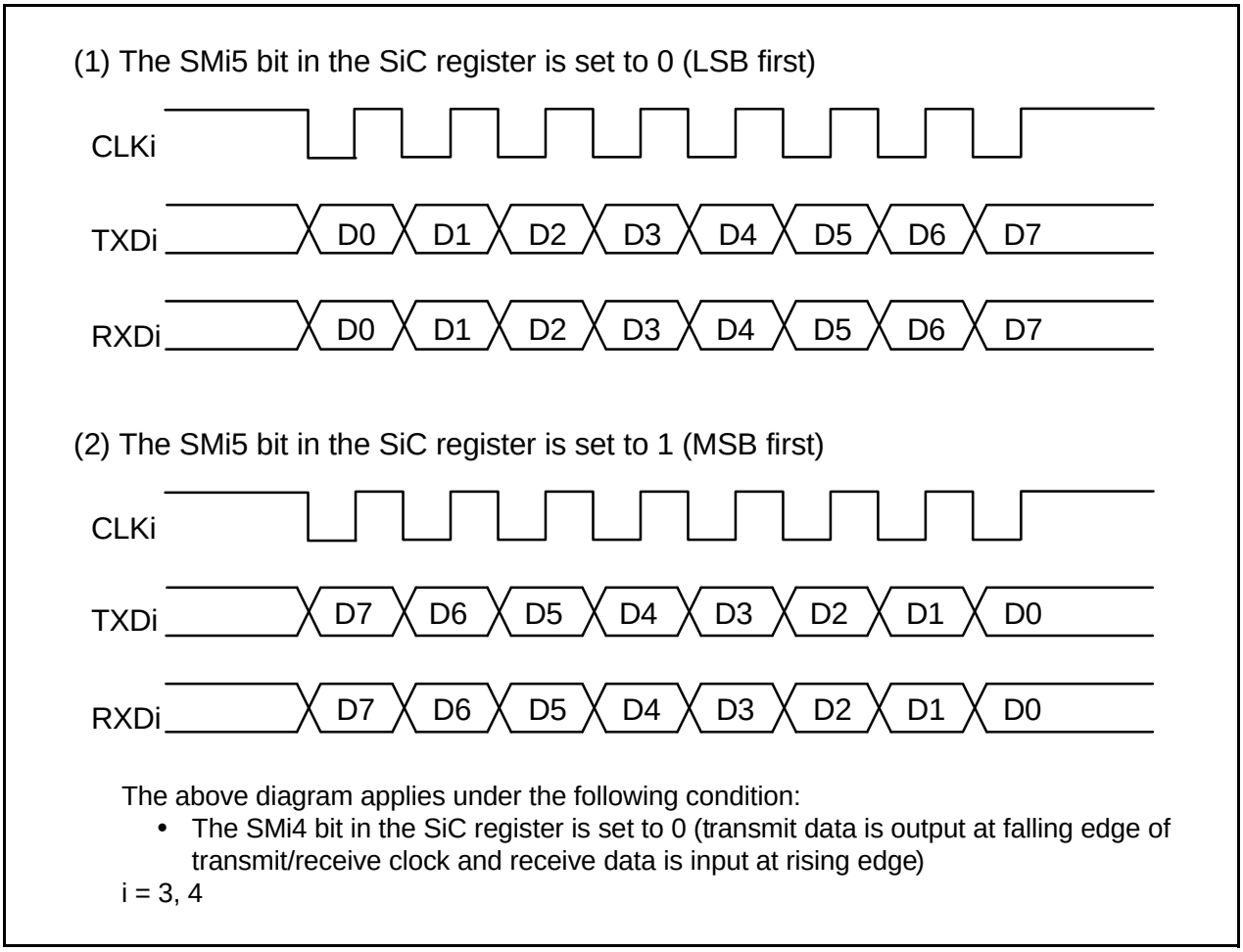


Notes:
The above diagram applies under the following conditions.
1. The SMi5 bit in the SiC register is 0 (LSB first).
2. The SMi6 bit in the SiC register is 1 (internal clock).
3. The SM26 bit or SM27 bit in the S32C2 register is 1 (SOUTi output retains last bit level)

Figure 24.2 Polarity of Transmit/Receive Clock

24.3.3 LSB First or MSB First Selection

Bit order is selected by the SMi5 bit in the SiC register (i = 3, 4). Figure 24.3 shows Bit Order.



The above diagram applies under the following condition:

- The SMi4 bit in the SiC register is set to 0 (transmit data is output at falling edge of transmit/receive clock and receive data is input at rising edge)

i = 3, 4

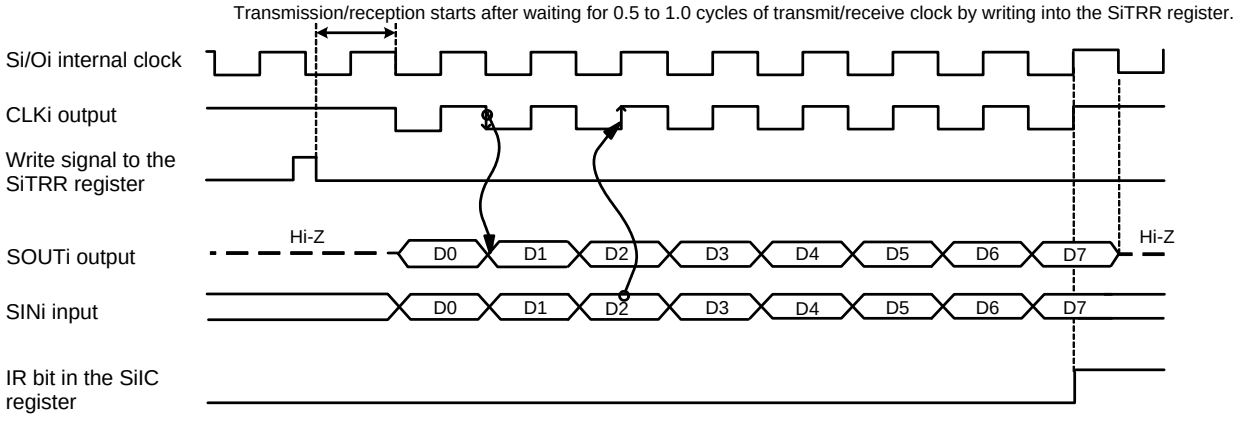
Figure 24.3 Bit Order

24.3.4 Internal Clock

When the SMi6 bit in the SiC register is 1, data is transmitted/received using internal clock. The internal clock is selected by the SM22 bit in the S32C2 register, the PCLK1 bit in the PLCKR register, and bits SMi1 to SMi0 in the SiC register. When the internal clock is used as transmit/receive clock, the SOUTi pin becomes high-impedance from when the SMi3 bit in the SiC register is set to 1 (SI/Oi enabled) and the SMi2 bit is set to 0 (SOUTi output enabled) to when the first data is output.

When writing the transmit data into the SiTRR register, data transmission/reception starts by outputting the transmit/receive clock from the CLKi pin after waiting for 0.5 to 1.0 cycles of the transmit/receive clock. When completing the transmission/reception of 8 bits data, the transmit/receive clock from the CLKi pin stops.

Figure 24.4 shows SI/Oi Operation Timing (Internal Clock).



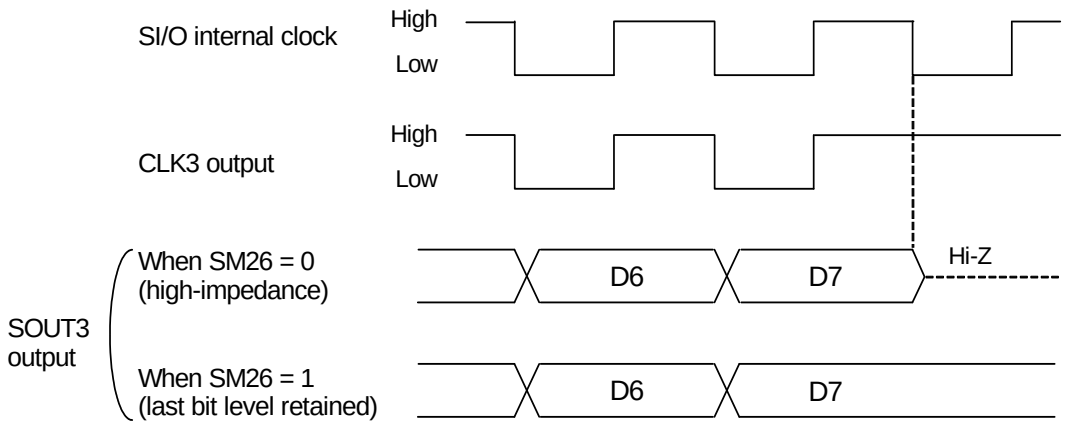
i = 3, 4

The above diagram applies under the following conditions:
In the SiC register, SMi2 = 0 (SOUTi output), SMi3 = 1 (SOUTi output, CLKi function), SMi4 = 0 (transmit data is output at falling edge of transmist/receive clock and receive data is input at rising edge), SMi5 = 0 (LSB first), SMi6 = 1 (internal clock).
In the S34C2 register, the SM26 bit (SOUT3) or SM27 bit (SOUT4) = 0 (high-impedance after transmission).

Figure 24.4 SI/Oi Operation Timing (Internal Clock)

24.3.5 Function for Selecting SOUTi State after Transmission

The SOUTi pin state after transmission is selected when the SMi6 bit in the SiC register is set to 1 (internal clock). If bits SM26 and SM27 in the S34C2 register are set to 1 (last bit level retained), output from the SOUTi pin retains the last bit level after transmission. Figure 24.5 shows Level of SOUT3 Pin after Transmission.



The above SOUT3 example applies under the following conditions.
The SM32 bit in the S3C register is 0 (SOUT3 output),
The SM33 bit in the S3C register is 1 (SOUT3 output, CLK3 selected),
The SM34 bit in the S3C register is 0 (transmit data output at the falling edge of the transmit/receive clock and the receive data is input at the rising edge),
The SM35 bit in the S3C register is 0 (LSB first), and
The SM36 bit in the S3C register is 1 (internal clock)

Figure 24.5 Level of SOUT3 Pin after Transmission

24.3.6 External Clock

When the SMi6 bit in the SiC register is set to 0, data is transmitted/received using external clock.
The external clock is used as transmit/receive clock, the SOUTi output level from when the SMi3 bit in the SiC register is set to 1 (SI/Oi enabled) and SMi2 bit is set to 0 (SOUTi output enabled) to when the first data is output can be selected by the SMi7 bit in the SiC register. Refer to 24.3.8 “Function for Setting SOUTi Initial Value”.
Transmission/reception starts with the external clock after writing the transmit data into the SiTRR register.
The data written into the SiTRR register is shifted every time the external clock is input. When completing data transmission/reception of the 8th bit, read or write into the SiTRR register before inputting the clock for the next data transmission/reception.
Figure 24.6 shows SI/Oi Operation Timing (External Clock).

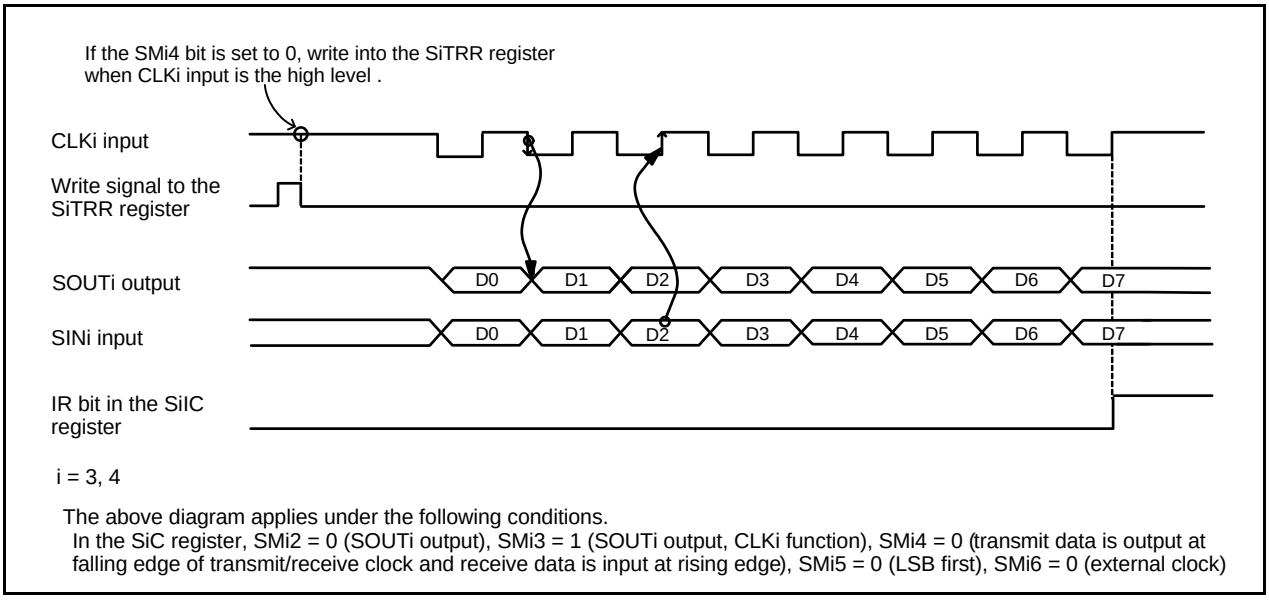


Figure 24.6 SI/Oi Operation Timing (External Clock)

When the SMi6 bit in the SiC register is set to 0 (external clock), write into the SiTRR register and SMi7 bit in the SiC register under the following conditions:

- When the SMi4 bit in the SiC register is set to 0 (transmit data is output at falling edge of transmit/receive clock and receive data is input at rising edge): CLKi input is high level.
- When the SMi4 bit is set to 1 (transmit data is output at rising edge of transmit/receive clock and receive data is input at falling edge): CLKi input is low level.

24.3.7 SOUTi Pin

The SOUTi pin state can be selected by bits SMi2 and SMi3 in the SiC register.
Table 24.4 lists SOUTi Pin State.

Table 24.4 SOUTi Pin State

Bit Setting		SOUTi Pin State
SiC register		
SMi2	SMi3	
0	0	I/O port or another peripheral function
	1	SOUTi output
1	0/1	High-impedance

24.3.8 Function for Setting SOUTi Initial Value

If the SMi6 bit in the SiC register is set to 0 (external clock), the SOUTi pin output can be fixed high or low when not transmitting/receiving data. High or low can be selected by the SMi7 bit in the SiC register. However, the last bit value of the previous unit of data is retained between adjacent units of data when using external clock. Figure 24.7 shows Timing Chart for Setting SOUTi Initial Value and How to Set It.

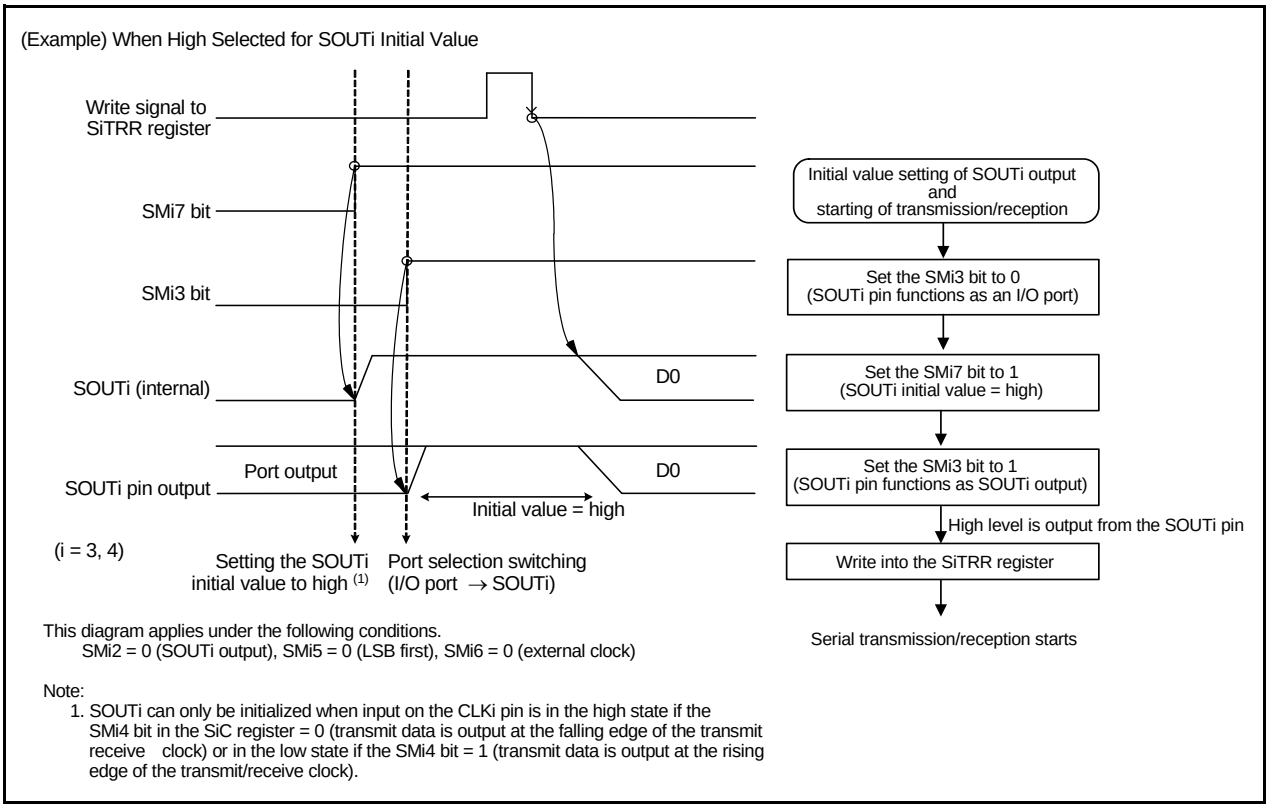


Figure 24.7 Timing Chart for Setting SOUTi Initial Value and How to Set It

24.4 Interrupt

Refer to the operation example for interrupt source or interrupt request generation timing. Refer to 14.7 “Interrupt Control” for interrupt control. Table 24.5 lists Registers Associated with SI/O3 and SI/O4.

Table 24.5 Registers Associated with SI/O3 and SI/O4

Address	Register Name	Register Symbol	After Reset
0048h	SI/O4 Interrupt Control Register	S4IC	XX00 X000b
0049h	SI/O3 Interrupt Control Register	S3IC	XX00 X000b
0207h	Interrupt Source Select Register	IFSR	00h

The following interrupts share the interrupt vector and interrupt control register with other peripheral functions. To use the following interrupts, set bits as follows.

- SI/O3: Set the IFSR6 bit in the IFSR register to 0 (SI/O3).
- SI/O4: Set the IFSR7 bit in the IFSR register to 0 (SI/O4).

Set the POL bit in the SiIC register to 0 (falling edge).

24.5 Notes on Serial Interface SI/O3 and SI/O4

24.5.1 SOUTi Pin Level When SOUTi Output Disabled

When the SMi2 bit in the SiC register is set to 1 (SOUTi output disabled), the target pin goes to high-impedance state regardless of which function of the pin is being used.

24.5.2 External Clock Control

The data written into the SiTRR register is shifted every time the external clock is input. When completing data transmission/reception of the 8th bit, read or write into the SiTRR register before inputting the clock for the next data transmission/reception.

24.5.3 Register Access When Using External Clock

When the SMi6 bit in the SiC register is set to 0 (external clock), write into the SMi7 bit in the SiC register and the SiTRR register under the following conditions:

- When the SMi4 bit in the SiC register is set to 0 (transmit data is output at falling edge of transmit/receive clock and receive data is input at rising edge): CLKi input is high level.
- When the SMi4 bit in the SiC register is set to 1 (transmit data is output at rising edge of transmit/receive clock and receive data is input at falling edge): CLKi input is low level.

24.5.4 SiTRR Register Access

Write transmit data into the SiTRR register while transmission/reception stops. Read receive data from the SiTRR register while transmission/reception stops.

The IR bit in the SiIC register becomes 1 (interrupt request) during output of the 8th bit.

If the SM26 bit (SOUT3) or SM27 bit (SOUT4) in the S32C2 register is set to 0 (high-impedance after transmission), SOUTi pin becomes high-impedance when the transmit data is written into the SiTRR register immediately after an interrupt request is generated, and hold time of the transmit data becomes shorter.

24.5.5 Pin Function Switch When Using Internal Clock

If the SMi3 bit in the SiC register (i = 3, 4) changes from 0 (I/O port) to 1 (SOUTi output, CLK function) when setting the SMi2 bit to 0 (SOUTi output) and the SMi6 bit to 1 (internal clock), SOUTi initial value set to the SOUTi pin by the SMi7 bit may be output about for 10 ns. After that, the SOUTi pin becomes high-impedance.

If the output level from the SOUTi pin when the SMi3 bit changes from 0 to 1 becomes a problem, set the SOUTi initial value by the SMi7 bit.

24.5.6 Operation After Reset When Selecting External Clock

When the SMi6 bit in the SiC register is set to 0 (external clock) after reset, the IR bit in the SiIC register becomes 1 (interrupt request) by inputting the external clock for 8 bits to the CLKi pin. This will also happen even when the SMi3 bit in the SiC register is 0 (serial interface disabled) or before the value is written into the SiTRR register.

25. Multi-Master I2C-bus Interface

25.1 Introduction

The multi-master I2C-bus interface (I2C interface) is a serial communication circuit based on I2C-bus data transmit/receive format, equipped with arbitration lost detection and clock synchronous functions.
Table 25.1 lists Multi-master I2C-bus Interface Specification, Table 25.2 lists Detections of I2C Interface, Figure 25.1 shows Multi-master I2C-bus Interface Block Diagram, and Table 25.3 lists I/O Ports.

Table 25.1 Multi-master I2C-bus Interface Specification

Item	Function
Format	Based on I2C-bus standard: 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	Based on I2C-bus standard: Master-transmitter Master-receiver Slave-transmitter Slave-receiver
Bit rate	16.1 kbps to 400 kbps (fVIIC = 4 MHz)
I/O pin	Serial data line SDAMM (SDA) Serial clock line SCLMM (SCL)
Interrupt request generating source	I2C-bus interrupt Completion of transmission Completion of reception Slave address match detection General call detection Stop condition detection Timeout detection • SDA/SCL interrupt Rising or falling edge of the SDAMM/SCLMM line
Selectable functions	• I2C-bus interface pin input level select Selectable input level with I2C-bus input level or SMBus input level • SDA/port, SCL/port selection A function to change pins SDAMM and SCLMM to output ports respectively. • Timeout detection A function to detect that SCLMM pin is driven high for over a certain period of time when the bus is busy. • Free format select A function to generate an interrupt request when receiving the 1st byte data, regardless of the slave address value.

fVIIC: I2C-bus system clock

Table 25.2 Detections of I2C Interface

Item	Function
Slave address match	A function to detect a slave address match as a slave-transmitter or receiver. When own slave address is matched with the calling address sent from a master, ACK is generated automatically. When an address match is not found, no ACK is generated and no more data is transmitted or received. One slave can have up to three slave addresses.
General call	A function to detect a general call as a slave-receiver.
Arbitration lost	A function to detect arbitration lost to stop the SDAMM clock output immediately.
Bus busy	A function to detect a bus busy state and set/reset the BB bit.

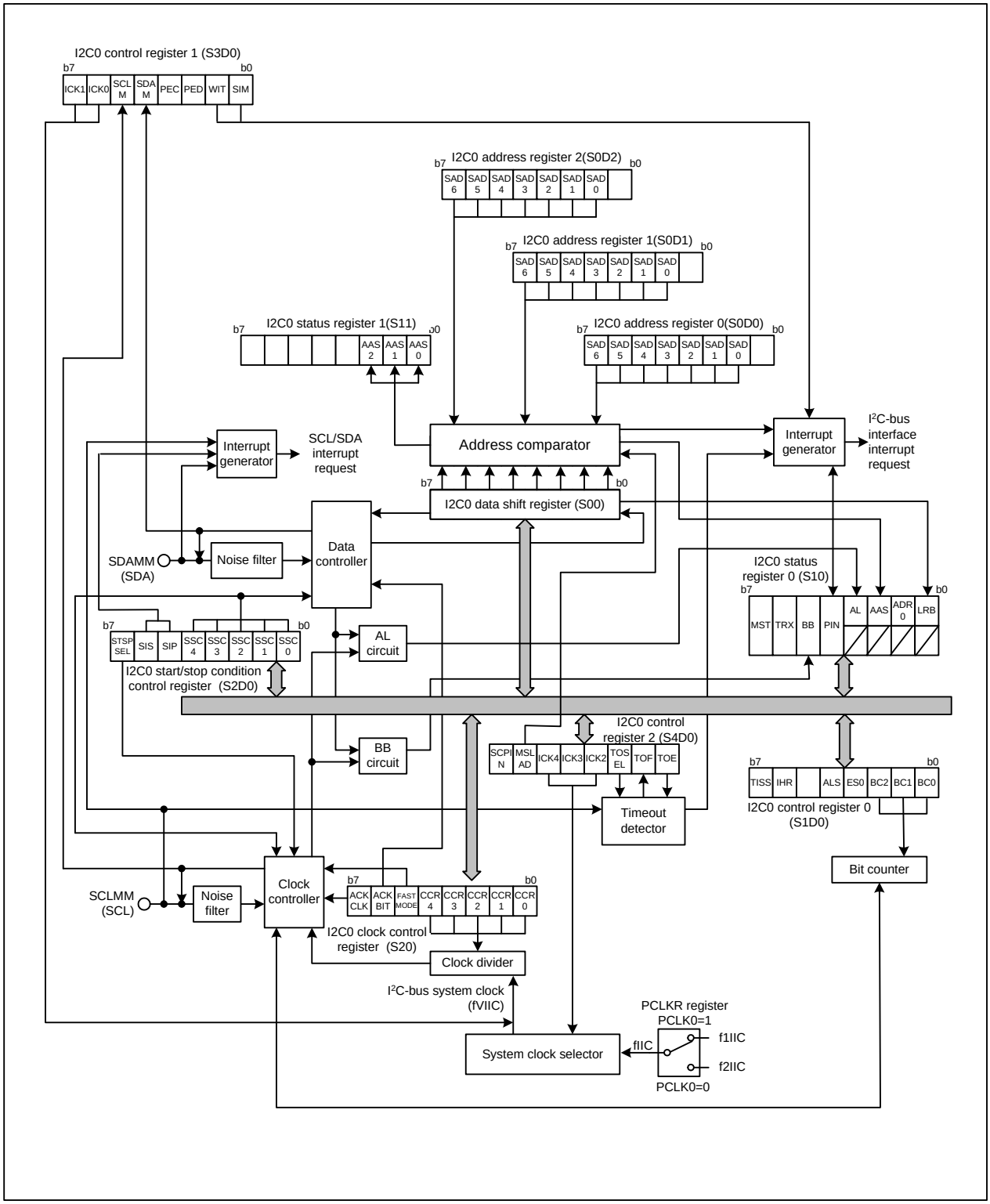


Figure 25.1 Multi-master I2C-bus Interface Block Diagram

Table 25.3 I/O Ports

Pin Name	I/O Type	Function
SDAMM	I/O	I/O pin for SDA (N channel open drain output)
SCLMM	I/O	I/O pin for SCL (N channel open drain output)

25.2 Registers Descriptions

Table 25.4 lists registers associated with multi-master I2C-bus interface. When the CM07 bit in the CM0 register is set to 1 (sub clock is CPU clock), registers listed in Table 25.4 should not be accessed. Set them after the CM07 bit is set to 0 (main clock, PLL clock, or on-chip oscillator clock).

Table 25.4 Register Configuration

Address	Register Name	Symbol	After Reset
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
02B0h	I2C0 Data Shift Register	S00	XXh
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	00h
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb

25.2.1 Peripheral Clock Select Register (PCLKR)

Peripheral Clock Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0		0	0	0		

Symbol	Address	After Reset
PCLKR	0012h	0000 0011b

Bit Symbol	Bit Name	Function	RW
PCLK0	Timers A and B clock select bit (clock source for timers A and B, the dead time timer, and muliti-master I2C-bus interface)	0: f2TIMAB/f2IIC 1: f1TIMAB/f1IIC	RW
PCLK1	SI/O clock select bit (clock source for UART0 to UART2, UART5 to UART7, SI/O3, and SI/O4)	0: f2SIO 1: f1SIO	RW
— (b4-b2)	Reserved bits	Set to 0	RW
PCLK5	Clock output function extension bit (valid in single-chip mode)	0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1	RW
— (b7-b6)	Reserved bits	Set to 0	RW

Write to the PCLKR register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

25.2.2 I2C0 Data Shift Register (S00)

I2C0 Data Shift Register

b7 b0	Symbol	Address	After Reset
	S00	02B0h	Undefined

Function	RW
Transmit/receive data is stored.	RW

When the I2C interface is a transmitter, write a transmit data to the S00 register. When the I2C interface is a receiver, a received data can be read from the S00 register. In master mode, this register is used to generate a start condition or stop condition on a bus. (Refer to 25.3.2 “Generation of Start Condition” and 25.3.3 “Generation of Stop Condition”.)

Write to the S00 register when the ES0 bit in the S1D0 register is set to 1 (I2C interface enabled). The S00 register should not be written when data transmission/reception is in progress.

When the I2C interface is a transmitter, the data written in the S00 register is transmitted to other devices. The MSB (bit 7) is transmitted first, synchronizing with the SCLMM clock. Every time one-bit data is output, the content of the S00 register is one-bit shifted to the left.

When the I2C interface is a receiver, a data is transferred to the S00 register from other devices. The LSB (bit 0) is input first, synchronizing with the SCLMM clock. Every time one-bit data is output, the content of the S00 register is one-bit shifted to the left. Figure 25.2 shows Timing to Store The Received Data into The S00 Register.

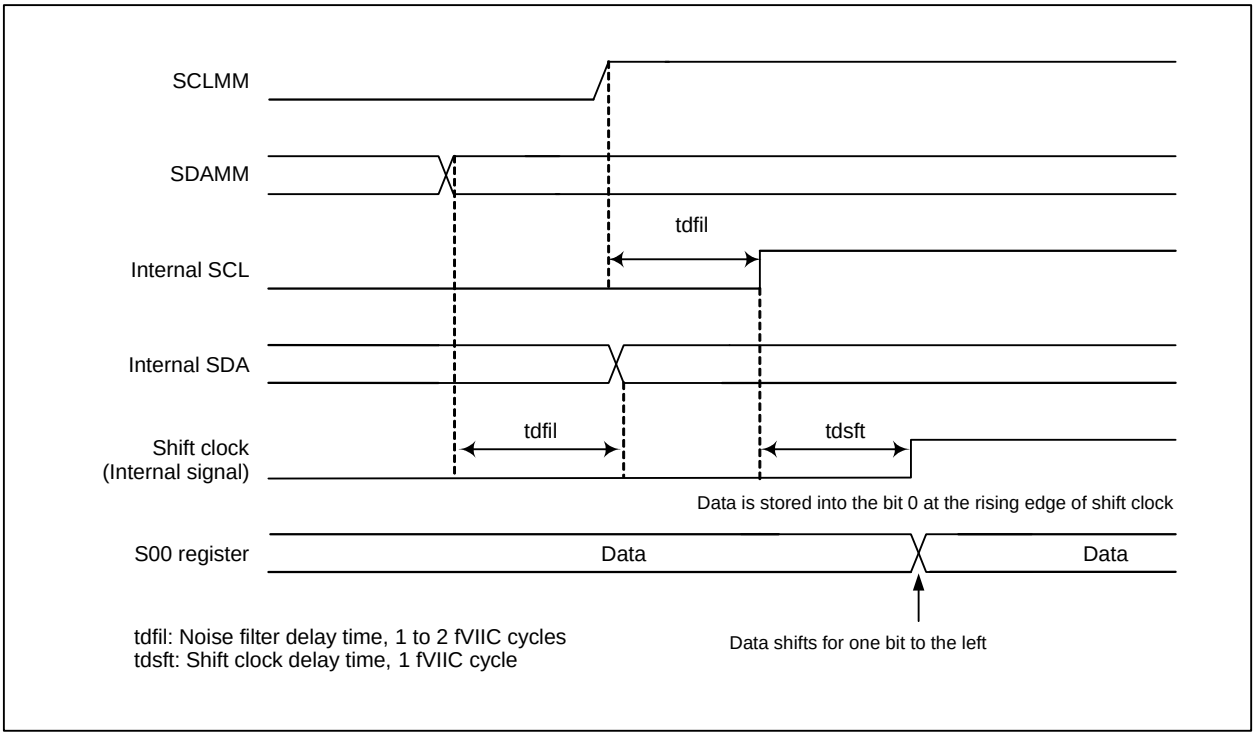


Figure 25.2 Timing to Store The Received Data into The S00 Register

25.2.3 I2C0 Address Register i (S0Di) (i = 0 to 2)

I2C0 Address Register i (i = 0 to 2)

b7	b6	b5	b4	b3	b2	b1	b0
							0

Symbol	Address	After Reset
S0D0	02B2h	0000 000Xb
S0D1	02BAh	0000 000Xb
S0D2	02BBh	0000 000Xb

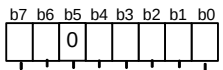
Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. Read as undefined value		—
SAD0	Slave Address	Set a slave address	RW
SAD1			RW
SAD2			RW
SAD3			RW
SAD4			RW
SAD5			RW
SAD6			RW

SAD6-SAD0 (Slave Address) (b7-b1)

Bits SAD6 to SAD0 indicate a slave address to be compared for a slave address match detection in slave mode. An I2C interface can have maximum of three slave addresses. Set bits SAD6 to SAD0 in the S0Di register to 0000000b when not setting the slave address.
However, when the MSLAD bit in the S4D0 register is 0, registers S0D1 and S0D2 are disabled. Only the slave address set to the S0D0 register is compared with address data received.

25.2.4 I2C0 Control Register (S1D0)

I2C0 Control Register 0



Symbol: S1D0 | Address: 02B3h | After Reset: 00X0 0000b

Bit Symbol	Bit Name	Function	RW
BC0	Bit counter (number of transmitted/received bits)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	RW
BC1			RW
BC2			RW
ES0	I2C bus interface enable bit	0: Disabled 1: Enabled	RW
ALS	Data format select bit	0: Addressing format 1: Free data format	RW
— (b5)	Reserved bit	Set to 0.	RW
IHR	I2C-bus interface reset bit	0: reset is deasserted (automatically) 1: reset	RW
TISS	I2C-bus interface pin input level select bit	0: I2C-bus input 1: SMBus input	RW

BC2-BC0 (Bit Counter) (b2-b0)

Bits BC2 to BC0 become 000b (8 bits) when start or stop condition is detected.
When the ACKCLK bit in the S20 register is 0 (no ACK clock), and data for the number of bits selected by bits BC2 to BC0 is transmitted or received, bits BC2 to BC0 become 000b again.
When the ACKCLK bit in the S20 register is 1 (ACK clock), data for the number of bits selected and an ACK is transmitted or received, bits BC2 to BC0 become 000b again.

ES0 (I2C bus Interface Enable Bit) (b3)

The ES0 bit enables the I2C interface.

When the ES0 bit is set to 0, the I2C interface status becomes as follows.

- Pins SDAMM and SCLMM: I/O port or other peripheral pins
- Write disable to the S00 register
- I2C-bus system clock (hereinafter called fVIIC) stops
- S10 register
  - ADR0 bit: 0 (general call not detected)
  - AAS bit: 0 (slave address not matched)
  - AL bit: 0 (arbitration lost not detected)
  - PIN bit: 1 (no I2C-bus interrupt request)
  - BB bit: 0 (bus free)
  - TRX bit: 0 (receive mode)
  - MST bit: 0 (slave mode)
- Bits AAS2 to AAS0 in the S11 register: 0 (slave address not matches)
- TOF bit in the S4D0 register: 0 (timeout not detected)

ALS (Data Format Select Bit) (b4)

The ALS bit is enabled in slave mode. When the ALS bit is 0 (addressing format), the slave address match detection is performed.

When any of the slave address stored into bits SAD6 to SAD0 in the S0Di register (i = 0 to 2) is compared and matched with the calling address by a master, or when a general call address is received, the IR bit in the IICIC register becomes 1 (interrupt requested).

When the ALS bit is 1 (free format), the slave address match detection is not performed. Therefore, the IR bit in the IICIC register becomes 1 (interrupt requested), regardless of the calling address by a master.

IHR (I2C bus Interface Reset Bit) (b6)

The IHR bit resets the I2C interface if a difficulty in transmission/reception is encountered. When the ES0 bit in the S1D0 register is 1 (I2C interface enabled) and then the IHR bit is set to 1 (reset), the I2C interface becomes as follows.

- S10 register

ADR0 bit: 0 (general call not detected)
AAS bit: 0 (slave address not matched)
AL bit: 0 (arbitration lost not detected)
PIN bit: 1 (No I2C-bus interrupt request)
BB bit: 0 (bus free)
TRX bit: 0 (receive mode)
MST bit: 0 (slave mode)

- Bits AAS2 to AAS0 in the S11 register: 0 (slave address not matches)
- TOF bit in the S4D0 register: 0 (timeout not detected)

When the IHR bit is set to 1, the I2C interface is reset and the IHR bit becomes 0 automatically. It takes maximum of 2.5 fVIIC cycles to complete reset sequence.

Figure 25.3 shows Reset Timing of I2C Interface.

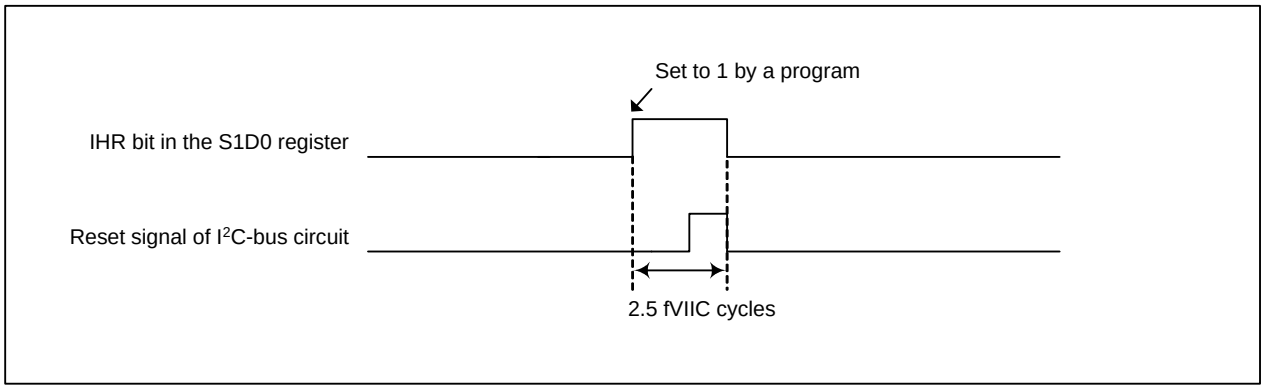


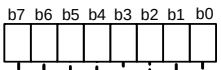
Figure 25.3 Reset Timing of I2C Interface

TISS (I2C bus Interface Pin Input Level Select Bit) (b7)

The TISS bit selects the input level of the SCLMM pin and SDAMM pin for the I2C interface.

25.2.5 I2C0 Clock Control Register (S20)

I2C0 Clock Control Register



Symbol	Address	After Reset
S20	02B4h	00h

Bit Symbol	Bit Name	Function	RW
CCR0	Bit rate control bit	Refer to bits CCR4 to CCR0 (Bit Rate Control Bit) (b4 to b0) in the S20 register.	RW
CCR1			RW
CCR2			RW
CCR3			RW
CCR4			RW
FASTMODE	SCL mode select bit	0: Standard-speed clock mode 1: High-speed clock mode	RW
ACKBIT	ACK bit	0: ACK is returned 1: ACK is not returned	RW
ACKCLK	ACK clock bit	0: No ACK clock present 1: ACK clock present	RW

CCR4-CCR0 (Bit Rate Control Bit) (b4-b0)

The setting range of bits CCR4 to CCR0 (CCR value) is 0 to 31. If the setting values of bits CCR4 to CCR0 are the CCR value (CCR value: 3 to 31), the bit rate can be determined by the following equations.
Refer to 25.3.1.2 “Bit Rate and Duty Cycle” for more details.

In standard speed clock mode,

$$\text{Bit rate} = \frac{\text{fVIIC}}{8 \times \text{CCR value}} \leq 100 \text{ kbps}$$

When the CCR value is other than 5 in high-speed clock mode,

$$\text{Bit rate} = \frac{\text{fVIIC}}{4 \times \text{CCR value}} \leq 400 \text{ kbps}$$

When the CCR value is 5 in high-speed clock mode, the bit rate is assumed to reach 400 kbps, the maximum bit rate in high-speed clock mode.

$$\text{Bit rate} = \frac{\text{fVIIC}}{2 \times \text{CCR value}} = \frac{\text{fVIIC}}{10} \leq 400 \text{ kbps}$$

The CCR value should not be set to 0 to 2 regardless of the fVIIC frequency.
Bits CCR4 to CCR0 should not be rewritten during transmission/reception.

FASTMODE (SCL Mode Select Bit) (b5)

When using the high-speed clock mode I2C-bus standard (400 kbps at maximum), set the FASTMODE bit to 1 (high-speed clock mode) and set fVIIC at 4 MHz or more.
The FASTMODE bit should not be rewritten during transmission/reception.

ACKBIT (ACK bit) (b6)

The ACK bit is enabled when the I2C interface is a master-receiver or slave-receiver. It is also enabled when receiving a slave address. When receiving a slave address, the SDAMM pin level during the ACK clock pulse is determined by the combination of bits ALS and ACKBIT in the S1D0 register and the received slave address.
When receiving data, the SDAMM pin level during the ACK clock pulse is determined by the ACKBIT bit. Table 25.5 lists the SDAMM Pin Level during the ACK Clock Pulse.

Table 25.5 SDAMM Pin Level during the ACK Clock Pulse

Received Content	ALS Bit in the S1D0 Register	ACKBIT Bit in the S20 Register	Slave Address Content	SDAMM Pin Level at ACK Clock
Slave Address	0	0	Matched with bits SAD6 to SAD0 in any of registers S0D0 to S0D2	L (ACK)
			0000000b	L (ACK)
			Others	H (NACK)
		1	—	H (NACK)
	1	0	—	L (ACK)
		1	—	H (NACK)
Data	—	0	—	L (ACK)
		1	—	H (NACK)

ACKCLK (ACK Clock Bit) (b7)

When the ACKCLK bit is 1 (ACK clock presents), an ACK clock is generated immediately after one-byte data is transmitted or received (8 clocks).
When the ACKCLK bit is 0 (no ACK clock), no ACK clock is generated after one-byte data is transmitted or received (8 clocks). At the falling edge of the data transmission/reception (the falling edge of the 8th clock), the IR bit in the IICIC register becomes 1 (interrupt requested).
The ACKCLK bit should not be rewritten during transmission/reception.

25.2.6 I2C0 Start/Stop Condition Control Register (S2D0)

I2C0 Start/Stop Condition Control Register

b7 b6 b5 b4 b3 b2 b1 b0	Symbol	Address	After Reset
	S2D0	02B5h	0001 1010b

Bit Symbol	Bit Name	Function	RW
SSC0	Start/stop condition setting bit	Refer to "SSC4 to SSC0 (Start/Stop Condition Setting Bit)" in the same page	RW
SSC1			RW
SSC2			RW
SSC3			RW
SSC4			RW
SIP	SCL/SDA interrupt pin polarity select bit	0: Falling edge 1: Rising edge	RW
SIS	SCL/SDA interrupt pin select bit	0: SDAMM 1: SCLMM	RW
STSPSEL	Start/stop condition generation select bit	0: Short setup/hold time mode 1: Long setup/hold time mode	RW

SSC4-SSC0 (Start/Stop Condition Setting Bit) (b4-b0)

Bits SSC4 to SSC0 select the start/stop condition detect condition (SCL open time, setup time, hold time) in standard clock mode. Refer to 25.3.7 “Start Condition and Stop Condition Detection”.
Do not set odd values or 00000b to bits SSC4 to SSC0.

SIP (SCL/SDA Interrupt Pin Polarity Select Bit) (b5)

SIS (SCL/SDA Interrupt Pin Select Bit) (b6)

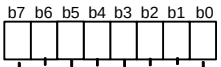
The IR bit in the SCLDAIC register is set to 1 (interrupt requested) when the I2C interface detects the edge selected by the SIP bit for the pin signal selected by the SIS bit. Refer to 25.4 “Interrupts”.

STSPSEL (Start/Stop Condition Generation Select Bit) (b7)

Refer to Table 25.13 “Setup/Hold Time for Start/Stop Condition Generation”.
If the fVIIC frequency is more than 4 MHz, set the STSPSEL bit to 1 (long mode).

25.2.7 I2C0 Control Register 1 (S3D0)

I2C0 Control Register 1



Symbol	Address	After Reset
S3D0	02B6h	0011 0000b

Bit Symbol	Bit Name	Function	RW
SIM	Stop condition detect interrupt enable bit	0: I2C-bus interrupt by stop condition detection is disabled 1: I2C-bus interrupt by stop condition detection is enabled	RW
WIT	Data receive interrupt enable bit	When write, 0: I2C-bus interrupt at 8th clock is disabled 1: I2C-bus interrupt is enabled at 8th clock When read, internal WAIT bit monitor 0: I2C-bus interrupt by falling edge of ACK clock 1: I2C-bus interrupt at 8th clock	RW
PED	SDAMM/port function select bit	0: SDAMM I/O pin 1: Port output pin	RW
PEC	SCLMM/port function select bit	0: SCLMM I/O pin 1: Port output pin	RW
SDAM	Internal SDA output monitor bit	0: Logic 0 output 1: Logic 1 output	RO
SCLM	Internal SCL output monitor bit	0: Logic 0 output 1: Logic 1 output	RO
ICK0	I2C-bus system clock select bit (Enabled when bits ICK4 to ICK2 in the S4D0 register are 000b)	b7 b6 0 0: fIIC divided by 2 0 1: fIIC divided by 4 1 0: fIIC divided by 8 1 1: Should not be set	RW
ICK1			RW

Do not use the bit managing instruction (read-modify-write instruction) to access the S3D0 register. Use MOV instruction to write to the S3D0 register.

SIM (Stop Condition Detect Interrupt Enable Bit) (b0)

When the SIM bit is 1 (I2C-bus interrupt by stop condition detection enabled) and a stop condition is detected, the SCPIN bit in the S4D0 register becomes 1 (stop condition detect interrupt requested) and the IR bit in the IICIC register becomes 1 (interrupt requested).

WIT (Data Receive Interrupt Enable Bit) (b1)

The WIT bit is enabled when the I2C interface is a master-receiver or slave-receiver.
The WIT bit has two functions.

- Select the I2C-bus interrupt timing when data is received. (write)
- Monitor the state of the internal WAIT flag. (read)

The WIT bit can select whether to generate an I2C-bus interrupt request at eighth clock (before ACK clock) during the data reception.
When the ACKCLK bit in the S20 register is 1 (ACK clock) and the WIT bit is set to 1 (enable I2C-bus interrupt at 8th clock), an I2C-bus interrupt request is generated at the eighth clock (before ACK clock). Then, the PIN bit in the S10 register becomes 0 (interrupt requested).
When the ACKCLK bit in the S20 register is 0 (no ACK clock), write a 0 to the WIT bit to disable the I2C-bus interrupt by data reception.
During data transmission and slave address reception, any interrupt request will not be generated at the eighth clock (before ACK clock) regardless of the value written to the WIT bit.
Reads of the WIT bit returns the internal WAIT flag status.
The I2C-bus interrupt request is generated at the falling edge of the ninth clock (ACK clock) regardless of the value written to the WIT bit. Then, the PIN bit in the S10 register becomes 0 (interrupt requested).
Therefore, read the internal WAIT flag status to determine whether the I2C-bus interrupt request is generated at eighth clock (before ACK clock) or at the falling edge of the ACK clock.
When a 1 is written to the WIT bit to enable the I2C-bus interrupt by data reception, the internal WAIT flag changes under the following condition.
Condition to become 0:

- The S20 register (ACKBIT bit) is written.

Condition to become 1:

- The S00 register is written.

During data transmission and slave address reception, the internal WAIT flag is 0 and the I2C-bus interrupt request will be generated only at the falling edge of the ninth clock (ACK clock), regardless of the value written to the WIT bit.
Table 25.6 lists an interrupt request generation timing and the conditions to restart transmission/reception during data reception. Figure 25.4 shows Interrupt Request Generation Timing in Receive Mode.

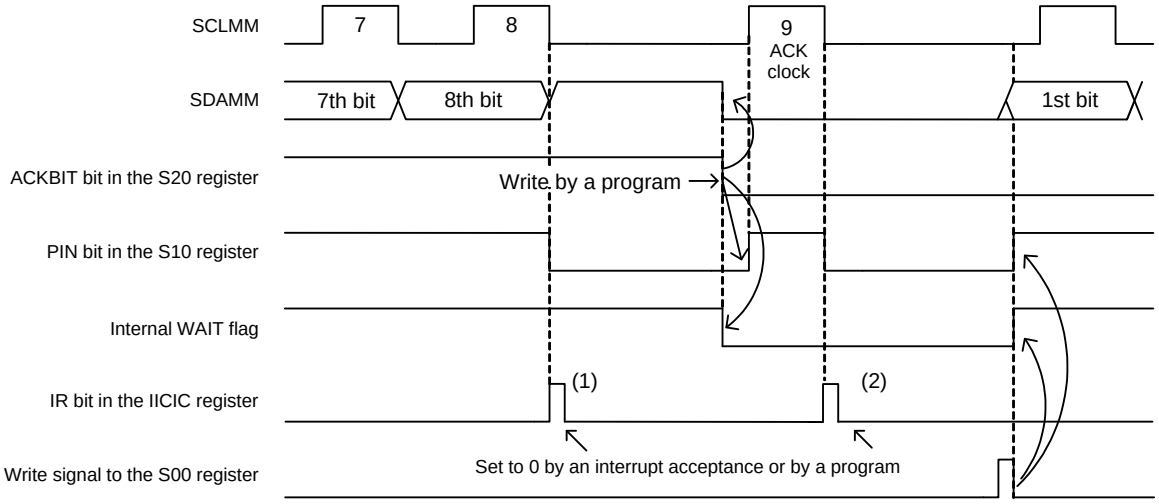
Table 25.6 Generating Interrupt Request and Restarting Transmission/Reception During Data Reception

I2C-bus Interrupt Request Generation Timing	Internal WAIT Flag Status	Conditions to Restart Transmission/Reception
At the falling edge of 8th clock of data (before the ACK clock) (1)	1	Write to the ACKBIT bit in the S20 register (3)
At the falling edge of 9th clock (ACK clock) (2)	0	Write to the S00 register

Notes:

1. See the timing of (1) on the IR bit in the IICIC register in Figure 25.4.
2. See the timing of (2) on the IR bit in the IICIC register in Figure 25.4.
3. Do not change the value of the bits other than ACKBIT bit in the S20 at this time. Also, do not write to the S00 register.

When setting the WIT bit to 1 in receive mode, and ACK clock is present:
(I2C-bus interrupt is enabled at 8th clock)



When setting the WIT bit to 0 in receive mode, and ACK clock is present:
(I2C-bus interrupt is disabled at 8th clock)

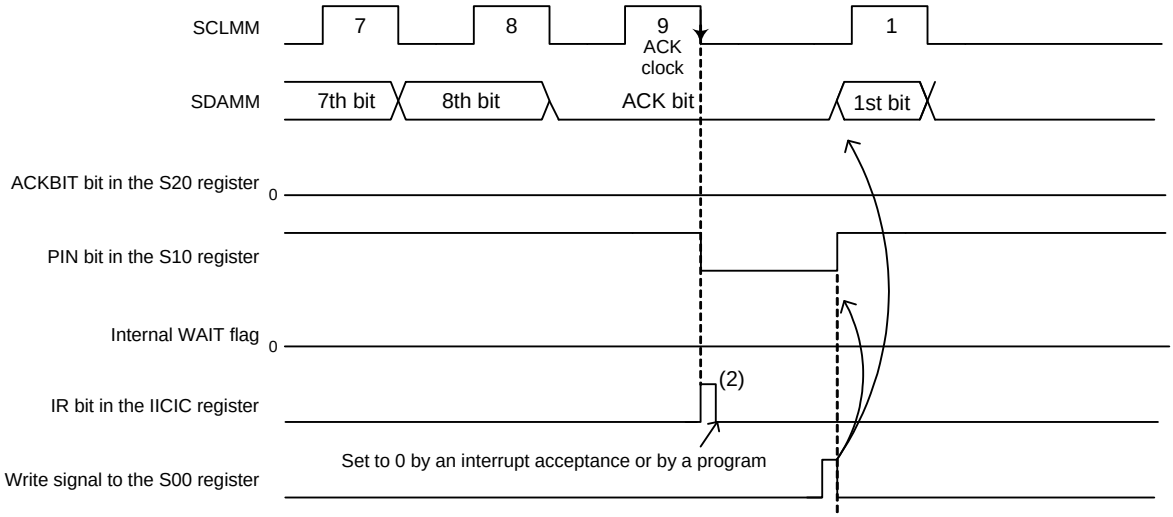


Figure 25.4 Interrupt Request Generation Timing in Receive Mode

PED (SDAMM Port Function Switch Bit) (b2)
PEC (SCLMM Port Function Switch Bit) (b3)

Bits PEC and PED are enabled when the ES0 bit in the S1D0 register is set to 1 (I2C interface enabled).
When the PEC bit is set to 1 (output port), the P7_1 bit value is output from the SCLMM pin regardless of the internal SCL output signal and PD7_1 bit value. When the PED bit is set to 1 (output port), the P7_0 bit value is output from the SDAMM pin regardless of the internal SDA output signal and PD7_0 bit value.
The signal level on the bus is input to the internal SDA and internal SCL.
When bits P7_1 to P7_0 in the P7 register are read after setting bits PD7_1 and PD7_0 in the PD7 register to 0 (input mode), the level on the bus can be read regardless of the setting values of bits PED and PEC. Table 25.7 lists SCLMM and SDAMM Pin Functions.

Table 25.7 SCLMM and SDAMM Pin Functions

Pin	S1D0 Register	S3D0 Register		Pin Function
	ES0 bit	PED bit	PEC bit	
P7_1/SCLMM	0	-	-	I/O port or other peripheral pins
	1	-	0	SCLMM (SCL input/output)
		-	1	Output port (output P7_1 bit value)
P7_0/SDAMM	0	-	-	I/O port or other peripheral pins
	1	0	-	SDAMM (SDA input/output)
		1	-	Output port (output P7_0 bit value)

–: 0 or 1

SDAM (Internal SDA Output Monitor Bit) (b4)
SCLM (Internal SCL Output Monitor Bit) (b5)

The internal SDA and SCL output signal levels are the same as the output level of the I2C interface before it has any effect from the external device output. Bits SDAM and SCLM are read only bits. Should be written with 0.

ICK1-ICK0 (I2C bus System Clock Select Bit) (b7-b6)

Bits ICK1 to ICK0 should be rewritten when the ES0 bit in the S1D0 register is 0 (I2C interface disabled). The fVIIC is selected by setting all the bits ICK1 to ICK0, bits ICK4 to ICK2 in the S4D0 register, and the PCLK0 bit in the PCLKR register. Refer to 25.3.1.2 “Bit Rate and Duty Cycle”.

Table 25.8 I2C-bus System Clock Select Bits

S4D0 Register			S3D0 Register		fVIIC
ICK4 Bit	ICK3 Bit	ICK2 Bit	ICK1 Bit	ICK0 Bit	
0	0	0	0	0	fIIC divided-by-2
0	0	0	0	1	fIIC divided-by-4
0	0	0	1	0	fIIC divided-by-8
0	0	1	–	–	fIIC divided-by-2.5
0	1	0	–	–	fIIC divided-by-3
0	1	1	–	–	fIIC divided-by-5
1	0	0	–	–	fIIC divided-by-6

–: 0 or 1
Do not set any combination other than the above.

25.2.8 I2C0 Control Register 2 (S4D0)

I2C0 Control Register 2

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S4D0	02B7h	00b

Bit Symbol	Bit Name	Function	RW
TOE	Timeout detect function enable bit	0: Disabled 1: Enabled	RW
TOF	Timeout detect flag	0: Not detected 1: Detected	RO
TOSEL	Timeout detect time select bit	0: Long time 1: Short time	RW
ICK2	I2C-bus system clock select bit	b5 b4 b3 0 0 0: Bits ICK1 and ICK0 in the S3D0 register are enabled 0 0 1: fIIC divided by 2.5 0 1 0: fIIC divided by 3 0 1 1: fIIC divided by 5 1 0 0: fIIC divided by 6 Do not set other than the above values.	RW
ICK3			RW
ICK4			RW
MSLAD	Slave address compare bit	0: S0D0 register only 1: Registers S0D0 to S0D2	RW
SCPIN	Stop condition detect interrupt request bit	0: I2C-bus interrupt not requested 1: I2C-bus interrupt requested	RW

TOE (Timeout Detect Function Enable Bit) (b0)

The TOE bit enables the timeout detect function. Refer to 25.3.9 “Timeout Detection” for details.

TOF (Timeout Detect Flag) (b1)

The TOF bit is enabled when the TOE is set to 1. When the TOF bit is set to 1 (detected), the IR bit in the IICIC register is set to 1 (requested) at the same time.

Condition to become 0:

- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Condition to become 1:

- The BB bit in the S10 register is set to 1 (bus busy) and the SCLMM high period is greater than the timeout detect period.

TOSEL (Timeout Detection Period Select Bit) (b2)

The TOSEL bit selects timeout detection period. The TOSEL bit is enabled when the TOE bit is 1 (timeout detect function enabled).
When long time is selected, the internal counter increments fVIIC as a 16-bit counter. when short time is selected, it increments fVIIC as a 14-bit counter. Therefore, timeout detect period is as follows.
When the TOSEL bit is set to 0 (long time),

$$65536 \times \frac{1}{\text{fVIIC}}$$

When the TOSEL bit is set to 1 (short time),

$$16384 \times \frac{1}{\text{fVIIC}}$$

Table 25.9 lists Timeout Detect Period.

Table 25.9 Timeout Detect Period

fVIIC	Timeout Detect	
	TOSEL Bit: 0 (Long time)	TOSEL bit: 1 (Short time)
4 MHz	16.4 ms	4.1 ms
2 MHz	32.8 ms	8.2 ms
1 MHz	65.6 ms	16.4 ms

ICK4-ICK2 (I2C bus System Clock Select Bit) (b5-b3)

Bits ICK4 to ICK2 should be rewritten when the ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
The fVIIC is selected by setting all the bits ICK4 to ICK2, bits ICK1 to ICK0 in the S3D0 register, and the PCLK0 bit in the PCLKR register. Refer to Table 25.8 “I2C-bus System Clock Select Bits” and 25.3.1.2 “Bit Rate and Duty Cycle”.

MSLAD (Slave Address Control Bit) (b6)

The MSLAD bit is enabled when the ALS bit in the S1D0 register is set to 0 (addressing format). The MSLAD bit selects the S0Di register (i = 0 to 2) that is used for address match detection.

SCPIN (Stop Condition Detect Interrupt Request Bit) (b7)

The SCPIN bit is enabled when the SIM bit in the S3D0 register is set to 1 (enable I2C-bus interrupt by stop condition detection).
Condition to become 0:

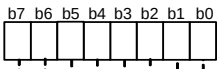
- Writing a 0 by a program.

Condition to become 1:

- Stop condition is detected
  (writing a 1 by a program has no effect).

25.2.9 I2C0 Status Register 0 (S10)

I2C0 Status Register 0



Symbol	Address	After Reset
S10	02B8h	0001 000Xb

Bit Symbol	Bit Name	Function	RW
LRB	Last receive bit	When read, 0: Last bit = 0 1: Last bit = 1 When write, refer to Table 24.10 Functions enabled by S10 register.	RW
ADR0	General call detection flag	When read, 0: Not detected 1: Detected When write, refer to Table 24.10 Functions enabled by S10 register.	RW
AAS	Slave address compare flag	When read, 0: No address matched 1: Address matched When write, refer to Table 24.10 Functions enabled by S10 register.	RW
AL	Arbitration lost detection flag	When read, 0: Not detected 1: Detected When write, refer to Table 24.10 Functions enabled by S10 register.	RW
PIN	I2C bus interface interrupt request bit	When read, 0: Interrupt requested 1: No interrupt requested When write, refer to Table 24.10 Functions enabled by S10 register.	RW
BB	Bus busy flag	When read, 0: Bus free 1: Bus busy When write, refer to Table 24.10 Functions enabled by S10 register.	RW
TRX	Communication mode select bit 0	0: Receive mode 1: Transmit mode	RW
MST	Communication mode select bit 0	0: Slave mode 1: Master mode	RW

Do not use the bit managing instruction (read-modify-write instruction) to access the S10 register. Use MOV instruction to write to the S10 register.

Bit 5 to bit 0 in the S10 register (six lower bits) monitors the state of the I2C interface. The bit values cannot be changed by a program. However, a write to the S10 register, including the six lower bits, is used to generate start/stop condition.

Bits MST and TRX are read and write bits. To change bits MST or TRX without generating the start/stop condition, set 1111b to four lower bits in the S10 register.

Table 21.10 lists the functions enabled by write access to the S10 register. Do not write other than the values listed in Table 21.10. If the values listed in Table 21.10 are written to the S10 register, six lower bits in the S10 register will not be changed.

Table 25.10 Functions Enabled by Writing to the S10 Register

Bit Setting of the S10 Register								Function
MST	TRX	BB	PIN	AL	AAS	ADR0	LRB	
1	1	1	0	0	0	0	0	Sets the I2C interface to start condition standby state in master transmit/receive mode
1	1	0	0	0	0	0	0	Sets the I2C interface to stop condition standby state in master transmit/receive mode
0/1	0/1	–	0	1	1	1	1	Selects communication mode

–: 0 or 1

Refer to 25.3.2 “Generation of Start Condition” and 25.3.3 “Generation of Stop Condition” for start/stop condition generation.

LRB (Last Receive Bit) (b0)

The LRB bit function in read access is described as follows. See Table 25.10 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.
The LRB bit stores the last bit value of the received data. It is used to check whether the ACK is received.
Condition to become 0:

- An ACK response is sent from a receiver at ACK clock.
- The ACKCLK bit is set to 0 (no ACK clock) and the last bit value is 0.
- The S00 register is written.

Condition to become 1:

- No ACK response is sent from a receiver at ACK clock.
- The ACKCLK bit is set to 0 (no ACK clock) and the last bit value is 1.

ADR0 (General Call Detection Flag) (b1)

The ADR0 bit function in read access is described as follows. See Table 25.10 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.
Condition to become 0:

- Stop condition is detected.
- Start condition is detected.
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Condition to become 1:

- The ALS bit in the S1D0 register is set to 0 (addressing format) and the received slave address is 0000000b (general call) in slave mode.

AAS (Slave Address Compare Flag) (b2)

The AAS bit function in read access is described as follows. See Table 25.10 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

Condition to become 0:

- The S00 register is written.
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Condition to become 1:

- In slave-receiver mode, the ALS bit in the S1D0 register is set to 0 (addressing format) and the received slave address is matched with bits SAD6 to SAD0 in any of registers S0D0 to S0D2.
- In slave-receiver mode, the ALS bit in the S1D0 register is set to 0 (addressing format) and the general call address (0000000b) is received.

AL (Arbitration Lost Detection Flag) (b3)

The AL bit function in read access is described as follows. See Table 25.10 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.

Condition to become 0:

- The S00 register is written.
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Condition to become 1:

- In master-transmitter mode or master-receiver mode, the SDAMM pin level changes to low by an external device, not by the ACK clock, when slave address is transmitted.
- The SDAMM pin level changes to low by an external device for other than the ACK clock when data is transmitted in master-transmitter mode.
- In master-transmitter mode or master-receiver mode, the SDAMM pin level changes to low by an external device when start condition is transmitted.
- In master-transmitter mode or master-receiver mode, the SDAMM pin level changes to low by an external device when stop condition is transmitted.
- The function to avoid start condition overlaps is started.

PIN (I2C bus Interface Interrupt Request Bit) (b4)

The PIN bit function in read access is described as follows. See Table 25.10 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.
Condition to become 0:

- Slave address transmission is completed in master mode (including a case of detecting arbitration lost).
- One-byte data transmission is completed (including a case of detecting arbitration lost).
- One-byte data reception is completed (the falling edge of 8th clock is detected when the ACKCKL bit is set to 0. The falling edge of ACK clock when the ACKCKL bit is set to 1.).
- The WIT bit in the S3D0 register is set to 1 (I^2C-bus interrupt enabled at 8th clock) and 1-byte data is received (before ACK clock).
- In slave-receiver mode, the ALS bit in the S1D0 register is set to 0 (addressing format) and any of the slave address stored into bits SAD6 to SAD0 in the S0Di register (i = 0 to 2) is matched with the received slave address (slave address match).
- In slave-receiver mode, the ALS bit in the S1D0 register is set to 0 (addressing format) and the general call address (0000000b) is received.
- In slave-receiver mode, the ALS bit in the S1D0 register is set to 1 (free format) and the slave address reception is completed.

Condition to become 1:

- The S00 register is written.
- The S20 register is written (when the WIT bit is 1 and internal WAIT flag is 1).
- The ES0 bit in the S1D0 register is set to 0 (I^2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I^2C interface reset).

The IR bit in the IICIC register is set to 1 (interrupt requested) as soon as the PIN bit is set to 0 (I^2C-bus interrupt requested). When the PIN bit is set to 0, the SCLMM pin output level is low.
However, the SCLMM pin output level does not become low when all the following conditions are met.

- In master mode, when arbitration lost is detected by a slave address, the ALS bit in the S1D0 register is 0 (addressing format), and the received address not 0000000b (general call) does not match any of bits SAD6 to SAD0 in the registers S0D0 to S0D2.
- In master mode, when arbitration lost is detected by data, the ALS bit in the S1D0 register is 0 (addressing format), and the slave address not 0000000b (general call) does not match any of bits SAD6 to SAD0 in the registers S0D0 to S0D2.

BB (Bus Busy Flag) (b5)

The BB bit function in read access is described as follows. See Table 25.10 “Functions Enabled by Writing to the S10 Register” for the bit function in write access.
The BB bit indicates the state of the bus system, whether the bus is free or not. The BB bit changes depending on the SCLMM and SDAMM input signals, regardless of master mode or slave mode.
Condition to become 0:

- Stop condition is detected.
- The ES0 bit in the S1D0 register is set to 0 (I^2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I^2C interface reset).

Condition to become 1:

- Start condition is detected.

TRX (Communication Mode Select Bit 0) (b6)

The TRX selects transmit mode or receive mode.
Condition to become 0:

- The TRX bit is set to 0 by a program.
- Arbitration lost is detected.
- Stop condition is detected.
- Start condition overlap protect function is enabled.
- Start condition is detected when the MST bit in the S10 register is set to 0 (slave mode).
- No ACK is detected from a receiver when the MST bit in the S10 register is set to 0 (slave mode).
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Condition to become 1:

- The TRX bit is set to 1 by a program.
- The ALS bit in the S1D0 register is set to 0 (addressing format), the AAS bit is set to 1 (address matched) after receiving the slave address, and the received R/W bit is set to 1, in slave mode.

MST (Communication Mode Select Bit 1) (b7)

The MST bit selects master mode or slave mode.
Condition to become 0:

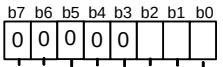
- The MST bit is set to 0 by a program.
- The one-byte data that lost arbitration is completed transmitting/receiving when arbitration lost is detected.
- Stop condition is detected.
- Start condition overlap protect function is enabled.
- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled.
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).

Condition to become 1:

- The MST bit is set to 1 by a program.

25.2.10 I2C0 Status Register 1 (S11)

I2C0 Status Register 1



Symbol	Address	After Reset
S11	02B9h	XXXX XXX0b

Bit Symbol	Bit Name	Function	RW
AAS0	Slave address 0 compare flag	0: No address matched 1: Address matched	RO
AAS1	Slave address 1 compare flag	0: No address matched 1: Address matched	RO
AAS2	Slave address 2 compare flag	0: No address matched 1: Address matched	RO
— (b7-b3)	Reserved bits	Set to 0	RO

AAS0 Bit (Slave Address 0 Compare Flag) (b0)
AAS1 Bit (Slave Address 1 Compare Flag) (b1)
AAS2 Bit (Slave Address 2 Compare Flag) (b2)

The AASi bit indicates the address match when the ALS bit in the S1D0 register is set to 0 (addressing format) and any of the slave address stored into bits SAD6 to SAD0 in the S0Di register (i = 0 to 2) is compared with the received slave address. The AASi bit is set to 1 when there is an address match or when a general call address is received.

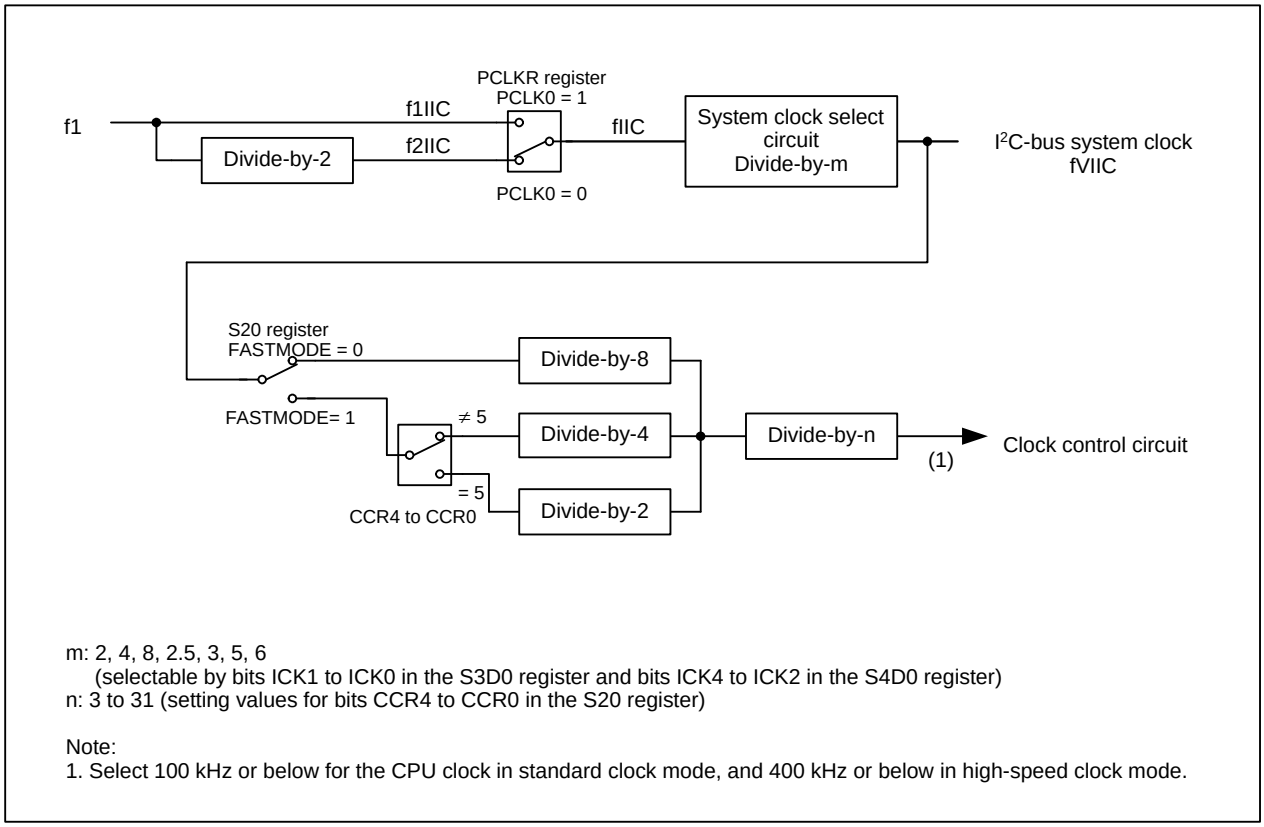
Bits AAS2 to AAS0 are set to 0 under the following conditions.

- The ES0 bit in the S1D0 register is set to 0 (I2C interface disabled).
- The IHR bit in the S1D0 register is set to 1 (I2C interface reset).
- The S00 register is written.

25.3 Operations

25.3.1 Clock

Figure 25.5 shows I2C-bus Interface Clock.



m: 2, 4, 8, 2.5, 3, 5, 6
(selectable by bits ICK1 to ICK0 in the S3D0 register and bits ICK4 to ICK2 in the S4D0 register)
n: 3 to 31 (setting values for bits CCR4 to CCR0 in the S20 register)

Note:
1. Select 100 kHz or below for the CPU clock in standard clock mode, and 400 kHz or below in high-speed clock mode.

Figure 25.5 I2C-bus Interface Clock

25.3.1.1 fVIIC

The fVIIC is determined by the setting combination of the following.

- The frequency of peripheral clock f1
- The PCLK0 bit in the PCLKR register
- Bits ICK1 to ICK0 in the S3D0 register
- Bits ICK4 to ICK2 in the S4D0 register

The fVIIC stops when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

Refer to Table 25.8 “I2C-bus System Clock Select Bits” for details.

25.3.1.2 Bit Rate and Duty Cycle

Bit rate is determined by the setting combination of the fVIIC and bits CCR4 to CCR0 in the S20 register.

Table 25.11 lists Bit Rate of Internal SCL Output and Duty Cycle. Even if there is a change in duty cycle, the bit rate does not change. The bit rate and duty cycle described here are the ones before the I2C interface have any effect from the SCL output of external device.

Table 25.11 Bit Rate of Internal SCL Output and Duty Cycle

Item	Standard Clock Mode	High-Speed Clock Mode (CCR value = other than 5)	High-Speed Clock Mode (CCR value = 5)
Bit rate (bps)	$\frac{fVIIC}{8 \times CCR\ value}$	$\frac{fVIIC}{4 \times CCR\ value}$	$\frac{fVIIC}{2 \times CCRvalue} = \frac{fVIIC}{10}$
Duty cycle	50% (1)	50% (2)	35 to 45%

CCR value: Setting value of bits CCR4 to CCR0

Notes:
1. Fluctuation of high level: -4 to +2 fVIIC cycles
2. Fluctuation of high level: -2 to +2 fVIIC cycles

When the setting value (CCR value) of bits CCR4 to CCR0 is 5 (00100b) in high-speed clock mode, the maximum bit rate should be 400 kbps in high-speed clock mode.

The bit rate and duty cycle are as follows.

- Bit rate:

$$\frac{fVIIC}{2 \times CCR\ value} = \frac{fVIIC}{10}$$

When fVIIC is 4 MHz, the bit rate is 400 kbps.

- Duty cycle is 35 to 45%

Even if the bit rate is 400 kbps, the minimum low period of SCLMM clock of 1.3 μs (I2C-bus standard) is ensured.

Table 25.12 lists Bit Setting of Bits CCR4 to CCR0 and Bit Rate (fVIIC = 4 MHz).

Table 25.12 Bit Setting of Bits CCR4 to CCR0 and Bit Rate (fVIIC = 4 MHz)

Bits CCR4 to CCR0 in the S20 Register					Bit Rate (kbps)	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard Clock Mode	High-Speed Clock Mode
0	0	0	0	0	Do not set (1)	Do not set (1)
0	0	0	0	1	Do not set (1)	Do not set (1)
0	0	0	1	0	Do not set (1)	Do not set (1)
0	0	0	1	1	Do not set (2)	333
0	0	1	0	0	Do not set (2)	250
0	0	1	0	1	100	400
0	0	1	1	0	83.3	166
:	:	:	:	:	:	:
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Notes:
1. Bits CCR4 to CCR0 should not be set to 0 to 2 regardless of the fVIIC frequency.
2. The maximum bit rate is 100 kbps in standard clock mode and 400 kbps in high-speed clock mode. Do not exceed the maximum bit rate.

25.3.1.3 Slave Address Receive in Wait Mode and Stop Mode

When the CM02 bit in the CM0 register is set to 0 (peripheral clock f1 does not stop in wait mode) and wait mode is entered, the I2C interface receives slave address even in wait mode.

When the CM02 bit in the CM0 register is set to 1 (peripheral clock f1 stops in wait mode), and wait mode, stop mode, or low-power consumption mode is entered, the I2C interface stops operating because fVIIC also stops.

The SCL/SDA interrupt can be used in both wait mode and stop mode.

25.3.2 Generation of Start Condition

Follow the procedure below when the ES0 bit in the S1D0 register is 1 (I2C interface enabled) and the BB bit in the S10 register is set to 0 (bus free). Figure 25.6 shows Start Condition Generation Procedure.

(1) Write “E0h” to the S10 register.
The I2C interface enters the start condition standby state and the SDAMM pin is left open.

(2) Write a slave address to the S00 register.
A start condition is generated. Then, the bit counter becomes 000b, the SCL clock signal is output for one byte, and the slave address is transmitted.

Write access to the S10 register is disabled during 1.5 fVIIC cycles after a stop condition is generated and the BB bit becomes 0 (bus free). Therefore, when writing E0h to the S10 register and a slave address to the S00 register during the 1.5 fVIIC cycles, start condition standby state is not entered, and a start condition is not generated accordingly.
When generating a start condition immediately after the falling edge of the BB bit, check both TRX and MST bits are 1 after the procedure (1), and then execute the procedure (2).

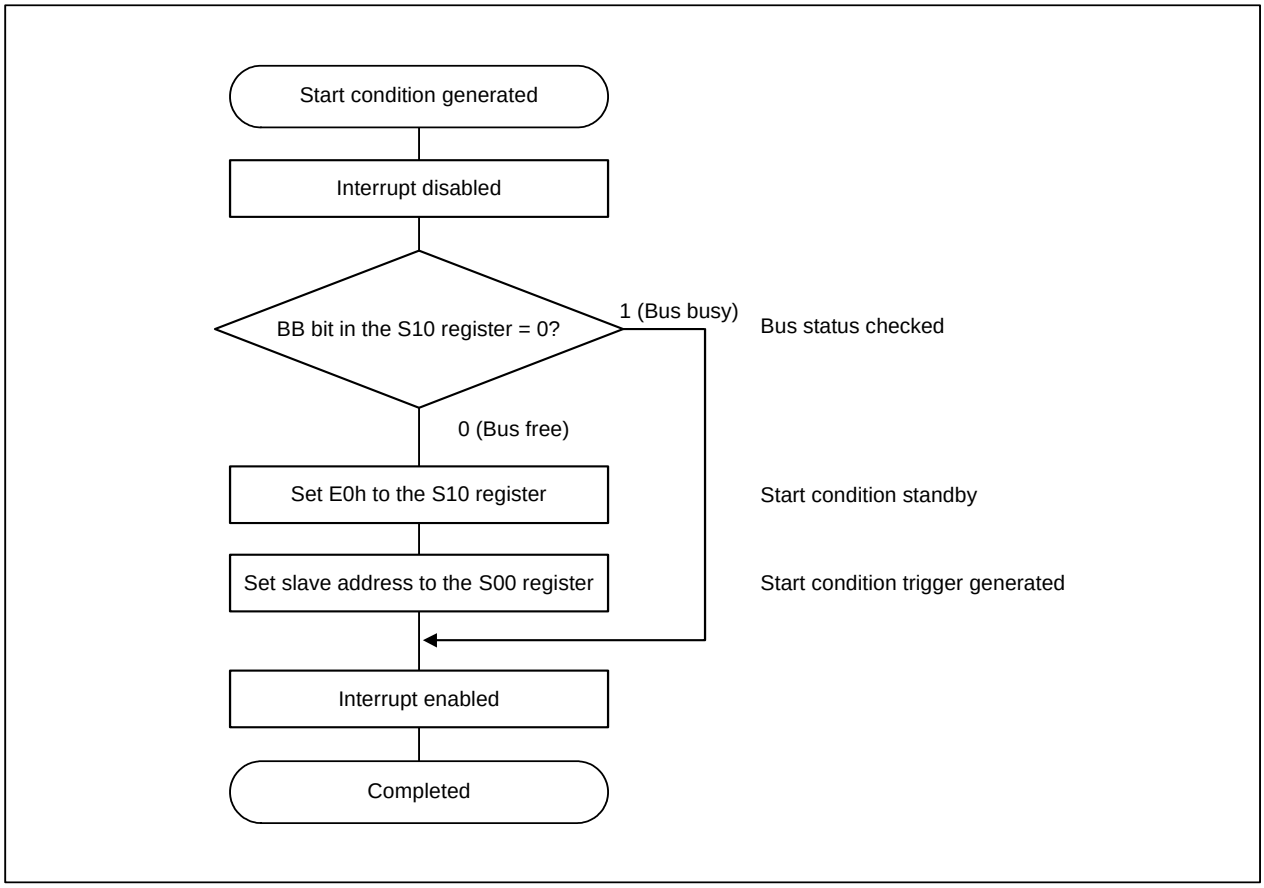


Figure 25.6 Start Condition Generation Procedure

The start condition generation timing depends on the modes (standard clock mode or high-speed clock mode). Figure 25.7 shows Start Condition Generation Timing.
Table 25.13 lists Setup/Hold Time for Start/Stop Condition Generation.

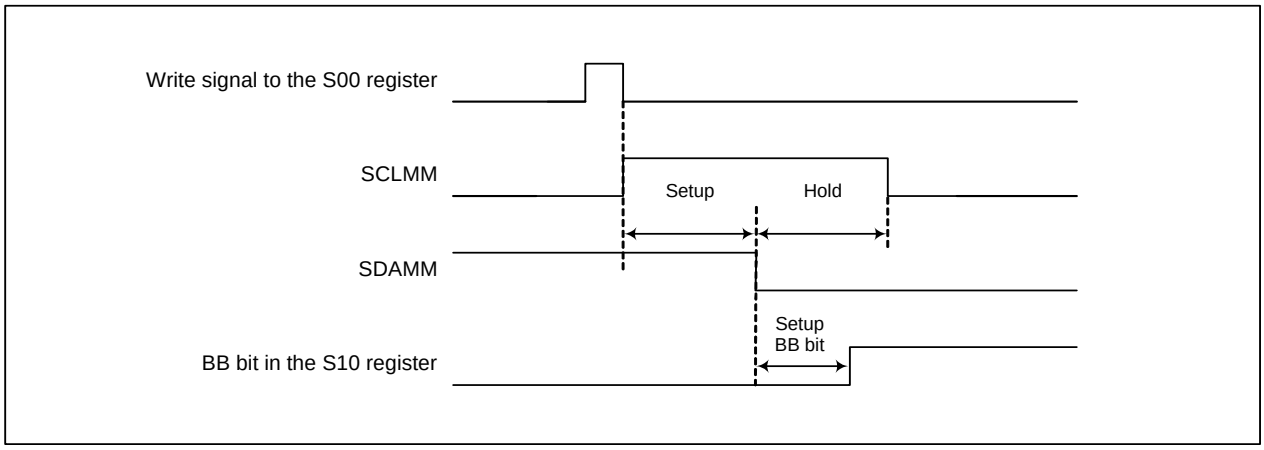


Figure 25.7 Start Condition Generation Timing

Table 25.13 Setup/Hold Time for Start/Stop Condition Generation

Item	STSPSEL Bit	Standard Clock Mode		High-speed Clock Mode	
		fVIIC cycles	fVIIC = 4 MHz	fVIIC cycles	fVIIC = 4MHz
Setup time	0 (short mode)	20	5.0 µs	10	2.5 µs
	1 (long mode)	52	13.0 µs	26	6.5 µs
Hold time	0 (short mode)	20	5.0 µs	10	2.5 µs
	1 (long mode)	52	13.0 µs	26	6.5 µs
BB bit set/ reset time	-	$\frac{\text{SSC value} - 1}{2} + 2$	3.375 µs (1)	3.5	0.875 µs

-: 0 or 1
STSPSEL: Bit in the S2D0 register
SSC value: Value of bits SSC4 to SSC0 in the S2D0 register
Note:
1. Example value when bits SSC4 to SSC0 are 11000b.

25.3.3 Generation of Stop Condition

Follow the procedure below when the ES0 bit in the S1D0 register is 1 (I2C interface enabled).

(1) Write C0h to the S10 register.
The I2C interface enters the stop condition standby state and the SDAMM pin is driven low.

(2) Write a dummy data to the S00 register.
A stop condition is generated.

The stop condition generation timing depends on the modes (standard clock mode or high-speed clock mode). Figure 25.8 shows Sop Condition Generation Timing. Refer to Table 25.13 “Setup/Hold Time for Start/Stop Condition Generation” for setup/hold time.

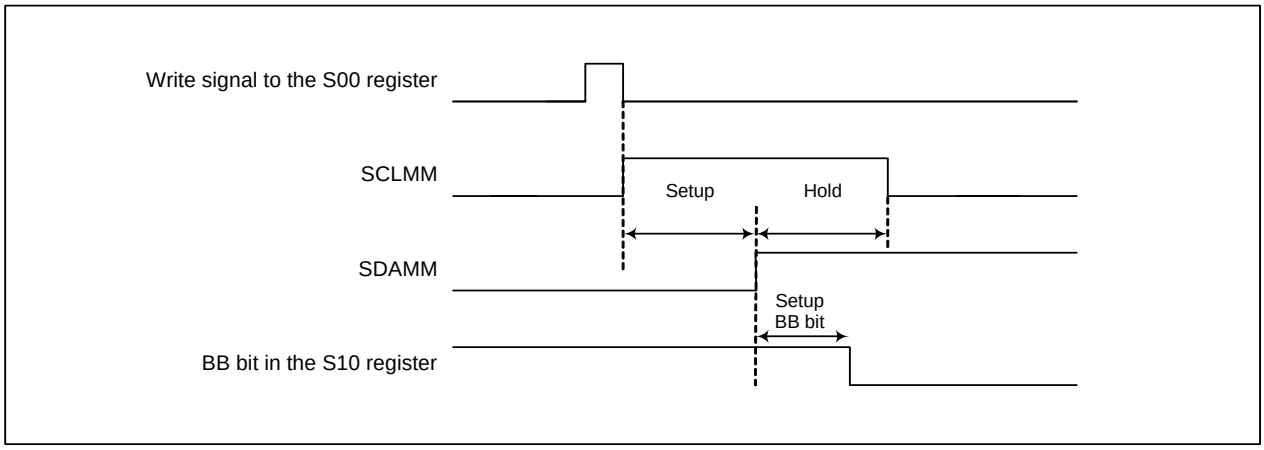


Figure 25.8 Sop Condition Generation Timing

The S10 register or S00 register should not be written until the BB bit in the S10 register becomes 0 (bus free) after the instructions to generate a stop condition (refer to above (2)) are executed.
If the SCLMM pin input signal becomes low until the BB bit in the S10 register becomes 0 (bus free) from the instruction to generate a stop condition is executed and the SCLMM pin becomes high-level, the internal SCL output becomes low. In this case, perform one of the procedures below to stop the low signal output from the SCLMM pin (leave the SCLMM pin open).

- Generate a stop condition (perform the procedures (1) and (2) described previously).
- Set the ES0 bit in the S1D0 register to 0 (I2C interface disabled).
- Write a 1 to the IHR bit (I2C interface reset).

25.3.4 Generation of Restart Condition

Follow the procedure below to generate a restart condition when one-byte data is transmitted/received.

(1) Write E0h to the S10 register. (Start condition standby state. SDAMM pin becomes high-impedance.)
(2) Wait until the SDAMM pin level becomes high.
(3) Write a slave address to the S00 register (a start condition trigger generated)

Figure 25.9 shows Restart Condition Generation Timing.

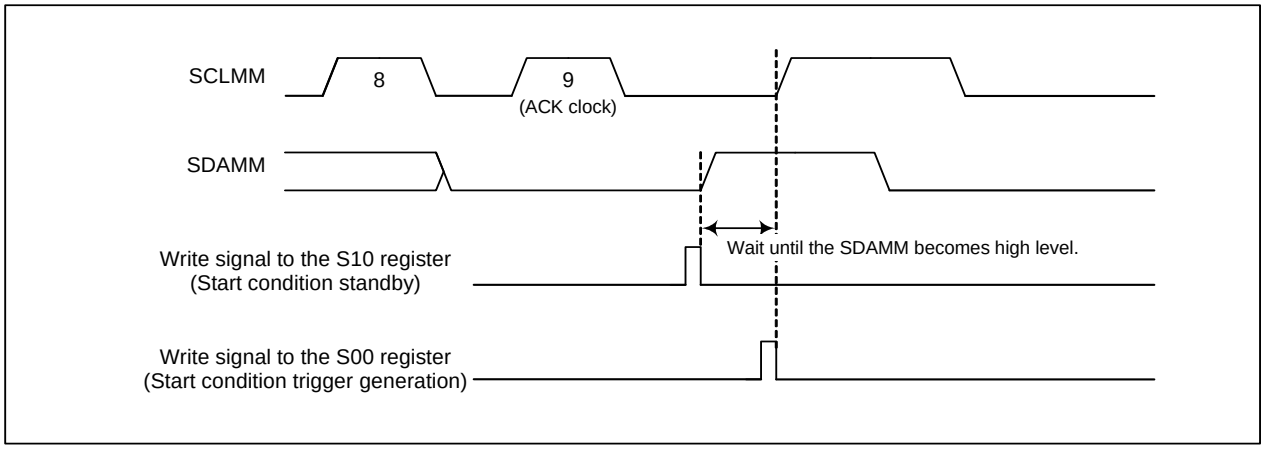


Figure 25.9 Restart Condition Generation Timing

25.3.5 Start Condition Overlap Protect

The I2C interface generates a start condition by setting registers S10 and S00 by a program. The bus system must be free before setting these registers. Check whether the bus is free with the BB bit in the S10 register by a program before setting the registers.
However, even if the bus system is checked free, other master devices may generate a start condition before setting registers S10 and S00. In this case, when the I2C interface detects the start condition, the BB bit becomes 1 (bus busy) and the start condition overlap protect function is performed.
The start condition overlap protect function operates as follows.

- The start condition standby state is not entered even if the S10 register is set to E0h.
- If the I2C interface is in the start condition standby state, exit the state.
- A start condition trigger is not generated even if a data is written to the S00 register by program.
- Bits MST and TRX in the S10 register are set to 0 (slave-receiver mode).
- The AL bit in the S10 register becomes 1 (arbitration lost detected).

Figure 25.10 shows Start Condition Overlap Protect Operation.

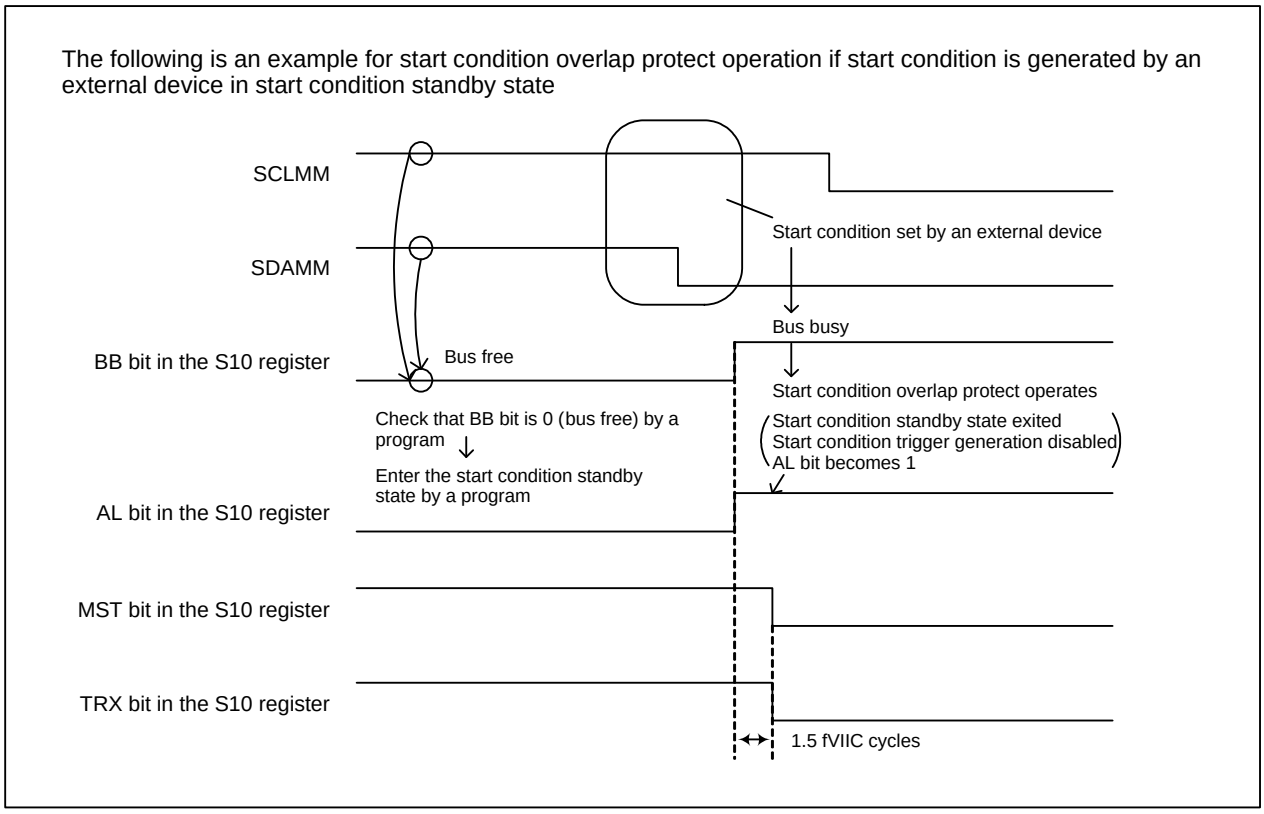


Figure 25.10 Start Condition Overlap Protect Operation

The start condition overlap protect is enabled from the falling edge of SDAMM (start condition) to the completion of the slave address receive. If data is written to register S10 and S00 during the period, the above operation is performed. Figure 25.11 shows Start Condition Overlap Protect Function Enable Period.

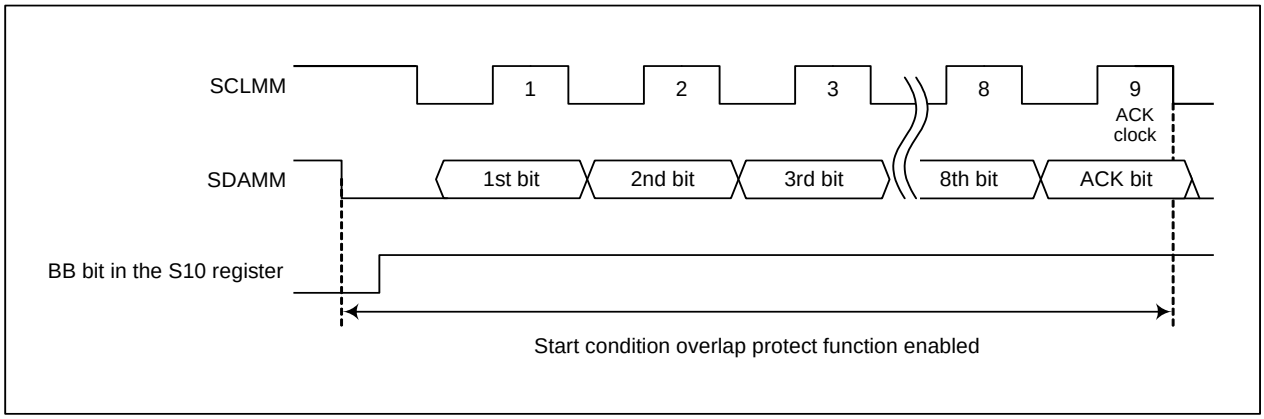


Figure 25.11 Start Condition Overlap Protect Function Enable Period

25.3.6 Arbitration Lost

When the following conditions are all met, the signal level of SDAMM pin becomes low by an external device and the I2C interface determines that it has lost arbitration.

(1) Transmit/receive (one of the following)
- Slave address transmit in master-transmitter mode or master-receiver mode
- Data transmit (ACK clock not included) in master-transmitter mode
- Start condition generated in master-transmitter mode or master-receiver mode
- Stop condition generated in master-transmitter mode or master-receiver mode

(2) Internal SDA output: High

(3) SDAMM pin level: Low (sampling at the rising edge of the clock of SCLMM pin.)

Figure 25.12 shows Operation Example When Arbitration Lost is Detected.

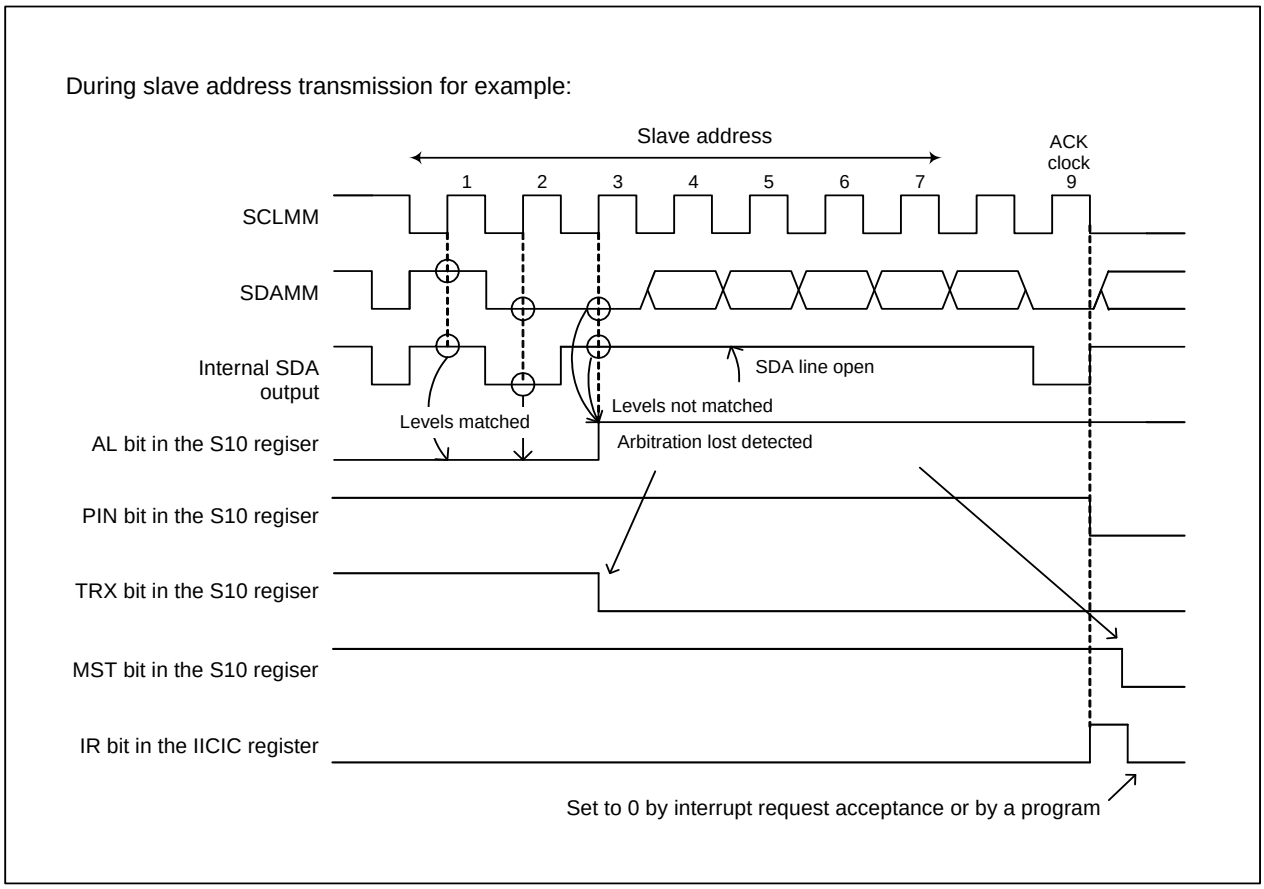


Figure 25.12 Operation Example When Arbitration Lost is Detected

When arbitration lost is detected,
- The AL bit in the S10 register becomes 1 (arbitration lost detected)
- Internal SDA output becomes high. (SDAMM becomes high-impedance)
- Slave-receiver mode is entered by setting the TRX bit in the S10 register to 0 (receive mode) and the MST bit in the S10 register to 0 (slave mode).

In order to write the AL bit to 0 again after arbitration lost is detected, set a value to the S00 register.

When arbitration is lost in slave address transmission, the I2C interface enters the slave-receiver mode automatically and receives slave address which sent from another master. When the ALS bit in the S1D0 register is 1 (addressing format), slave address comparison result is determined by reading bits ADR0 and AAS in the S10 register

When arbitration is lost during data transmission, slave-receiver mode is automatically entered.

25.3.7 Start Condition and Stop Condition Detection

Figure 25.13 shows Start Condition Detection, Figure 25.14 shows Stop Condition Detection, and Table 25.14 lists Conditions to Detect Start/Stop Condition.

Start/Stop condition is detected only when the start/stop condition detect conditions (SCL open time, setup time, and hold time) are selected by bits SSC4 to SSC0 in the S2D0 register, and the signals input to pins SCLMM and SDAMM meet all three conditions (SCLMM open time, setup time, and hold time) listed in Table 25.14.

The BB bit in the S10 register becomes 1 when a start condition is detected. It becomes 0 when a stop condition is detected. The set timing and reset timing of the BB bit depends on the mode, standard mode or high-speed clock mode. Refer to BB bit set/reset time in Table 25.15.

Table 25.15 lists Recommended SSCi (i = 0 to 4) Bit Value in Standard Clock Mode.

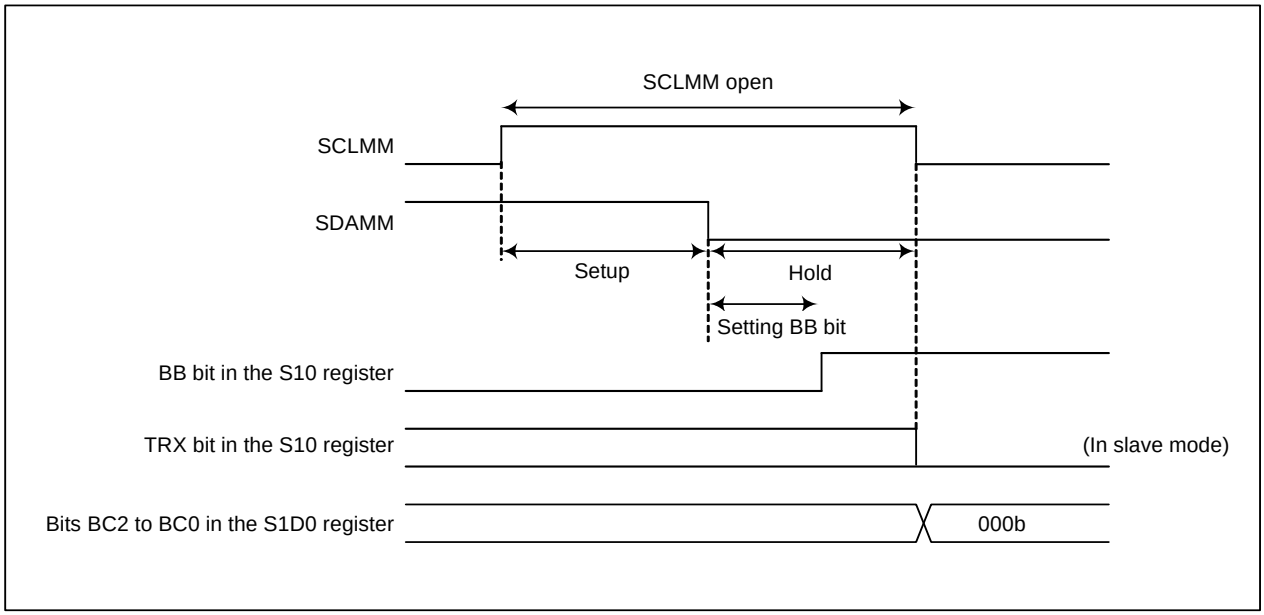


Figure 25.13 Start Condition Detection

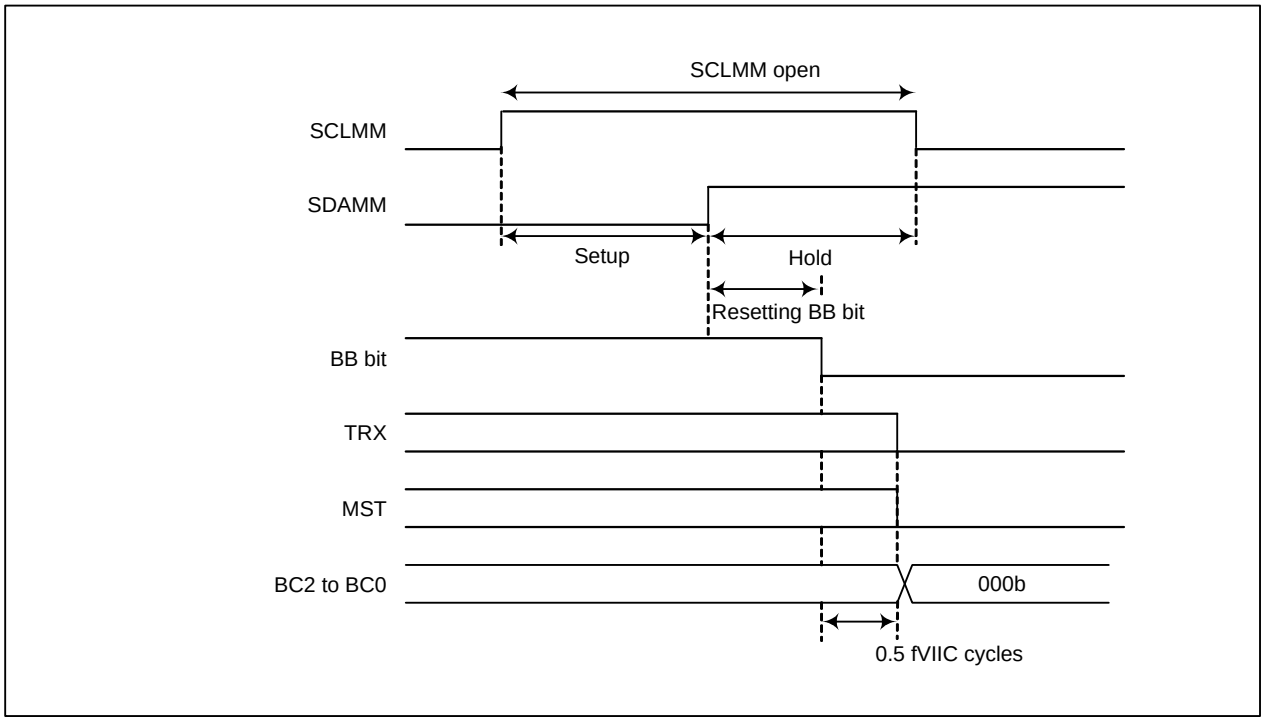


Figure 25.14 Stop Condition Detection

Table 25.14 Conditions to Detect Start/Stop Condition

	Standard Clock Mode	High-speed Clock Mode
SCLMM open time	SSC value + 1 cycle	4 cycles
Setup time	$\frac{\text{SSC value}}{2}$ + 1 cycles	2 cycles
Hold time	$\frac{\text{SSC value}}{2}$ cycles	2 cycles
BB bit set/ reset time	$\frac{\text{SSC value} - 1}{2}$ + 2 cycles	3.5 cycles

Unit: fVIIC cycles
SSC value: Value of bits SSC4 to SSC0 in the S2D0 register

Table 25.15 Recommended SSCi (i = 0 to 4) Bit Value in Standard Clock Mode

fVIIC	SSC Value (recommended)	Start/stop Condition			BB Bit Set/reset Time
		SCLMM Open Time	Setup Time	Hold Time	
5 MHz	11110b	6.2 µs (31)	3.2 µs (16)	3.0 µs (15)	4.125 µs (16.5)
4 MHz	11010b	6.75 µs (27)	3.5 µs (14)	3.25 µs (13)	3.625 µs (14.5)
	11000b	6.25 µs (25)	3.25 µs (13)	3.0 µs (12)	3.375 µs (13.5)
2 MHz	01100b	6.5 µs (13)	3.5 µs (7)	3.0 µs (6)	3.75 µs (7.5)
	01010b	5.5 µs (11)	3.0 µs (6)	2.5 µs (5)	3.25 µs (6.5)
1 MHz	00100b	5.0 µs (5)	3.0 µs (3)	2.0 µs (2)	3.5 µs (3.5)

SSC value: Value of bits SSC4 to SSC0 in the S2D0 register
( ): fVIIC cycles

25.3.8 Operation After Completion of Slave Address/Data Transmit/Receive

After completing transmission/reception of slave address or one-byte data, the PIN bit in the S10 register is set to 0 (interrupt requested) at the falling edge of ACK clock. The IR bit in the IICIC register becomes 1 (interrupt requested) at the same time. The value in the S10 register and so on changes depending on the state of transmit/receive data, and the level of pins SCLMM and SDAMM. Figure 25.15 shows Operation After Completion of Slave Address/Data Transmit/Receive.

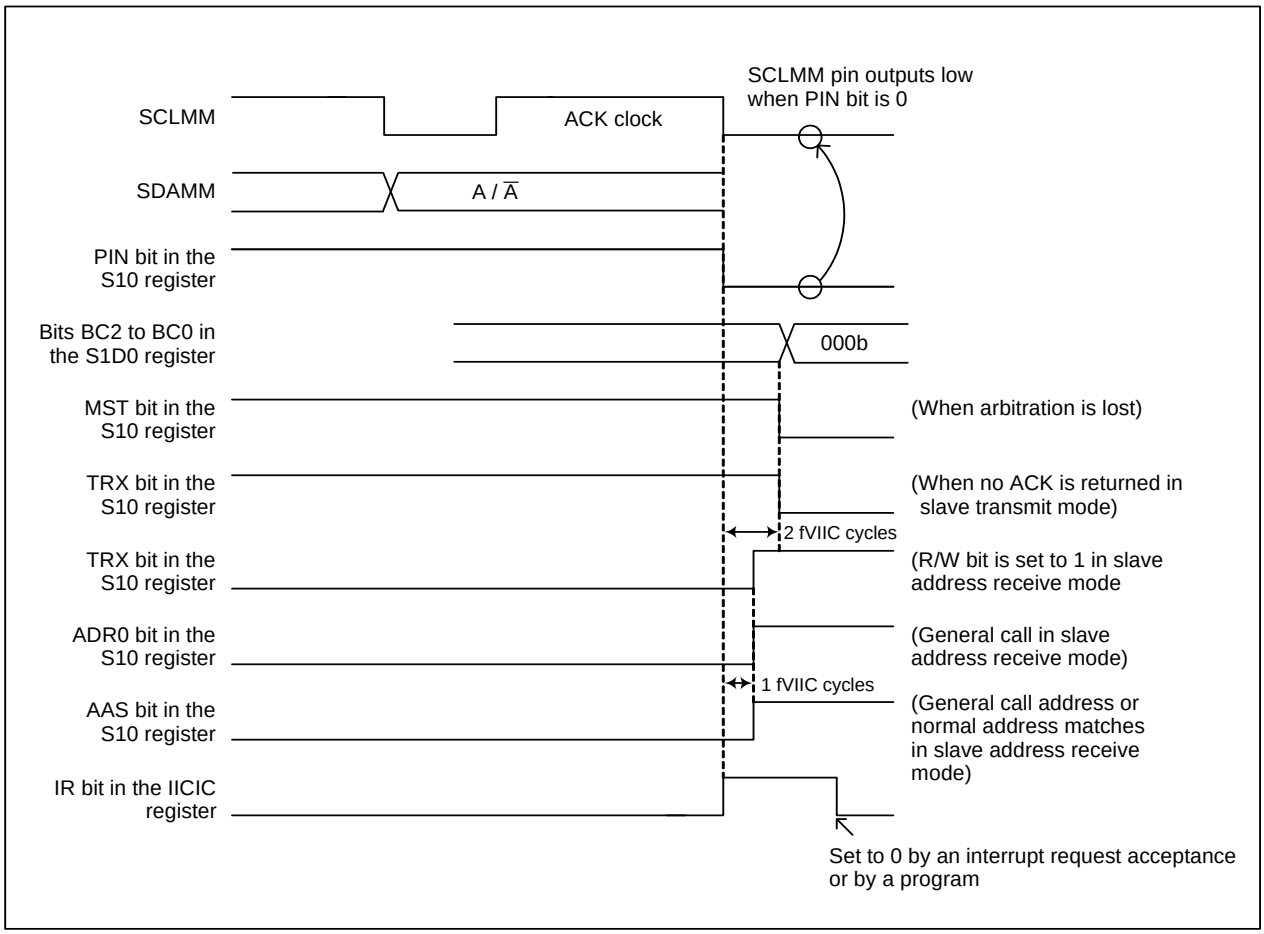


Figure 25.15 Operation After Completion of Slave Address/Data Transmit/Receive

25.3.9 Timeout Detection

If the SCL clock is stopped in transmit/receive mode, each device stops operating, keeping the communication state. Timeout detection is a function to detect timeout and generate an I2C-bus interrupt request when the SCLMM pin is driven high for more than the selected timeout detection period in transmit/receive mode. Figure 25.16 shows Timeout Detect Timing. Refer to "TOSEL (Timeout Detection Period Select Bit) (b2)" of 25.2.8 "I2C0 Control Register 2 (S4D0)" for timeout detection period.

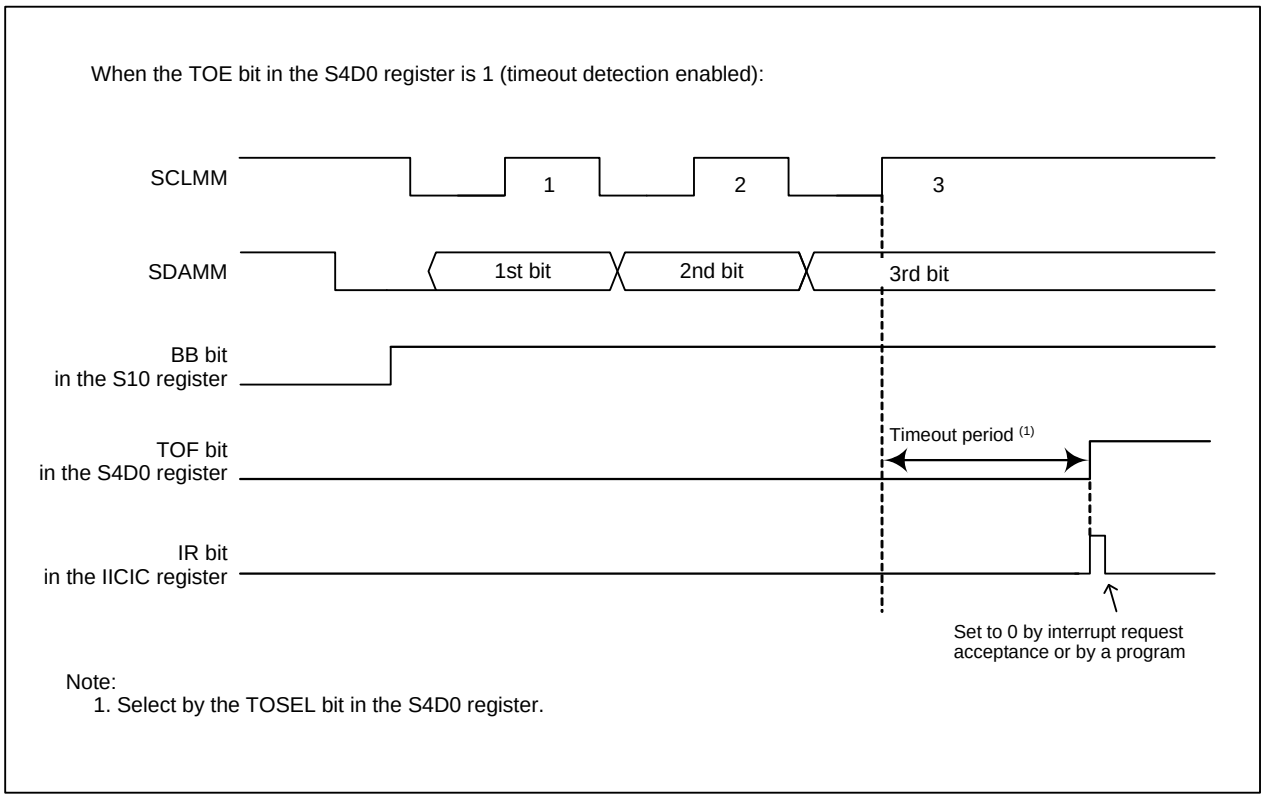


Figure 25.16 Timeout Detect Timing

Timeout is detected when the following conditions are all met:

- The TOE bit in the S4D0 register is set to 1 (timeout detection enabled)
- The BB bit in the S10 register is set to 1 (bus busy)
- Driving the SCLMM pin high for more than timeout detect period

When the timeout is detected,

- the TOF bit in the S4D0 register becomes 1 (timeout detected)
- the IR bit in the IICIC register becomes 1 (I2C-bus interrupt requested)

When the timeout is detected, perform one of the following.

- Set the ES0 bit in the S1D0 register to 0 (disabled).
- Set the IHR bit in the S1D0 register to 1 (I2C interface reset).

25.3.10 Data Transmit/Receive Examples

The data transmit/receive examples are described in this section. The conditions for the examples are follows.

- Slave address: 7 bits
- Data: 8 bits
- ACK clock
- Standard clock mode, bit rate: 100 kbps (fIIC: 20 MHz, fVIIC: 4 MHz)
  20 MHz (fIIC) divided-by-5 = 4 MHz (fVIIC),
  4 MHz (fVIIC) divided-by-8 and further divided-by-5 =100 kbps (bit rate)
- In receive mode, ACK response is sent for other than the last data. NACK is returned after the last data is received.
- When receiving data, I2C-bus interrupt at 8th clock (just before ACK clock): disabled
- Stop condition interrupt: enabled
- Timeout interrupt: disabled
- Set an own slave address to the S0D0 register (registers S0D1 or S0D2 should not be used)

If an I2C-bus interrupt at 8th clock (just before ACK clock) is enabled in data receive, a receiver generates ACK or NACK after each byte of data has been received.

25.3.10.1 Initial Setting

Follow the initial setting procedures below for 25.3.10.2 to 25.3.10.5.

(1) Write an own slave address to bits SAD6 to SAD0 in the S0D0 register.
(2) Write 85h to the S20 register. (CCR value: 5, standard mode selected, ACK clock presents)
(3) Write 18h to the S4D0 register. (fVIIC: fIIC divided-by-5, timeout interrupt disabled)
(4) Write 01h to the S3D0 register. (stop condition detect interrupt enabled and I2C-bus interrupt at 8th clock is disabled when receiving data)
(5) Write 0Fh to the S10 register. (slave-receiver mode)
(6) Write 98h to the S2D0 register (SSC value: 18h, start/stop condition generation timing: long mode)
(7) Write 08h to the S1D0 register (bit counter: 8, I2C interface enabled, addressing format, input level: I2C-bus input)

If the MCU uses a single-master system and it is a master, start the initial setting procedures from (2).

25.3.10.2 Master Transmission

The master transmission is described in this section. The initial settings described in 25.3.10.1 “Initial Setting” are assumed to be completed. Figure 21.17 shows the operation of master transmission. The following programs (A) to (C) are executed at the (A) to (C) in Figure 25.17, respectively.

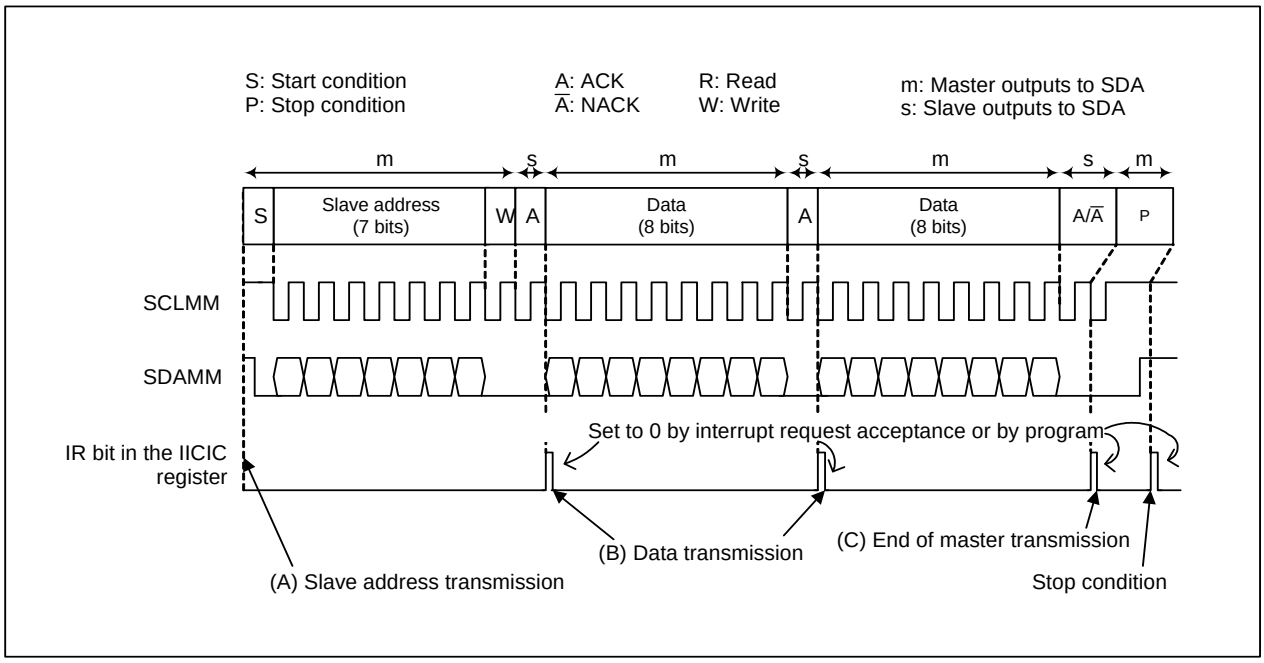


Figure 25.17 Example of Master Transmission

(A) Slave address transmission
(1) The BB bit in the S10 register must be 0 (bus free).
(2) Write E0h to the S10 register. (Start condition standby)
(3) Write a slave address to the seven most significant bits (MSB) and a 0 to the least significant bit (LSB). (Start condition generated, then slave address transmitted)

(B) Data transmission
(in I2C-bus interrupt routine)
(1) Write transmit data to the S00 register. (data transmission)

(C) Completion of Master transmission
(in I2C-bus interrupt routine)
(1) Write C0h to the S10 register. (Stop condition standby state)
(2) Write a dummy data to the S00 register. (stop condition generated)

When the transmission is completed or ACK is not returned from slave device (NACK returned), master transmission should be completed as above.

25.3.10.3 Master Reception

The master reception is described in this section. The initial settings described in 25.3.10.1 “Initial Setting” are assumed to be completed. Figure 25.18 shows the operation example of master reception. The following programs (A) to (D) are executed at the (A) to (D) in Figure 25.18, respectively.

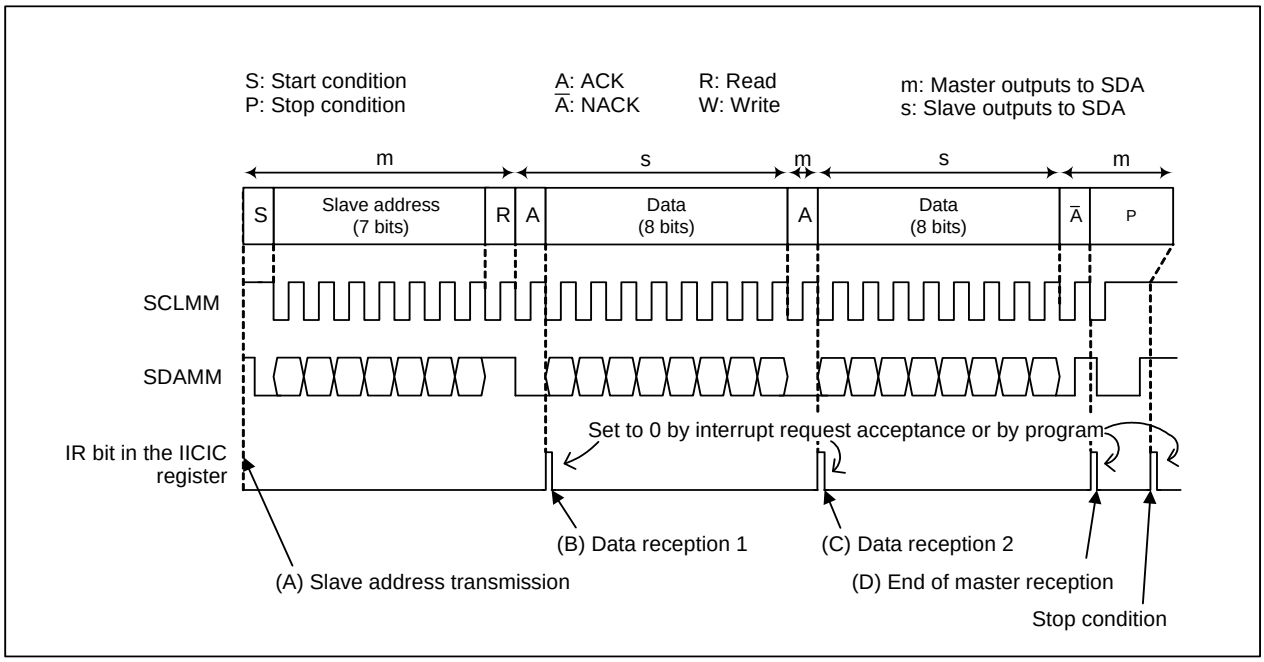


Figure 25.18 Example of Master Reception

(A) Slave address transmission
(1) The BB bit in the S10 register must be 0 (bus free).
(2) Write E0h to the S10 register. (Start condition standby)
(3) Write a slave address to the seven most significant bits (MSB) and a 0 to the least significant bit (LSB). (Start condition generated, then slave address transmitted)

(B) Data reception 1 (after slave address transmission)
(In I2C-bus interrupt routine)
(1) Write AFh to the S10 register. (Master-receiver mode)
(2) Set the ACKBIT bit in the S20 register to 0 (ACK presents) because the data is not the last one.
(3) Write a dummy data to the S00 register

(C) Data reception 2 (data reception)
(In I2C-bus interrupt routine)
(1) Read the received data from the S00 register
(2) Set the ACKBIT bit in the S20 register to 1 (no ACK) because the data is the last one.
(3) Write a dummy data to the S00 register

(D) End of master reception
(In I2C-bus interrupt routine)
(1) Read the received data from the S00 register
(2) Write C0h to the S10 register. (Stop condition standby state)
(3) Write a dummy data to the S00 register (stop condition generated)

25.3.10.4 Slave Reception

The slave reception is described in this section. The initial settings described in 225.3.10.1 “Initial Setting” are assumed to be completed. Figure 25.19 shows the example of slave reception. The following programs (A) to (C) are executed at the (A) to (C) in Figure 25.19, respectively.

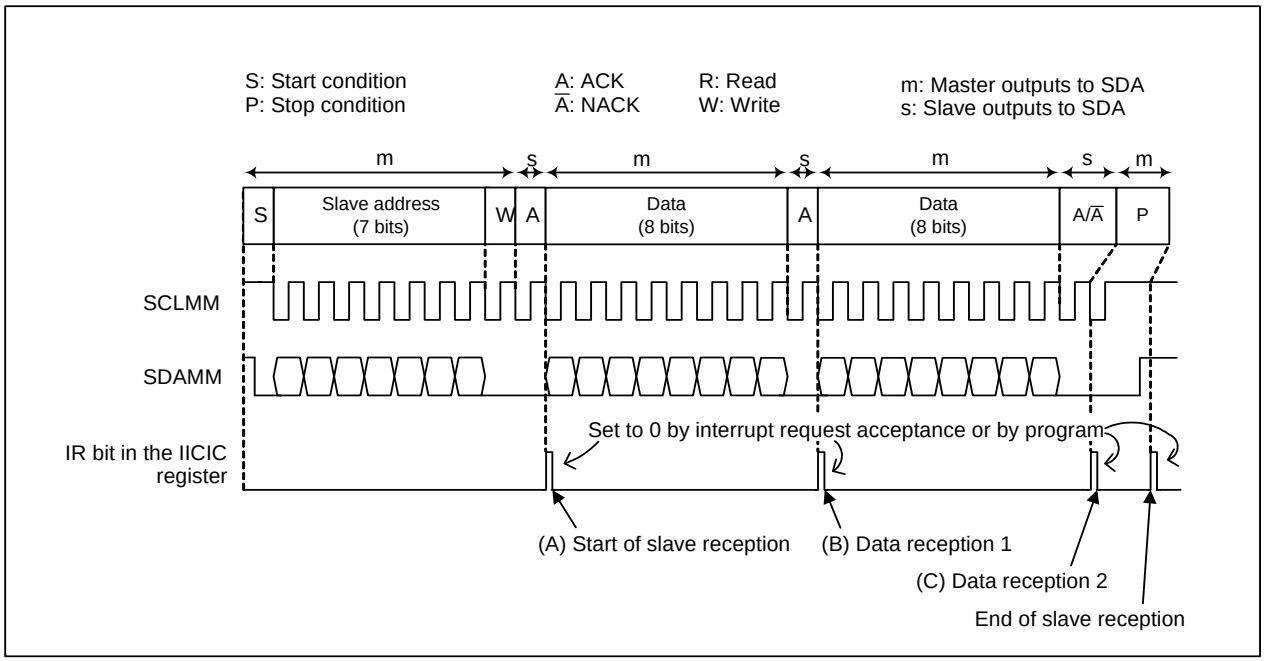


Figure 25.19 Example of Slave Reception

(A) Slave receive is started.
(In I2C-bus interrupt routine)
(1) Check the content of S10 register. When the TRX bit is 0, the I2C interface is in slave-receiver mode.
(2) Write a dummy data to the S00 register.

(B) Data reception 1
(In I2C-bus interrupt routine)
(1) Read the received data from the S00 register.
(2) Set the ACKBIT bit in the S20 register to 0 (ACK presents) because the data is not the last one.
(3) Write a dummy data to the S00 register.

(C) Data reception 2
(In I2C-bus interrupt routine)
(1) Read the received data from the S00 register
(2) Set the ACKBIT bit in the S20 register to 1 (no ACK presents) because the data is the last one.
(3) Write a dummy data to the S00 register.

25.3.10.5 Slave Transmission

The slave transmission is described in this section. The initial settings described in 25.3.10.1 “Initial Setting” are assumed to be completed. Figure 25.20 shows the example of slave transmission. The following programs (A) to (B) are executed at the (A) and (B) in Figure 25.20, respectively.

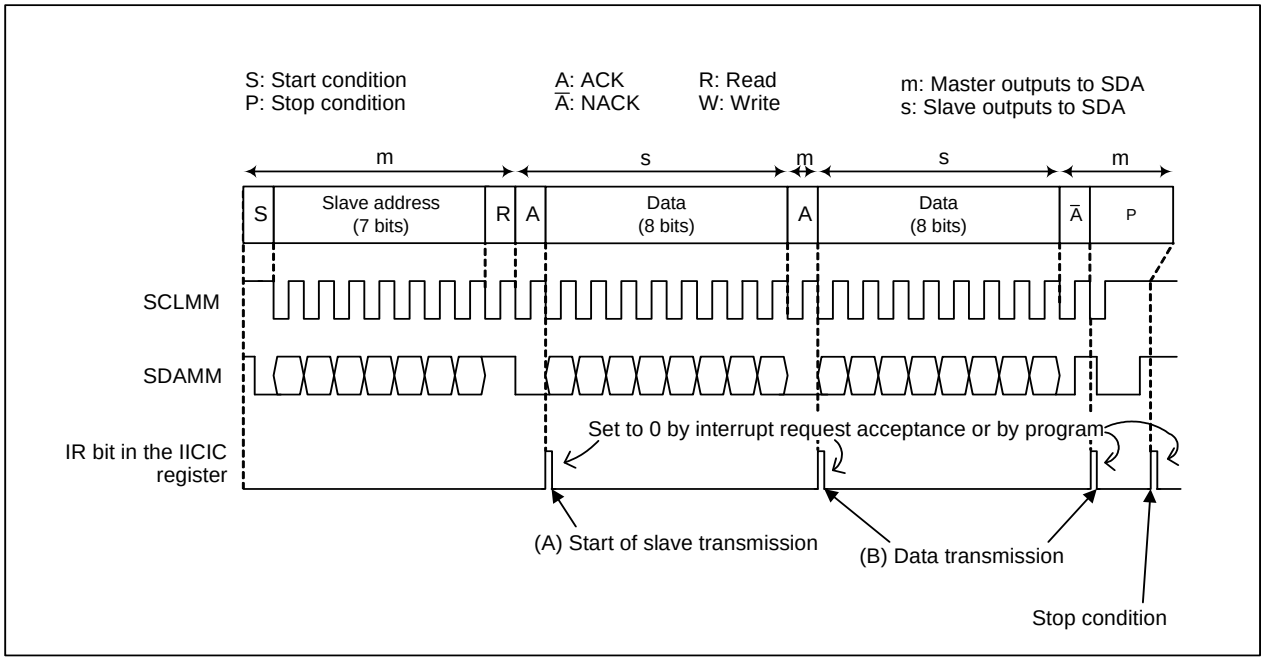


Figure 25.20 Example of Slave Transmission

(A) Start of slave transmission
(In I2C-bus interrupt routine)
(1) Check the content of the S10 register. When the TRX bit is set to 1, the I2C interface is in slave-transmitter mode.
(2) Write a transmit data to the S00 register

(B) Data transmission
(In I2C-bus interrupt routine)
(1) Write a transmit data to the S00 register

Write a dummy data to the S00 register even if an interrupt occurs at an ACK clock of the last transmit data. When the S00 register is written, the SCLMM pin becomes high-impedance.

25.4 Interrupts

I2C interface generates an interrupt request. Figure 25.21 shows I2C Interface Interrupts, and Table 25.16 lists I2C-bus Interrupts.

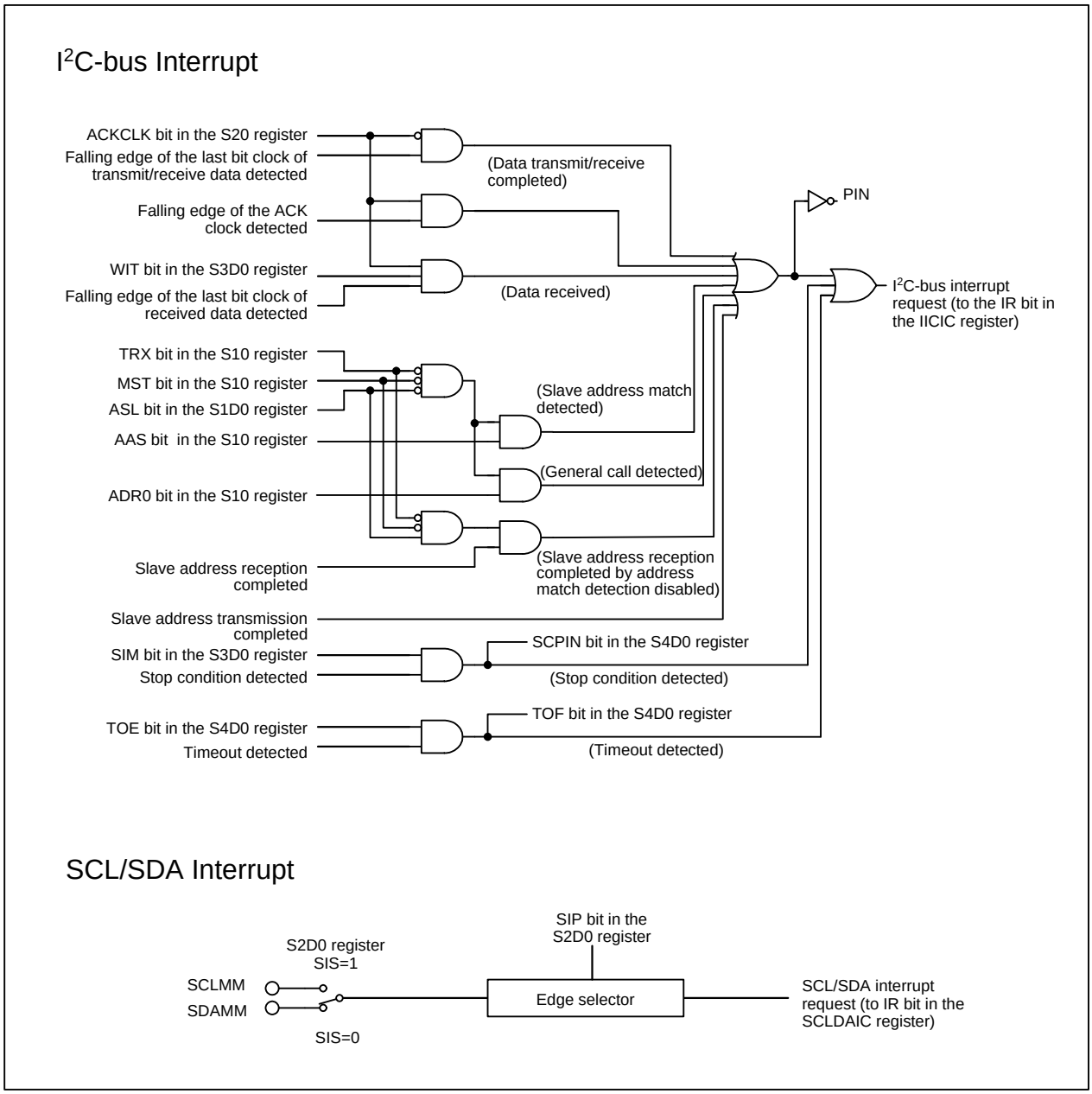


Figure 25.21 I2C Interface Interrupts

Table 25.16 I2C-bus Interrupts

Interrupt	Interrupt Source	Associated Bits (Register)		Interrupt Control Register
		Interrupt enabled	Interrupt request	
I2C-bus Interrupt	Completion of data transmit/receive When the ACKCKL = 0, Detection of the falling edge of the last clock of transmit/receive data through SCLMM pin When the ACKCKL = 1, Detection of the falling edge of ACK clock through SCLMM pin	—	PIN (S10)	IICIC
	Data reception (before ACK clock) Detection of the falling edge of the last clock of transmit/receive data through SCLMM pin	WIT (S3D0)		
	Detection of slave address match Received slave address matches bits SAD6 to SAD0 in slave-receiver mode with addressing format (AAS bit in the S10 register = 1)	—		
	Detection of general call General call in slave-receiver mode with addressing format (ADR0 bit in the S10 register = 1)			
	Completion of receiving slave address in slave-receiver mode with free format			
	Stop condition detected	SIM (S3D0)	SCPIN (S4D0)	
	Timeout detected	TOE (S4D0)	TOF (S4D0)	
SCL/ SDA interrupt	Detection of the falling edge or rising edge of input/output signal for the SCLMM or SDAMM pin	—	—	SCLDAIC

Refer to 14.7 “Interrupt Control”. Table 25.17 lists Registers Associated with I2C Interface Interrupts.

Table 25.17 Registers Associated with I2C Interface Interrupts

Address	Register Name	Register Symbol	Value After Reset
007Bh	IICBus Interface Interrupt Control Register	IICIC	XXXX X000b
007Ch	SCL/SDA Interrupt Control Register	SCLDAIC	XXXX X000b
0206h	Interrupt Source Select Register 2	IFSR2A	00h

When using the I2C-bus interface interrupt, set the IFSR22 bit in the IFSR2A register to 1 (I2C-bus interrupt). When using SCL/SDA interrupt, set the IFSR23 bit in the IFSR2A register to 1 (SCL/SDA interrupt).

The SCL/SDA interrupt is enabled even in wait mode and stop mode.

The IR bit in the SCLDAIC register may become 1 (interrupt requested) when the ES0 bit in the S1D0 register, SIP bit in the S2D0 register, or SIS bit in the S2D0 register is changed. Therefore, follow the procedure below to change these bits. Refer to 14.13 “Notes on Interrupts”.

(1) Set bits ILVL2 to ILVL0 in the SCLDAIC register to 000b (interrupt disabled).
(2) Set the ES0 bit in the S1D0 register and bits SIP and SIS in the S2D0 register.
(3) Set the IR bit in the SCLDAIC register to 0 (no interrupt request).

25.5 Notes on Multi-Master I2C-bus Interface

25.5.1 Limitation on CPU Clock

When the CM07 bit in the CM0 register is 1 (CPU clock is a sub clock), do not access the registers listed in Table 25.4 “Register Configuration”. Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock) to access these registers.

25.5.2 Register Access

Notes are described to access the I2C interface control registers. The period from the rising edge of 1st clock of slave address or one-byte data transmission/reception to the falling edge of an ACK clock is considered as “period of transmission/reception”. When the ACKCLK bit is 0 (no ACK clock), the period of transmission/reception is from the rising edge of 1st clock of slave address or one-byte data transmission/reception to the falling edge of 8th clock.

25.5.2.1 S00 Register

Do not write to the S00 register during transmission/reception.

25.5.2.2 S10 Register

Do not change bits other than the IHR bit in the S10 register during transmission/reception.

25.5.2.3 S20 Register

Do not change bits other than the ACKBIT bit in the S20 register during transmission/reception.

25.5.2.4 S3D0 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S3D0 register.
- Bits ICK1 and ICK0 should be changed when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

25.5.2.5 S4D0 Register

Bits ICK4 to ICK2 should be changed when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

25.5.2.6 S10 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S10 register.
- Do not write to the S10 register when bits MST and TRX change their values.

Figure 25.13 “Start Condition Detection” to Figure 25.15 “Operation After Completion of Slave Address/ Data Transmit/Receive” shows when bits MST and TRX change.

26. Consumer Electronics Control (CEC) Function

26.1 Introduction

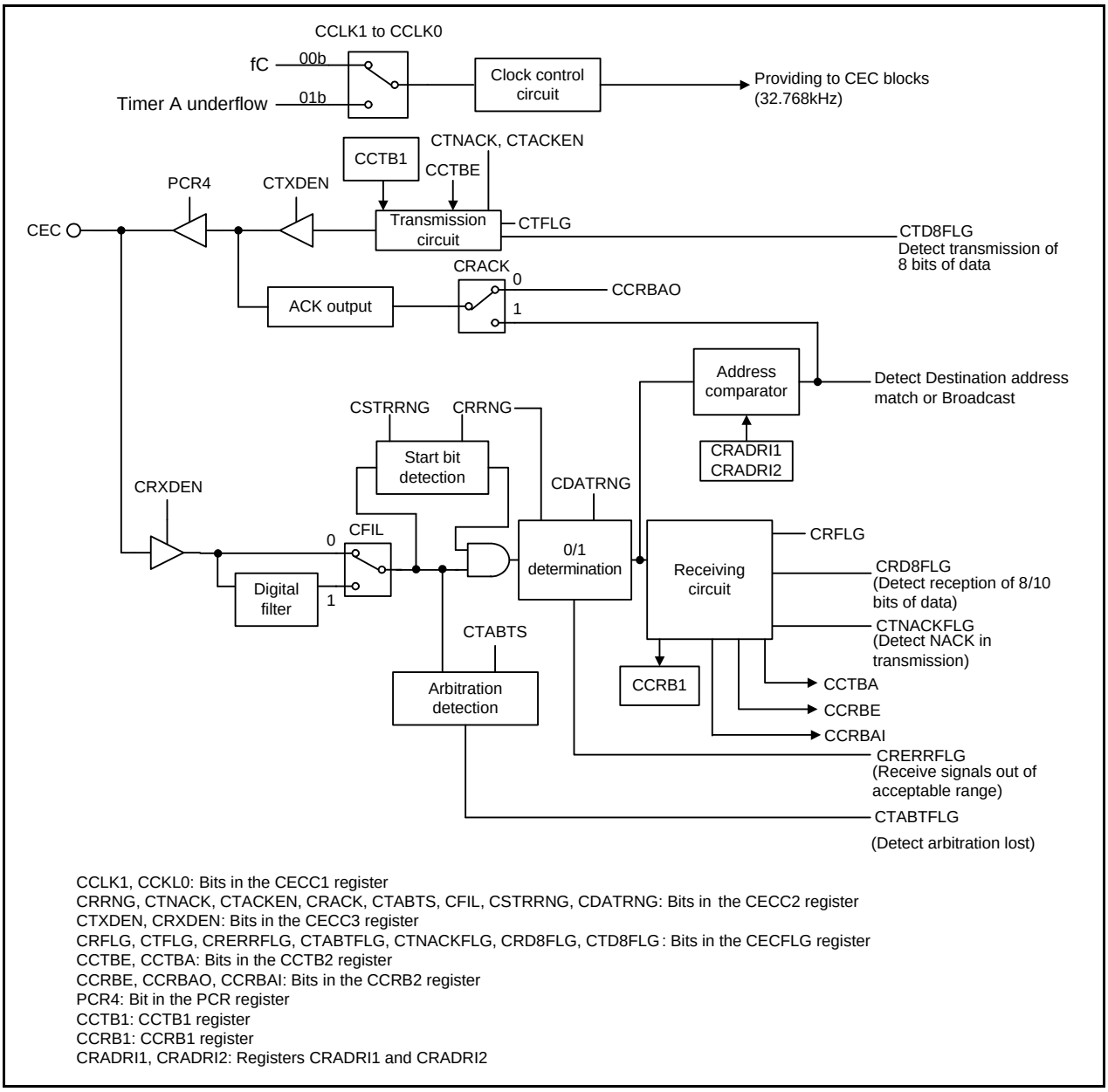
The CEC function indicates circuitry which supports the transmission and reception of CEC signals standardized by the HDMI (High-Definition Multimedia Interface).
Table 26.1 and Table 26.2 list CEC function specifications, Figure 26.1 shows CEC Function Block Diagram and Table 26.3 lists I/O Pin.

Table 26.1 CEC Function Specifications (1/2)

Item	Specification
Count source	fC, timer A0 underflow In either case, the frequency should be 32.768 kHz and oscillation allowable error should be within ± 1%.
Data format	Start bit: 1 bit Data bit: 8 bits EOM bit: 1 bit ACK bit: 1 bit
Transmission start condition	Before transmission starts, satisfy the following requirement. • The CTXDEN bit in the CECC3 register = 1 (transmission enabled)
Reception start condition	Before reception starts, satisfy the following requirements. • The CRXDEN bit in the CECC3 register = 1 (reception enabled) • Start bit detected
Interrupt request generation timing	Transmit interrupt • When 8 bits of data is transmitted completely. • When 10 bits of data is transmitted completely. Transmit error interrupt • When transmit arbitration lost occurs. • When NACK is received in transmission (ACK received in Broadcast transmission). Receive interrupt • When 8 bits of data is received completely. • When 10 bits of data is received completely. • The above receive interrupts can be confined to when matching Destination address or in Broadcast • When the start bit is received completely. Receive error interrupt • A signal out of the acceptable range is received.
Error detection	Arbitration lost If one of the following conditions occurs during transmission, arbitration lost is detected: • When changing the CEC pin from Hi-Z to low output, the pin level is already low. • When changing the CEC pin from low output to Hi-Z, the pin level remains low even after being out of the acceptable range. Transmission error A value of the CCTBA bit in the CCTB2 register matches a value of the CTNACK bit in the CECC2 register. Acceptable range error Low or high period of the data bit is out of the acceptable range.

Table 26.2 CEC Function Specifications (2/2)

Item	Specification
Select functions	Digital filter enabled/disabled Transmission stop selected Transmission stop by receiving ACK or NACK can be selected. Arbitration lost detection conditions One of the following conditions can be selected. • When transmitting the start bit and the data bit of Initiator address • When transmitting the start bit and all data bits Transmit rising timing selected • Selected from 8 levels, standard value -180 μs to standard value +30μs Transmit falling timing selected • Start bit: standard value -160μs to standard value • Data bit: selectable from 4 levels, standard value -310 μs to standard value Receive edge detection selected One of the following conditions can be selected. • Only a falling edge detected • Both falling and rising edges detected ACK output in receiving process One of the following conditions can be selected. • Inserted by program Set by the CCRBAO bit of CCRB2 register. • Inserted by hardware ACK is output when matching Destination address. Otherwise, NACK is output. Start bit acceptable range • Select ± 200μs or ± 300μs Data bit acceptable range One of the following conditions can be selected. • Period between a falling edge and a rising edge ± 200 μs, Period between a falling edge and a falling edge ± 350 μs • Period between a falling edge and a rising edge ± 300 μs, Period between a falling edge and a falling edge ± 500 μs Low pulse output when receive error occurs • Whether error low pulse is output or not can be selected when the receive error occurs. Low pulse output wait control when receive error occurs. One of the following conditions can be selected. • Error low pulse is output in synchronization with the rising edge of the CEC input signal if the CEC input signal is low level when the receive error occurs. • Error low pulse is output immediately after the error occurs regardless of the CEC input signal state.



CCLK1, CCKL0: Bits in the CECC1 register
CRRNG, CTNACK, CTACKEN, CRACK, CTABTS, CFIL, CSTRRNG, CDATRNG: Bits in the CECC2 register
CTXDEN, CRXDEN: Bits in the CECC3 register
CRFLG, CTFLG, CRERRFLG, CTABTFLG, CTNACKFLG, CRD8FLG, CTD8FLG: Bits in the CECFLG register
CCTBE, CCTBA: Bits in the CCTB2 register
CCRBE, CCRBAO, CCRBAI: Bits in the CCRB2 register
PCR4: Bit in the PCR register
CCTB1: CCTB1 register
CCRB1: CCRB1 register
CRADRI1, CRADRI2: Registers CRADRI1 and CRADRI2

Figure 26.1 CEC Function Block Diagram

Table 26.3 I/O Pin

Pin Name	I/O Type	Description
CEC	Input/Output	CEC input and output (N-channel open-drain output)

Note:
1. Set the direction bit of the ports sharing a pin to 0 (input mode).

26.2 Registers

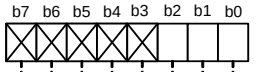
The registers and the bits of the CEC function are synchronized with the count source. The contents of the register is changed immediately after rewriting the value of the register by a program, while the internal circuit starts to operate from the next count source timing.

Table 26.4 Register Structure

Address	Register Name	Register Symbol	After Reset
0350h	CEC Function Control Register 1	CECC1	XXXX X000b
0351h	CEC Function Control Register 2	CECC2	00h
0352h	CEC Function Control Register 3	CECC3	XXXX 0000b
0353h	CEC Function Control Register 4	CECC4	00h
0354h	CEC Flag Register	CECFLG	00h
0355h	CEC Interrupt Source Select Register	CISEL	00h
0356h	CEC Transmit Buffer Register 1	CCTB1	00h
0357h	CEC Transmit Buffer Register 2	CCTB2	XXXX XX00b
0358h	CEC Receive Buffer Register 1	CCRB1	00h
0359h	CEC Receive Buffer Register 2	CCRB2	XXXX X000b
035Ah	CEC Receive Follower Address Set Register 1	CRADRI1	00h
035Bh	CEC Receive Follower Address Set Register 2	CRADRI2	00h
0366h	Port Control Register	PCR	0000 0XX0b

26.2.1 CEC Function Control Register 1 (CECC1)

CEC Function Control Register 1



Symbol	Address	After Reset
CECC1	0350h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
CECEN	CEC enable bit	0: Disabled 1: Enabled	RW
CCLK0	Clock source select bit	b2 b1 0 0 : fC 0 1 : Timer A0 underflow 1 0 : Do not set 1 1 : Do not set	RW
CCLK1			
— (b7-b3)	Reserved bits	Set to 0. Read as undefined value.	RW

CECEN (CEC Enable Bit) (b0)

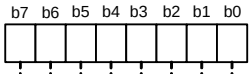
Set the CECEN bit to 1 (CEC enabled) when the count source is selected by using bits CCLK1 to CCLK0 and the count source is stable.
When the CECEN bit is set to 0 (CEC disabled), the circuit of the CEC function is reset.

CCLK1-CCLK0 (Clock Source Select Bit) (b2-b1)

Change the clock source when the CECEN bit is set 0 (CEC disabled).

26.2.2 CEC Function Control Register 2 (CECC2)

CEC Function Control Register 2



Symbol	Address	After Reset
CECC2	0351h	00h

Bit Symbol	Bit Name	Function	RW
CRRNG	Receive edge detection select bit	0: Detects falling edge acceptable range 1: Detects both edges acceptable range	RW
CTNACK	Transmit NACK (ACK) end select bit	0: End with ACK 1: End with NACK	RW
CTACKEN	Transmit NACK (ACK) end control bit	0: Continue to transmit 1: End with NACK/ACK	RW
CRACK	ACK output control bit	0: Inserted by program 1: Inserted by hardware	RW
CTABTS	Arbitration lost detect condition select bit	0: When transmitting start bit and Initiator address 1: When transmitting start bit and all data bits	RW
CFIL	Digital filter enable bit	0: Filter disabled 1: Filter enabled	RW
CSTRRNG	Start bit acceptable range select bit	0: ±200 µs 1: ±300 µs	RW
CDATRNG	Data bit acceptable range select bit	0: Period between falling edge and rising edge ± 200 µs Period between falling edge and falling edge ± 350 µs 1: Period between falling edge and rising edge ± 300 µs Period between falling edge and falling edge ± 500 µs	RW

CTNACK (Transmit NACK (ACK) End Select Bit) (b1)

This bit is enabled when the CTACKEN bit is set to 1 (end with ANCK/ACK).

CTACKEN (Transmit NACK (ACK) End Control Bit) (b2)

Select the end condition by using the CTNACK bit when the CTACKEN bit is set to 1 (end with NACK/ACK).

CRACK (ACK Output Control Bit) (b3)

When the CRACK bit is set 0 (inserted by program), the value of the CCRBAO bit in the CCRB2 register is output as ACK data.

When the CRACK bit is set to 1 (inserted by hardware), ACK is output if the received Destination address matches the address selected by the CRADRI1 or CRADRI2 register. Table 26.5 lists ACK Output When Inserted by Hardware.

Table 26.5 ACK Output When Inserted by Hardware

Destination Address		ACK Output
Received Destination Address	Address Selected by the CRADRI1 or CRADRI2 Register (Own Address)	
Directly address (0000b to 1110b)	Matches the received Destination address	ACK
	Not match the received Destination address	NACK
Broadcast (1111b)	1111b (matches the received Destination address)	ACK
	0000b to 1110b	NACK

CTABTS (Arbitration Lost Detect Condition Select Bit) (b4)

When the CEC output is low, the range of detecting arbitration lost if the level becomes Hi-z (rising edge) by the external source can be selected.

When the CEC output is Hi-z, arbitration lost is detected regardless of the rage selected by the CTABTS bit, if the level becomes low (falling edge) by the external source.

26.2.3 CEC Function Control Register 3 (CECC3)

CEC Function Control Register 3

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X				

Symbol	Address	After Reset
CECC3	0352h	XXXX 0000b

Bit Symbol	Bit Name	Function	RW
CTXDEN	Transmit enable bit	0: Disabled 1: Enabled	RW
CRXDEN	Receive enable bit	0: Disabled 1: Enabled	RW
CREGCLR	Receive edge detect flag clear bit	The CREGFLG bit in the CECC4 register becomes 0 by setting 1 to this bit	RW
CEOMI	EOM disable bit	0: EOM enabled 1: EOM disabled (EOM ignored)	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value		—

CTXDEN (Transmit Enable Bit) (b0)
CRXDEN (Receive Enable Bit) (b1)

When changing the value of these bits, transmission/reception is enabled or disabled after one or more cycles of the clock source elapses.

CREGCLR (Receive Edge Detect Flag Clear Bit) (b2)

The CREGFLG bit in the CECC4 register is set to 0 by setting the CREGCLR bit to 1 when the CEC input is Hi-Z. When the CEC input is low, the CREGFLG bit remain unchanged even if the CREGCLR bit is set to 1.
The CREGCLR bit holds the written value.
To set the CREGCLR bit to 1 in order to set the CREGFLG bit to 0 again, write 0 and then 1.
Figure 26.2 shows Operation of Bits CREGFLG and CREGCLR.

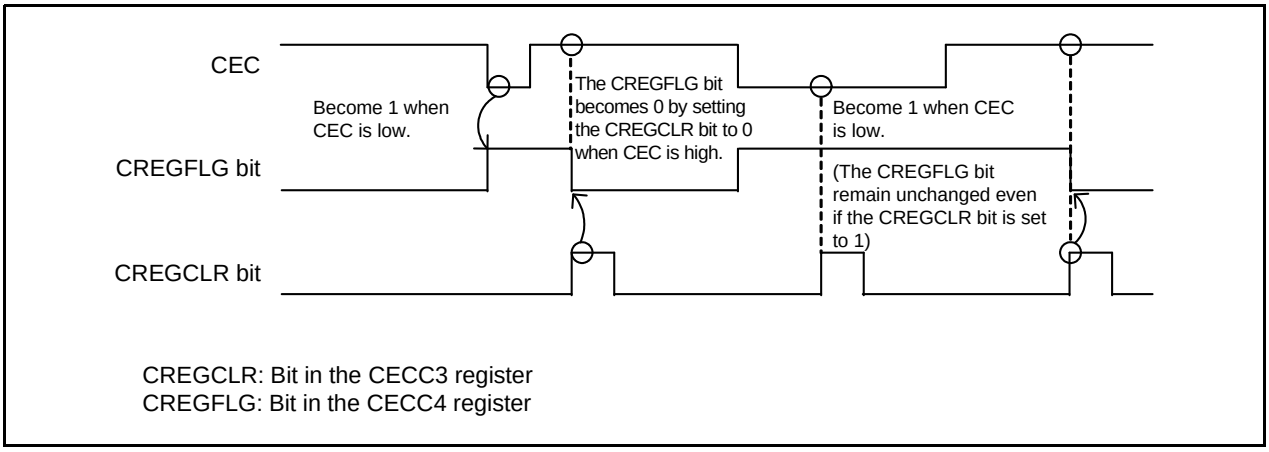


Figure 26.2 Operation of Bits CREGFLG and CREGCLR

CEOMI (EOM Disable Bit) (b3)

Whether the operation continues or stops can be selected when the EOM is 1. Table 26.6 lists Operation When the EOM is 1.

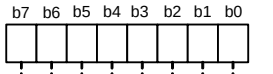
When the CEOMI bit is set to 1 (EOM disabled), data transmission continues even though the EOM is 1. To stop transmitting, set the CTXDEN bit in the CECC3 register to 0 (transmission disabled).

Table 26.6 Operation When the EOM is 1

CEOMI Bit	Operation When EOM is 1	
	Reception	Transmission
0	Subsequent data reception is ignored once the data that the EOM is 1 (wait for start bit) is received.	Subsequent data is not transmitted once the data that the EOM is 1 is transmitted.
1	ACK/NACK is returned even if the data that the EOM is 1 is received.	Data is transmitted even if the data that the EOM is 1 is transmitted.

26.2.4 CEC Function Control Register 4 (CECC4)

CEC Function Control Register 4



Symbol	Address	After Reset
CECC4	0353h	00h

Bit Symbol	Bit Name	Function	RW
CRISE0	Rising timing select bit	b2 b1 b0 0 0 0: Standard value 0 0 1: Standard value - 30 µs 0 1 0: Standard value - 60 µs 0 1 1: Standard value - 90 µs 1 0 0: Standard value - 120 µs 1 0 1: Standard value - 150 µs 1 1 0: Standard value - 180 µs 1 1 1: Standard value + 30 µs	RW
CRISE1			RW
CRISE2			RW
CABTEN	Error low pulse output enabled bit	0: Disabled 1: Enabled	RW
CFALL0	Falling timing select bit	Refer to the following.	RW
CFALL1			RW
CREGFLG	Receive edge detect flag	0: Not detected 1: Detected	RO
CABTWEN	Error low pulse output wait control bit	0: Low pulse output regardless of CEC signal state 1: Low pulse output at the rising edge of the CEC signal	RW

CRISE2-CRISE0 (Rising Timing Select Bit) (b2-b0)

The rising timing of the signal in transmission is selected. The rising timing is common to the start bit and data bit.

CABTEN (Error Low Pulse Output Enable Bit) (b3)

When the CABTEN bit is set to 1 (low pulse output enabled in receive error), 3.6 ms of low pulse is output if the data bit in reception is out of the acceptable range.
Output timing is selected by the CABTWEN bit.

CFALL1-CFALL0 (Falling Timing Select Bit) (b5-b4)

The falling timing of the signal in transmission is specified.

Table 26.7 Falling Timing of Signal in Transmission

Bits CFALL1 to CFALL0	Falling Timing	
	Start Bit	Data Bit
00b	Standard value	Standard value
01b	Standard value - 40 µs	Standard value - 190 µs
10b	Standard value - 100 µs	Standard value - 250 µs
11b	Standard value - 160 µs	Standard value - 310 µs

CREGFLG (Receive Edge Detect Flag) (b6)

Refer to Figure 26.2 “Operation of Bits CREGFLG and CREGCLR”.
Condition to become 0.

- Set the CREGCLR bit in the CECC3 register to 1 when the CEC input is Hi-Z.

Condition to become 1.

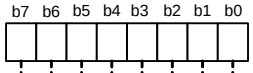
- The CEC input is low level.

CABTWEN (Error Low Pulse Output Wait Control Bit) (b7)

This bit is enabled when the CABTEN bit is set to 1 (low pulse output enabled in reception error).
If the receive error occurs when the CABTWEN bit is set to 1 (low pulse output at rising edge of the CEC signal) and the CEC input is low, 3.6 ms of low pulse is output from the rising edge of the CEC signal after the error. If there is no rising edge of the CEC signal within 3.6 ms from the reception error, low pulse is not output because it is assumed that another device outputs error low pulse.

26.2.5 CEC Flag Register (CECFLG)

CEC Flag Register



Symbol	Address	After Reset
CECFLG	0354h	00h

Bit Symbol	Bit Name	Function	RW
CRFLG	Receive status flag	0: Waiting 1: Receiving	RO
CTFLG	Transmit status flag	0: Waiting 1: Receiving	RO
CRERRFLG	Receive error detect flag	0: Not detected 1: Error detected (out of the determinable range)	RO
CTABTFLG	Arbitration lost detect flag	0: Not detected 1: Detected	RO
CTNACKFLG	Transmit NACK detect flag	0: Not detected 1: NACK detected (when transmitting Directly addressed) ACK detected (in Broadcast)	RO
CRD8FLG	8th bit of data receive flag	0: 8th bit not received or 10th bit received 1: 8th bit received	RO
CTD8FLG	8th bit of data transmit flag	0: 8th bit not transmitted or 10th bit transmitted 1: The 8th bit transmitted	RO
CRSTFLG	Start bit detection	0: Start bit not detected or 8th bit received. 1: Start bit detected	RO

CRFLG (Receive Status Flag) (b0)

Condition to become 0.

- Waiting

Condition to become 1.

- Receiving
- Error low pulse is being output when the CABTEN bit in the CECC4 register is set to 1 (error low pulse output enabled).

CRERRFLG (Receive Error Detect Flag) (b2)

Condition to become 0.

- Set the CRXDEN bit in the CECC3 to 0 (receive disabled).

Condition to become 1.

- Low or high period of the data bit is out of the acceptable range

CTABTFLG (Arbitration Lost Detect Flag) (b3)

Condition to become 0.

- Set the CTXDEN bit in the CECC3 register to 0 (transmit disabled).

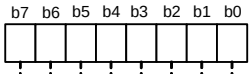
CTNACKFLG (Transmit NACK Detect Flag) (b4)

Condition to become 0.

- Set the CTXDEN bit in the CECC3 register to 0 (transmit disabled).

26.2.6 CEC Interrupt Source Select Register (CISEL)

CEC Interrupt Source Select Register



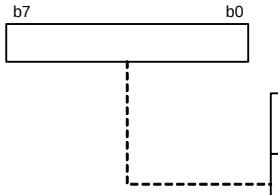
Symbol	Address	After Reset
CISEL	0355h	00h

Bit Symbol	Bit Name	Function	RW
CRISEL0	8th bit receive interrupt enable bit	0: Disabled 1: Enabled	RW
CRISEL1	10th bit receive interrupt enable bit	0: Disabled 1: Enabled	RW
CRISEL2	Receive error interrupt enable bit	0: Disabled 1: Enabled	RW
CRISELM	Receive interrupt mode select bit	0: No limitation of 8th/10th bit receive interrupt 1: 8th/10th bit receive interrupt occurs only when matching Destination address or in Broadcast	RW
CTISEL0	8th bit transmit interrupt enable bit	0: Disabled 1: Enabled	RW
CTISEL1	10th bit transmit interrupt enable bit	0: Disabled 1: Enabled	RW
CTISEL2	Transmit NACK receive interrupt enable bit	0: Disabled 1: Enabled	RW
CRISELS	Reception start bit interrupt enable bit	0: Disabled 1: Enabled	RW

Set the CECEN bit in the CECC1 register to 0 (CEC disabled) to change the CISEL register.

26.2.7 CEC Transmit Buffer Register 1 (CCTB1)

CEC Transmit Buffer Register 1



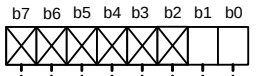
Symbol	Address	After Reset
CCTB1	0356h	00h

Function	RW
Sets the transmit data	RW

Rewrite the CCTB1 register when the CTXDEN bit in the CECC3 register is set to 0 (transmit disabled), or the CTXDEN bit is set to 1 and the CTD8FLG in the CECFLG register is set to 1 (while bits EOM and ACK are being transmitted after the 8th bit has been transmitted). Do not rewrite the CCTB1 register when the CTXDEN bit is set to 1 and the CTD8FLG bit is set to 0 (while the 1st bit to 8th bit are being transmitted).

26.2.8 CEC Transmit Buffer Register 2 (CCTB2)

CEC Transmit Buffer Register 2



Symbol	Address	After Reset
CCTB2	0357h	XXXX XX00b

Bit Symbol	Bit Name	Function	RW
CCTBE	Transmit data EOM bit	0: Data block continues 1: Data block ends	RW
CCTBA	Transmit data ACK input bit	0: ACK input 1: NACK input	RW
— (b7-b2)	No register bits. If necessary, set to 0. Read as undefined value		—

CCTBE (Transmit Data EOM Bit) (b0)

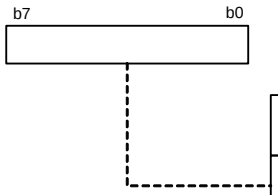
Rewrite the CCTBE bit when the CTXDEN bit in the CECC3 register is set to 0 (transmit disabled), or the CTXDEN bit is set to 1 and the CTD8FLG in the CECFLG register is set to 1 (while bits EOM and ACK are being transmitted after the 8th bit has been transmitted). Do not rewrite the CCTBE bit when the CTXDEN bit is set to 1 and the CTD8FLG bit is set to 0 (while the 1st bit to 8th bit are being transmitted).

CCTBA (Transmit Data ACK Input Bit) (bs1)

Read the CCTBA bit after transmitting the 10th bit (ACK bit) (the CTD8FLG bit in the CECFLG register changes from 1 to 0).

26.2.9 CEC Receive Buffer Register 1 (CCRB1)

CEC Receive Buffer Register 1



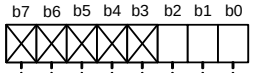
Symbol	Address	After Reset
CCRB1	0358h	00h

Function	RW
Reads the receive data.	RW

Read the CCRB1 register after receiving the 8th bit (the CRD8FLG bit in the CECFLG register changes from 0 to 1).

26.2.10 CEC Receive Buffer Register 2 (CCRB2)

CEC Receive Buffer Register 2



Symbol	Address	After Reset
CCRB2	0359h	XXXX X000b

Bit Symbol	Bit Name	Function	RW
CCRBE	Receive data EOM bit	0: Data block continues 1: Data block ends	RO
CCRBAO	Receive data ACK output bit	0: ACK output 1: NACK output	RW
CCRBAI	Receive data ACK input bit	0: ACK input 1: NACK input	RO
— (b7-b3)	No register bits. If necessary, set to 0. Read as undefined value		—

CCRBE (Receive Data EOM bit) (b0)

Read the CCRBE bit after receiving the 10th bit (ACK bit) (the CRD8FLG bit in the CECFL register changes from 1 to 0).

CCRBAO (Receive Data ACK Output Bit) (b1)

The CCRBAO bit is valid when the CRACK bit in the CECC2 register is set to 0 (inserted by program).

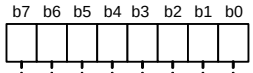
Rewrite the CCRBAO bit when the CRXDEN bit in the CECC3 register is set to 0 (receive disabled), or the CRXDEN bit is set to 1 and the start bit to EOM bit are being received. Do not rewrite the CCRBAO bit when the ACK bit is being transmitted.

CCRBAI (Receive Data ACK Input Bit) (b2)

Read the CCRBAI bit after the 10th bit (ACK bit) is received (the CRD8FLG bit in the CECFL register changes from 1 to 0).

26.2.11 CEC Receive Follower Address Set Register 1 (CRADRI1), CEC Receive Follower Address Set Register 2 (CRADRI2)

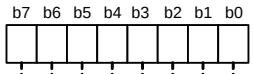
CEC Receive Follower Address Set Register 1



Symbol	Address	After Reset
CRADRI1	035Ah	00h

Bit Symbol	Bit Name	Function	RW
CRADRI10	0000b select bit	0: Not selected 1: Selected	RW
CRADRI11	0001b select bit		RW
CRADRI12	0010b select bit		RW
CRADRI13	0011b select bit		RW
CRADRI14	0100b select bit		RW
CRADRI15	0101b select bit		RW
CRADRI16	0110b select bit		RW
CRADRI17	0111b select bit		RW

CEC Receive Follower Address Set Register 2



Symbol	Address	After Reset
CRADRI2	035Bh	00h

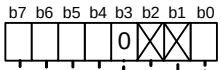
Bit Symbol	Bit Name	Function	RW
CRADRI20	1000b select bit	0: Not selected 1: Selected	RW
CRADRI21	1001b select bit		RW
CRADRI22	1010b select bit		RW
CRADRI23	1011b select bit		RW
CRADRI24	1100b select bit		RW
CRADRI25	1101b select bit		RW
CRADRI26	1110b select bit		RW
CRADRI27	1111b select bit		RW

Select the receive follower address (own address).
Set the CECEN bit in the CECC1 register to 0 (CEC disabled) to change registers CRADRI1 and CRADRI2.

ACK is returned by setting the CRADRI27 bit to 1 (selects 1111b) when the Follower address is 1111b (Broadcast) and the CRACK bit in the CECC2 register is 1 (ACK output in reception is inserted by hardware).
When the received Destination address matches the address selected by the CRADRI1 or CRADRI2 register, it may be described as Destination address match in this chapter.

26.2.12 Port Control Register (PCR)

Port Control Register



Symbol: PCR | Address: 0366h | After Reset: 0000 0XX0b

Bit Symbol	Bit Name	Function	RW
PCR0	Port P1 control bit	When reading the P1 register: 0 : Input level of pins P1_0 to P1_7 is read when the port is set to input. Port latch is read when the port is set to output. 1 : Port latch is read whether the port is set to input or output.	RW
(b2-b1)	No register bits. If necessary, set to 0. Read as undefined value		RW
PCR3	Reserved bit	Set to 0	RW
PCR4	CEC output enable bit	0 : CEC output disabled 1 : CEC output enabled	RW
PCR5	$\overline{\text{INT6}}$ input enable bit	0 : Enabled 1 : Disabled	RW
PCR6	$\overline{\text{INT7}}$ input enable bit	0 : Enabled 1 : Disabled	RW
PCR7	Key input enable bit	0 : Enabled 1 : Disabled	RW

PCR4 (CEC Output Enable Bit) (b4)

To use the CEC function, set the PCR4 bit to 1 (CEC output enabled).

26.3 Operations

26.3.1 Standard Value and I/O Timing

The CEC transmission/reception is based on the count source cycle.
When outputting, an output waveform is based on the count source cycle which is closest to the CEC standard value. When inputting, an input waveform is sampled in the count source cycle
Also, the input/output is practically performed based on the count source cycle closest to the acceptable range or output timing.

26.3.2 Count Source

Select fC or timer A0 underflow by bits CCLK1 to CCLK0 in the CECC1 register. In either case, the clock frequency should be 32.768kHz and oscillation allowable error should be within ± 1%. Set the CECEN bit in the CECC1 register to 1 (CEC enabled), after the count source is selected by bits CCLK1 and CCLK0 and when the count source is stable.

To use fC, set the PM25 bit in the PM2 register to 1 (peripheral clock fC provided). Refer to 8. “Clock Generator” for details.

When the timer A0 underflow is used as the count source, each time timer A0 underflows the internal signal of the timer A0 is reversed. Since this internal signal is the count source, two cycles of timer A0 underflows are one cycle of the count source. Figure 26.3 shows Count Source When Timer A0 Underflow Selected. Use the timer A0 without timer mode and gate function. Refer to 17. “Timer A” for details.

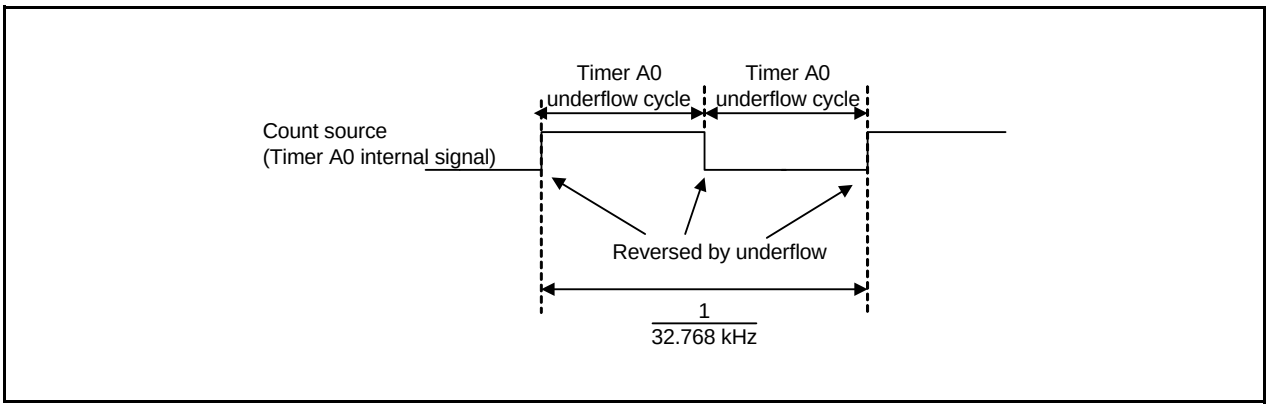


Figure 26.3 Count Source When Timer A0 Underflow Selected

26.3.3 CEC Input/Output

The CEC input and output share pins with the I/O port and $\overline{\text{NMI}}$ input. To use CEC input and output, set bits as follows:

- set the PM24 bit in the PM2 register to 0 ($\overline{\text{NMI}}$ interrupt disabled)
- set bits NMIDF2 to NMIDF0 in the NMIDF register to 000b ($\overline{\text{NMI}}$/$\overline{\text{SD}}$ filter disabled)
- set the PCR4 bit in the PCR register to 1 (CEC output enabled)
- set the PD8_5 bit in the PD8 register to 0 (input mode)

Also, the CEC input has a digital filter besides the $\overline{\text{NMI}}$/$\overline{\text{SD}}$ filter (refer to 26.3.4 “Digital Filter”).

26.3.4 Digital Filter

The input to the CEC pin goes into the internal circuit in synchronization with the count source. If the same level signal is input to the CEC pin twice in a row that level is transferred to the internal circuit, when the CFIL bit in the CECC2 register is set to 1 (digital filter enable). Figure 26.4 shows Digital Filter.

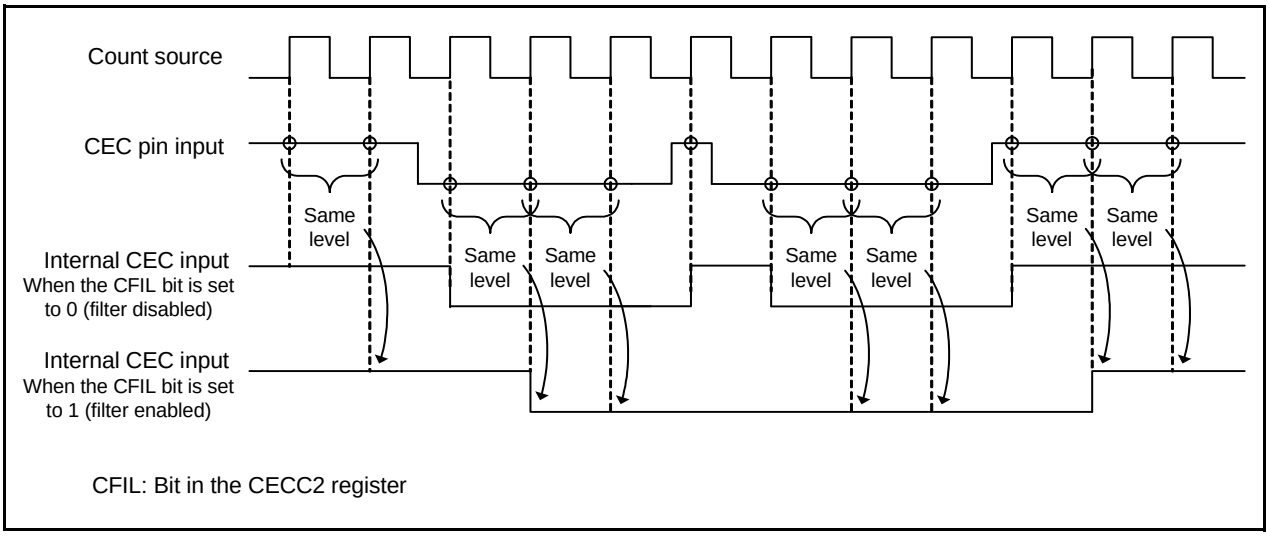


Figure 26.4 Digital Filter

26.3.5 Reception

26.3.5.1 Start Bit Detection

The detect timing of the start bit and data bit is selected by the CRRNG bit in the CEC2 register. Select the start bit acceptable range by the CSTRRNG bit in the CECC2 register. Figure 26.5 shows Start Bit Acceptable Range.

When the start bit within the acceptable range is detected, the CRSTFLG bit in the CECFLG register becomes 1 (start bit detected).

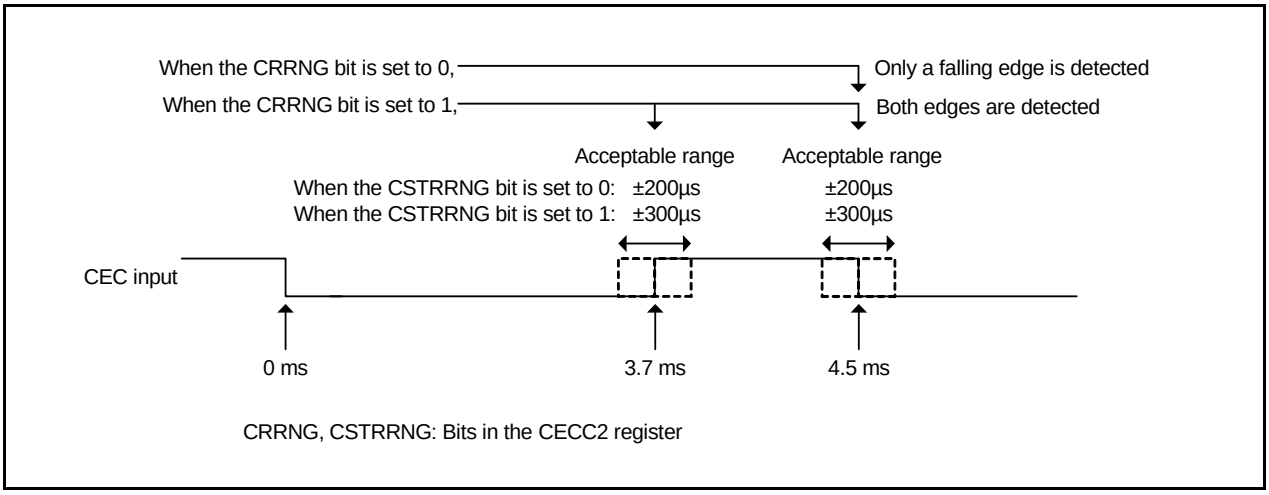


Figure 26.5 Start Bit Acceptable Range

26.3.5.2 Data Bit Detection

The detect timing of the start bit and data bit (other than start bit) is selected by the CRRNG bit in the CECC2 register. Select the data bit acceptable range by the CDATRNG bit in the CECC2 register. Figure 26.6 shows Data Bit Acceptable Range (CRRNG Bit = 0).

When the CRRNG bit is set to 0 (detects falling edge acceptable range), the input data is determined as data 1 if the rising edge is detected before 1.05ms and the input data is determined as data 0 if the rising edge is detected after 1.05 ms.

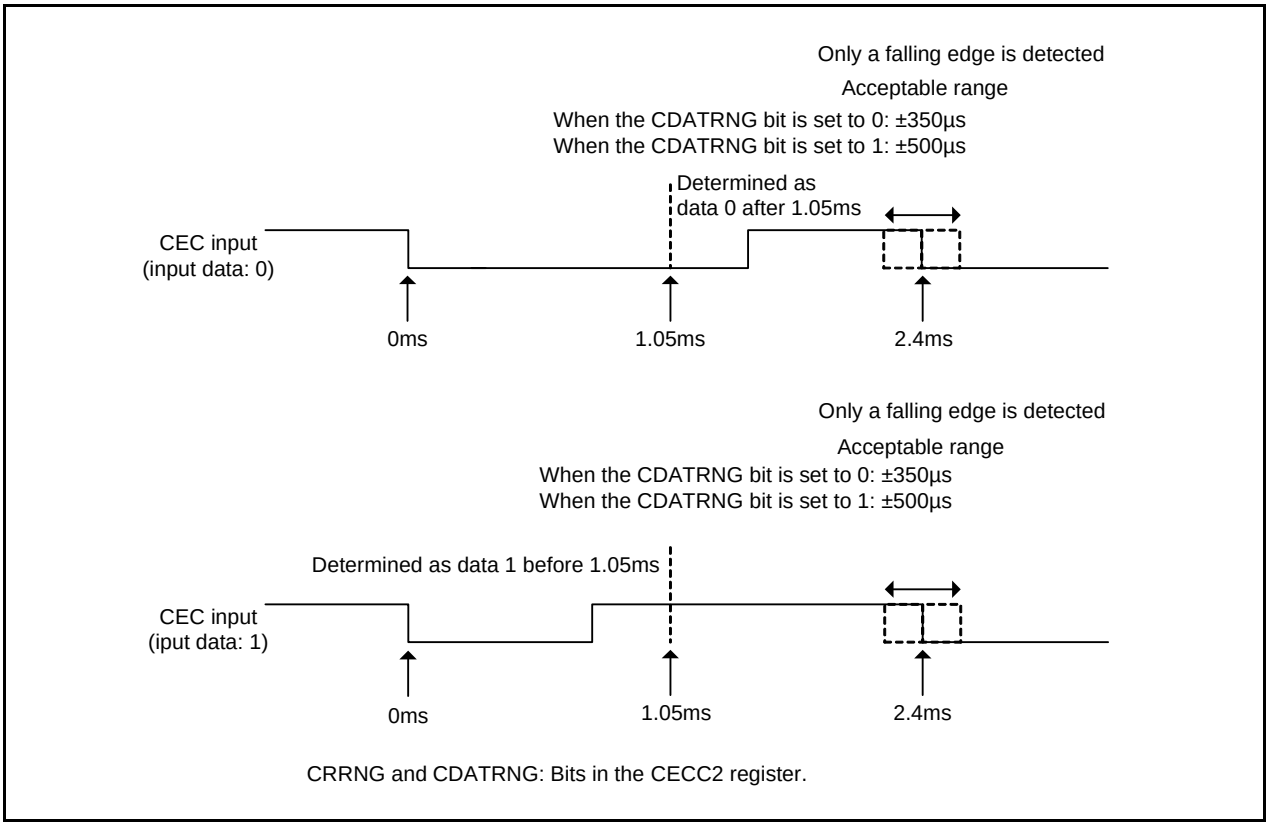


Figure 26.6 Data Bit Acceptable Range (CRRNG Bit = 0)

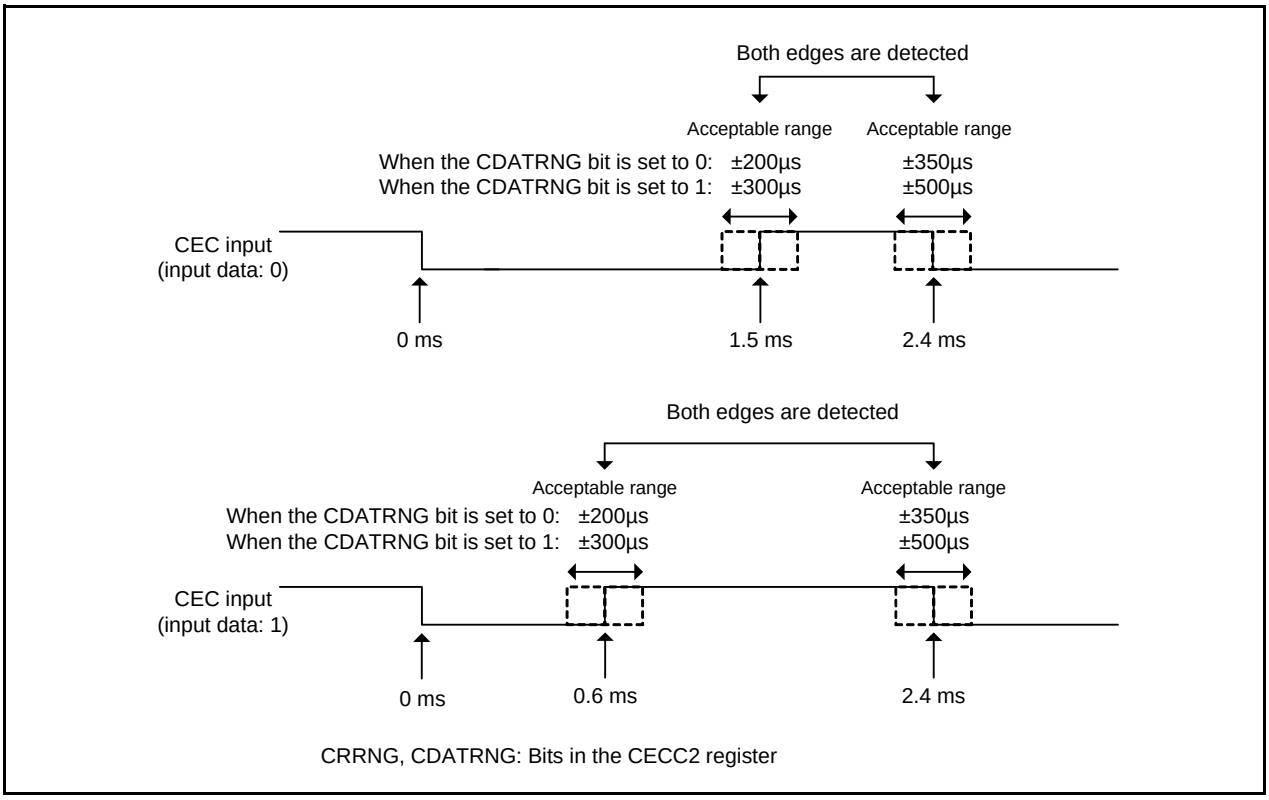


Figure 26.7 Data Bit Acceptable Range (CRRNG Bit = 1)

If the data bit is out of the acceptable range, the receive error occurs. The operations when the receive error occurs are as follows:

- The CRERRFLG bit in the CECFLG register is set to 1 (receive error)
- 3.6 ms of low pulse is output when the CABTEN bit in the CECC4 register is set to 1 (low pulse output enabled in receive error).

Low pulse output timing can be selected by the CABTWEN bit in the CECC4 register when the CABTEN bit is set to 1 (low pulse output enabled in receive error). Figure 26.8 shows Low Pulse Output in Receive Error.

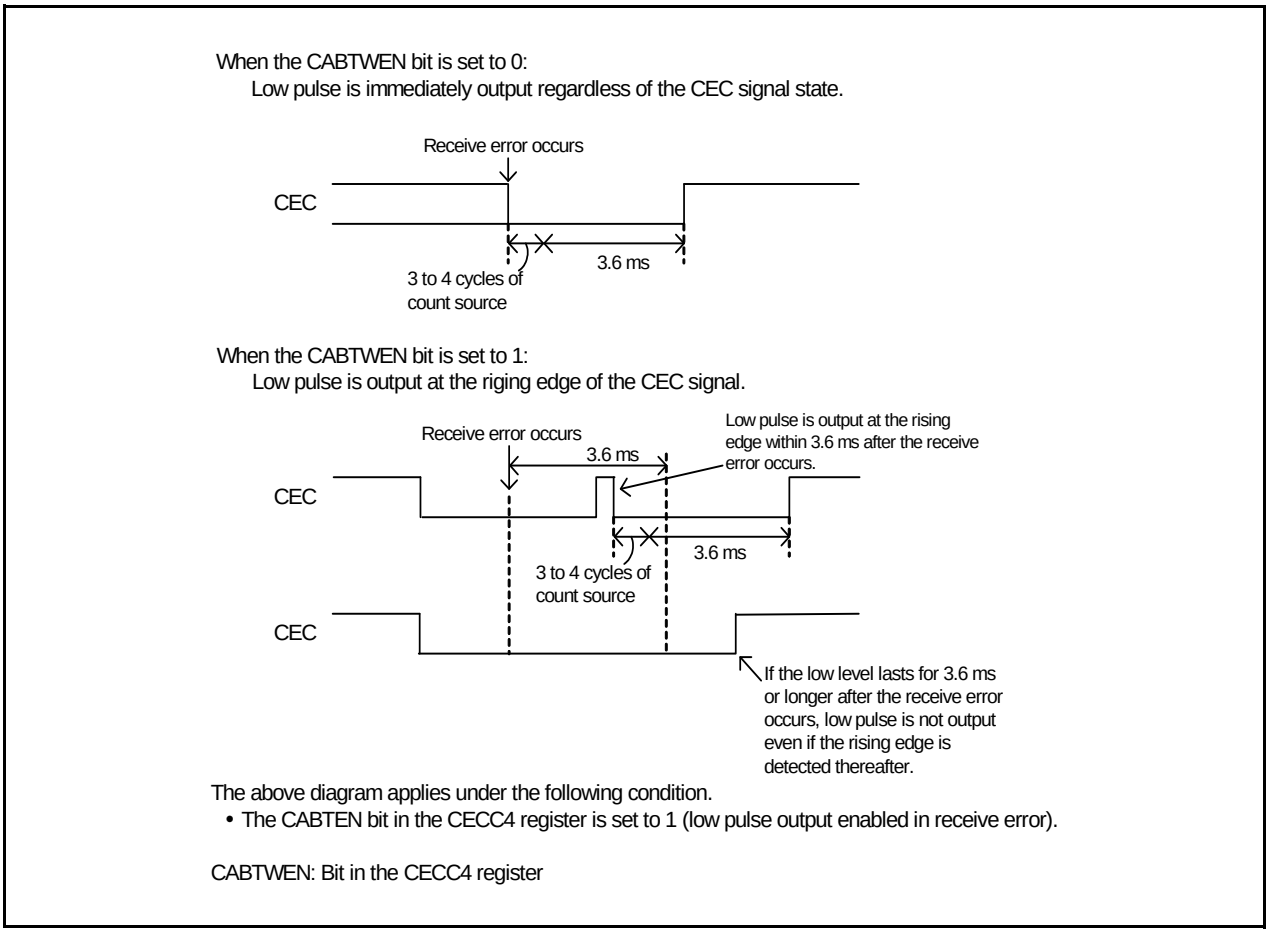


Figure 26.8 Low Pulse Output in Receive Error

26.3.5.3 ACK Bit Output

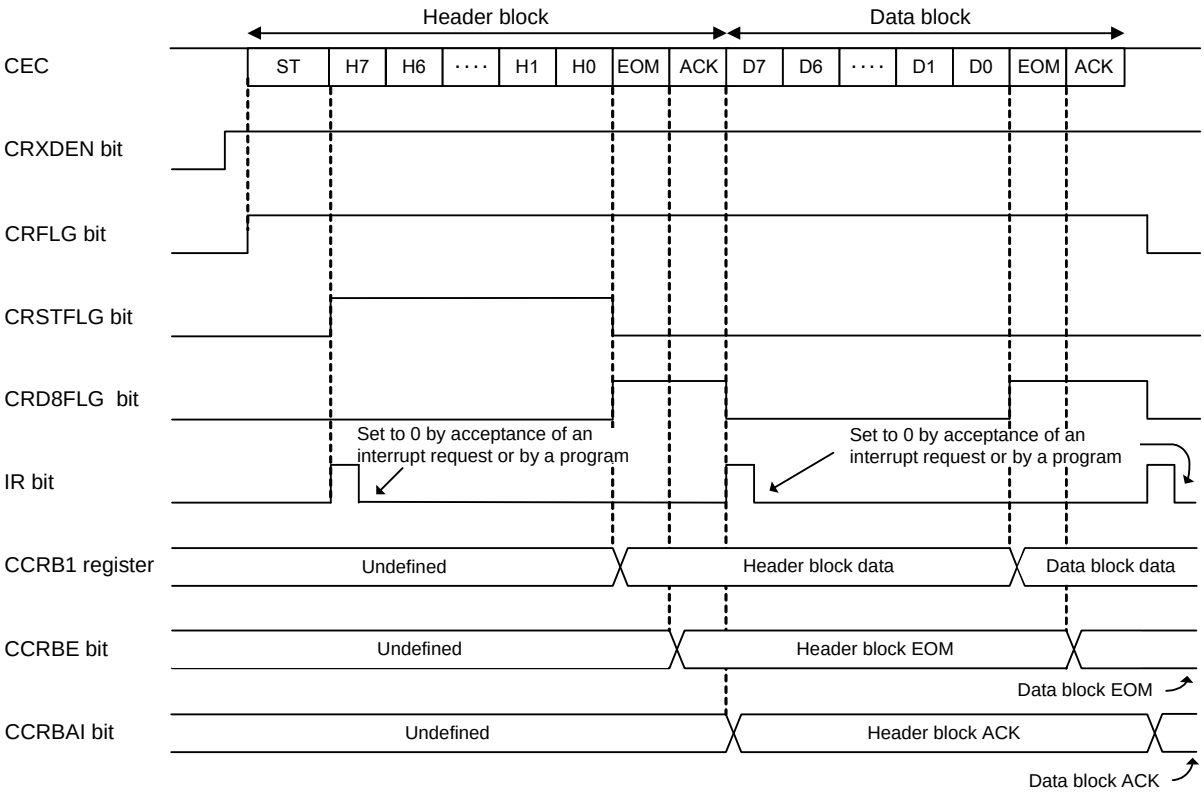
The output value of the 10th bit (ACK bit) can be selected.
When the CRACK bit in the CECC2 register is set to 0 (inserted by program), the value of the CCRBAO bit in the CCRB2 register is output as ACK data.
When the CRACK bit is set to 1 (inserted by hardware), ACK is output when the received Destination address matches the address selected by the CRADRI1 or CRADRI2 register (own address). Table 26.8 lists ACK Output.

Table 26.8 ACK Output

CRACK Bit	CCRBAO Bit	Destination Address		ACK Output
		Received Destination Address	Address selected by the CRADRI1 or CRADRI2 Register (Own Address)	
0	0	-	-	ACK
	1	-	-	NACK
1	-	Directly address (0000b to1110b)	Matches received Destination address	ACK
			Not match received Destination address	NACK
		Broadcast address (1111b)	1111b (matches received Destination address)	ACK
			0000b to 1110b	NACK

26.3.5.4 Reception Examples

Figure 26.9 shows a Reception Example and Figure 26.10 shows a Reception Example (Change from Error Low Pulse Output Disabled to Enabled When an Error Occurs).
When a receive error occurs, the CRERRFLG bit in the CECFLG register becomes 1 (receive error). If a reception ends due to the error during the reception, set the CRXDEN bit in the CECC3 register to 0 (receive disabled). When the CRXDEN bit is set to 0, the CRERRFLG bit becomes 0. To restart the reception, set the CRXDEN bit to 0 (reception disabled), and then set the CRXDEN bit to 1 (reception enabled) after waiting for one or more cycles of the count source.

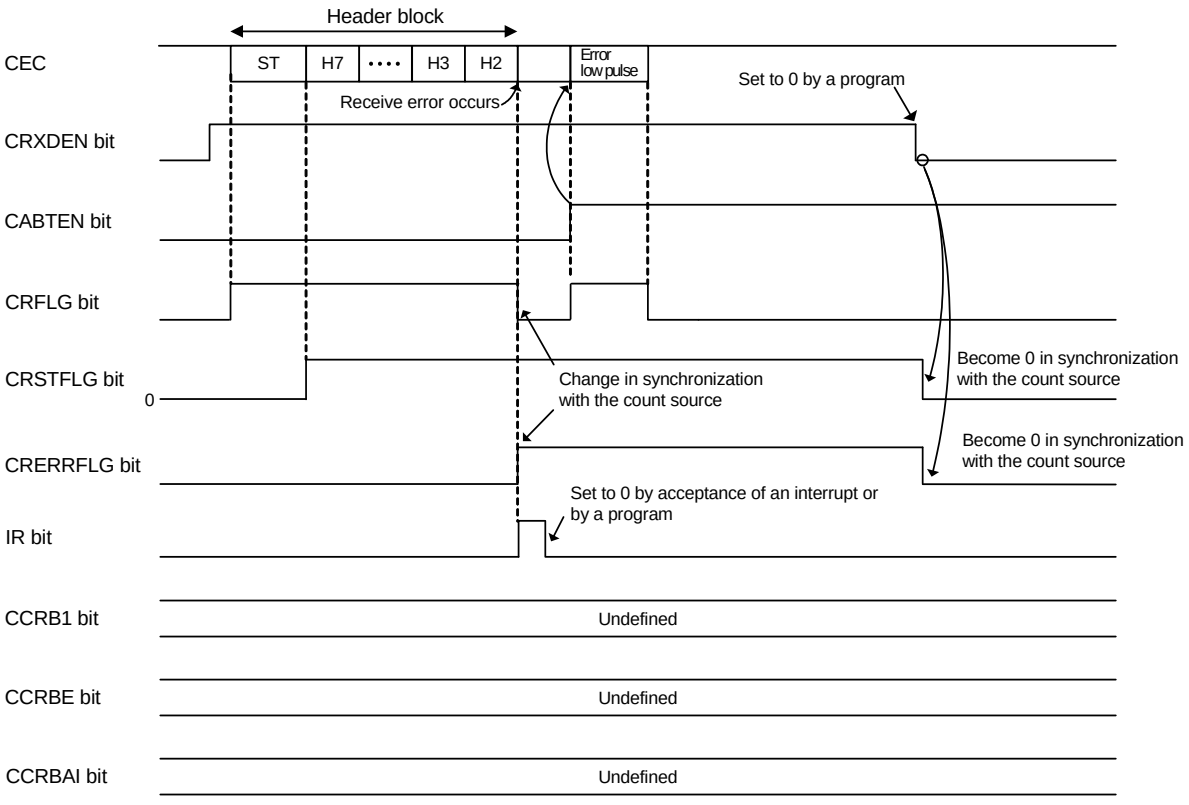


CRXDEN bit: Bit in the CECC3 register
Bits CRFLG, CRD8FLG, and CRSTFLG: Bits in the CECFLG register
IR bit: Bit in the CEC2IC register
Bits CCRBE and CCRBAI: Bits in the CCRB2 register

The above diagram applies under the following conditions.

- The CFIL bit in the CICC2 register is set to 0 (filter disabled).
- The CRISEL0 bit in the CISEL register is set to 0 (8th bit receive interrupt disabled).
- The CRISEL1 bit in the CISEL register is set to 1 (10th bit receive interrupt enabled).
- The CRISELS bit in the CISEL register is set to 1 (reception start bit interrupt enabled).

Figure 26.9 Reception Example



CRXDEN bit: Bit in the CECC3 register
Bits CRFLG, CRERRFLG, and CRSTFLG: Bits in the CECFLG register
IR bit: Bit in the CEC2IC register
Bits CCRBE and CCRBAI: Bits in the CCRB2 register

The above diagram applies under the following conditions.

- The CFIL bit in the CECC2 register is se to 0 (filter disabled)
- The CABTEN bit in the CECC4 register is set to 1 (error low pulse output enabled)
- The CRISEL2 bit in the CISEL register is set to 1 (receive error interrupt enabled)
- The CRISELS bit in the CISEL register is se to 0 (reception start bit interrupt disabled)

Figure 26.10 Reception Example (Change from Error Low Pulse Output Disabled to Enabled When an Error Occurs)

26.3.6 Transmission

26.3.6.1 Transmit Signal Timing Select

Rising or falling timing of the transmit signal can be selected.
The rising timing of the transmit signal is selected by bits CRISE2 to CRISE0 in the CECC4 register.
Figure 26.11 shows Rising Timing of Transmit Signal.

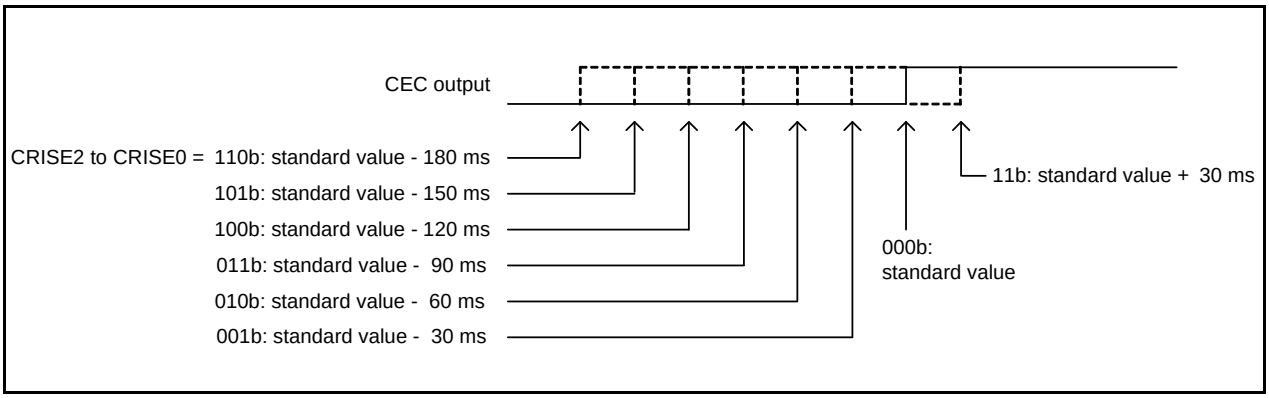


Figure 26.11 Rising Timing of Transmit Signal

The falling timing of the transmit signal is selected by bits CFALL1 to CFALL0 in the CECC4 register.
Figure 26.12 shows Falling Timing of Transmit Signal.

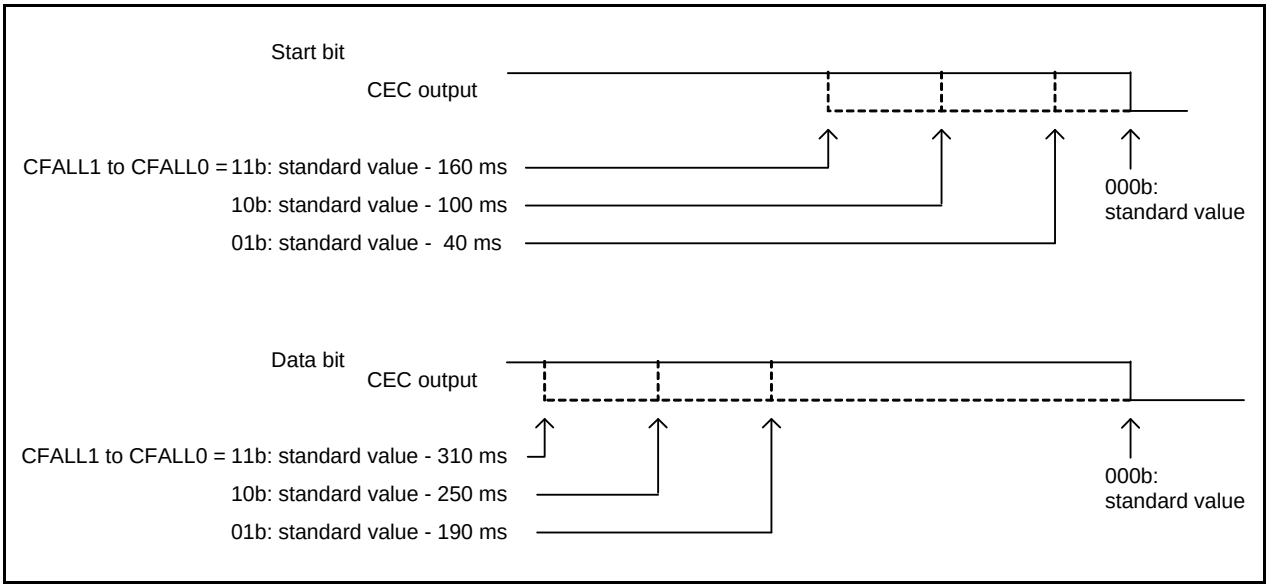


Figure 26.12 Falling Timing of Transmit Signal

26.3.6.2 Arbitration Lost Detection

When data is transmitted, an arbitration lost is detected in the following cases.

- The CEC output changes from Hi-Z to low by the external source (falling edge).
- The CEC output changes from low to Hi-Z by the external source (rising edge).

A range for detecting the arbitration lost the rising edge is selected by the CTABTS bit in the CECC2 register. Figure 26.13 shows Arbitration Lost Detectable Range.

When the arbitration lost is detected, the CTABTFLG bit in the CECFLG register becomes 1 (arbitration lost detected).

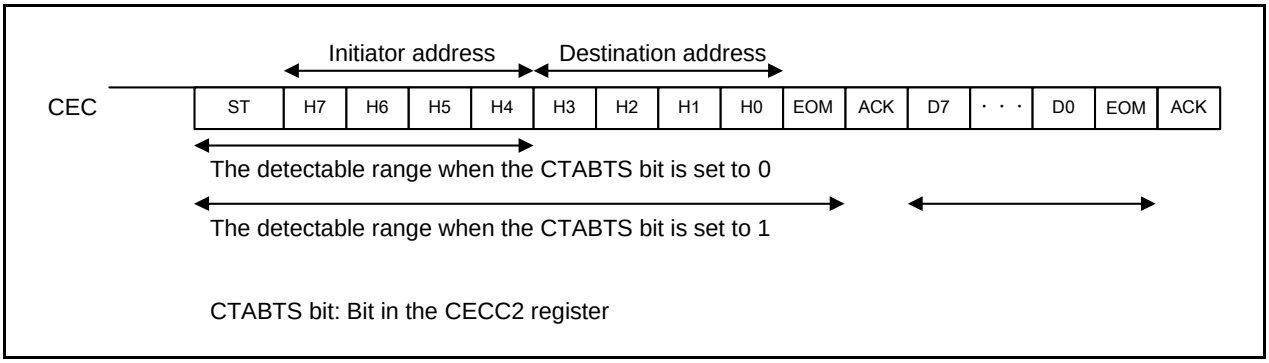
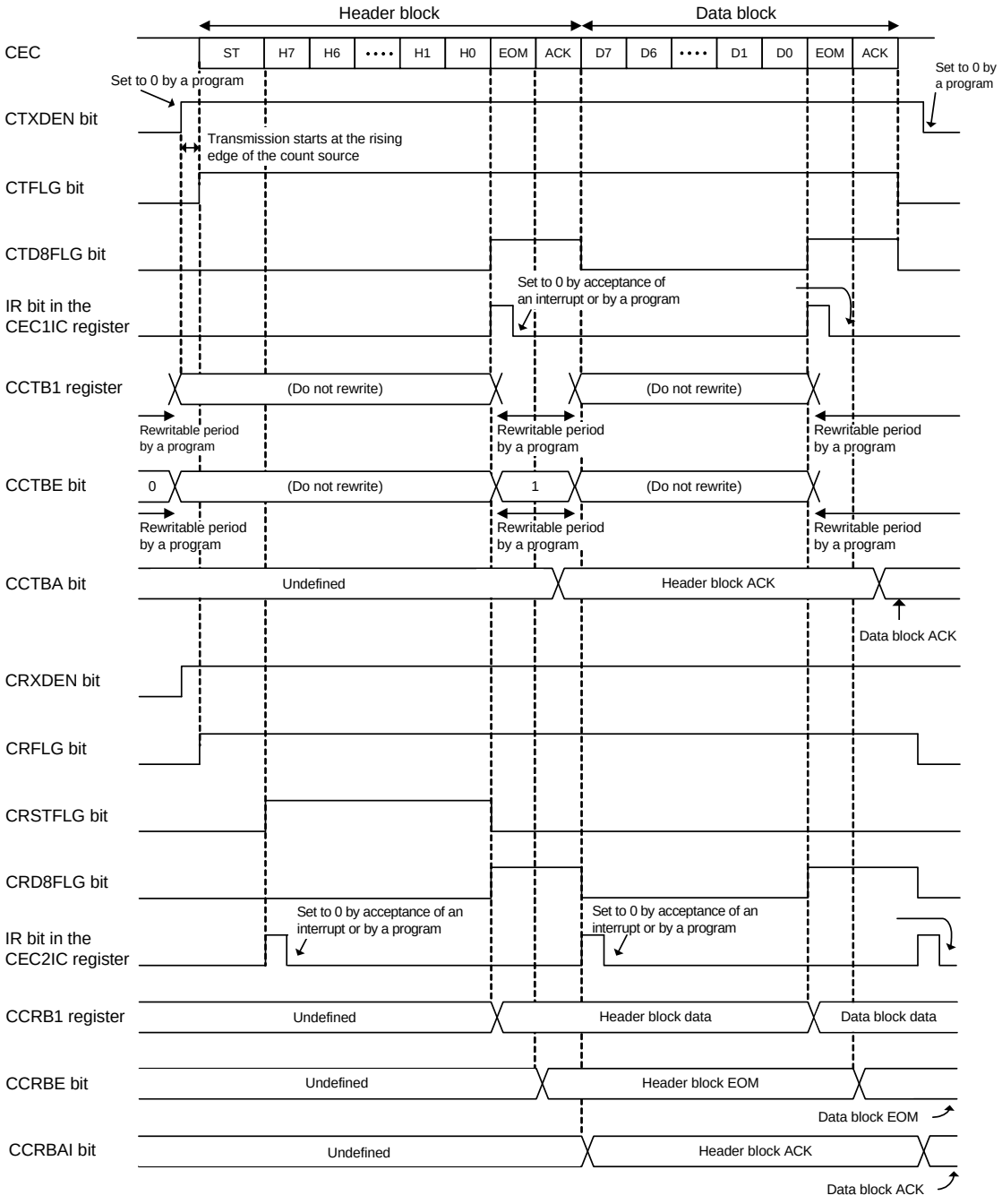


Figure 26.13 Arbitration Lost Detectable Range

26.3.6.3 Transmission Example

Figure 26.14 shows a Transmission Example, Figure 26.15 shows a Transmission Example (When NACK Received) and Figure 26.16 shows a Transmission Example (When an Arbitration Lost Detected).

Set the CTXDEN bit in the CECC3 register to 0 (transmit disabled) after the transmission. To continue the transmission, set the CTXDEN bit to 0 (transmit disabled) after sending one frame (one header block and one or more data blocks), and wait for one or more cycles of the count source before setting the CTXDEN bit to 1 (transmit enabled).

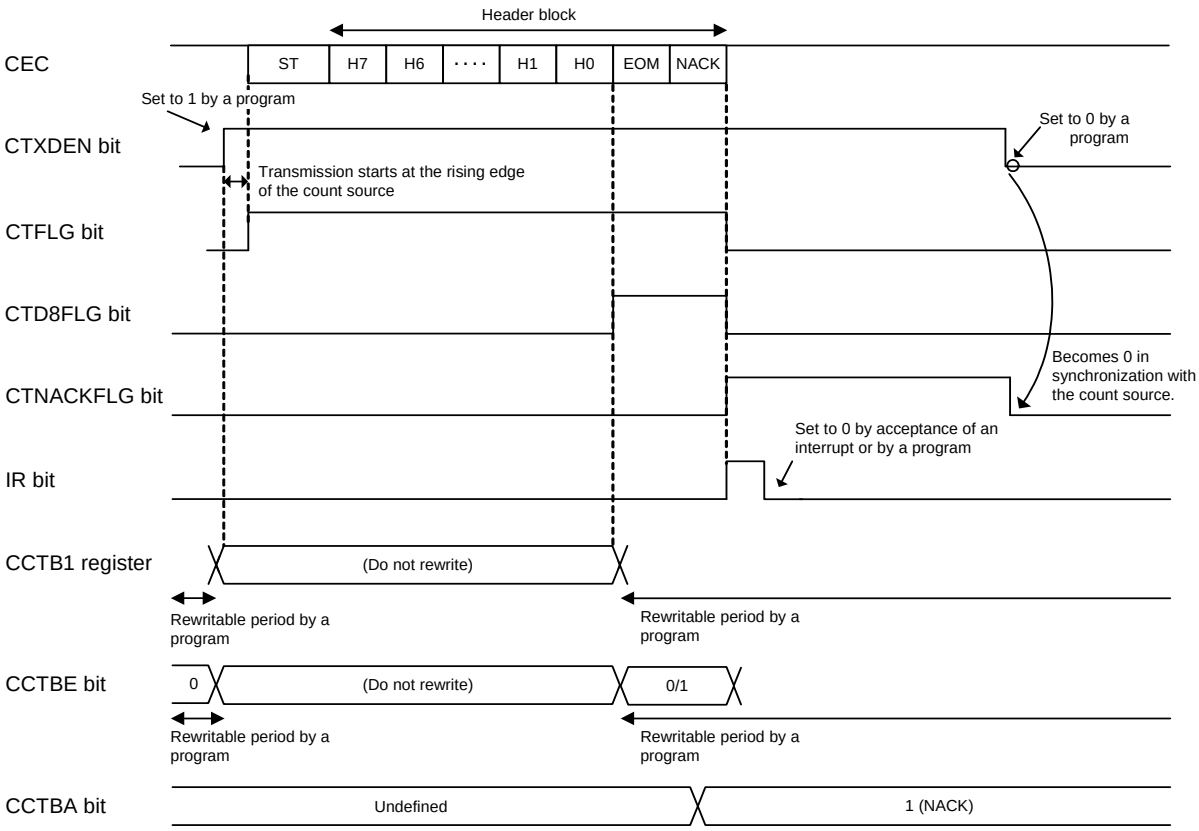


Bits CTXDEN and CRXDEN: Bits in the CECC3 register
Bits CTFLG, CTD8FLG, CRFLG, CRD8FLG, and CRSTFLG: Bits in the CECFLG register
Bits CCTBE and CCTBA: Bits in the CCTB2 register
Bits CCRBE and CCRBAI: Bits in the CCRB2 register

The above diagram applies under the following conditions:

- The CTISEL0 bit in the CISEL register is set to 1 (8th bit transmit interrupt enabled).
- The CTISEL1 bit in the CISEL register is set to 0 (10th bit transmit interrupt disabled).
- The CEMOM bit in the CECC3 register is set to 0 (EOM enabled).
- The CFIL bit in the CECC2 register is set to 0 (filter disabled).
- The CRISEL0 bit in the CISEL register is set to 0 (8th bit receive interrupt disabled).
- The CRISEL1 bit in the CISEL register is set to 1 (10th bit receive interrupt enabled).
- The CRISELS bit in the CISEL register is set to 1 (reception start bit interrupt enabled).

Figure 26.14 Transmission Example

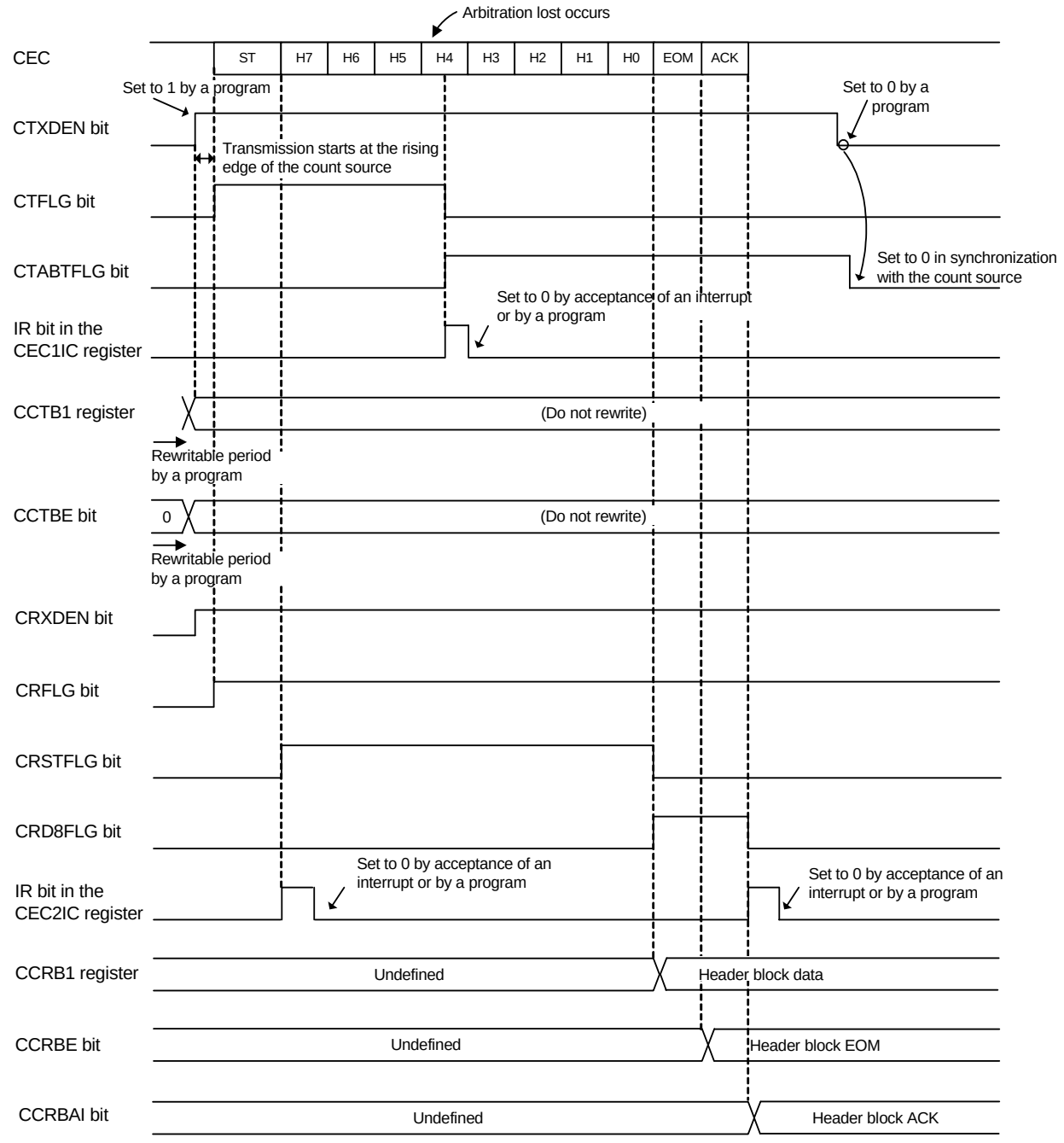


CTXDEN bit: Bit in the CECC3 register
Bits CTFLG, CTD8FLG, and CTNACKFLG: Bits in the CECFLG register
IR bit: Bit in the CEC1IC register
Bits CCTBE and CCTBA: Bits in the CCTB2 register

The above diagram applies under the following conditions.

- The CTISEL2 bit in the CISEL register is set to 1 (transmit NACK interrupt enabled).
- The CTNACK bit in the CECC2 register is set to 1, and the CTACKEN bit is 1 (transmission stops with NACK).

Figure 26.15 Transmission Example (When NACK Received)



Bits CTXDEN and CRXDEN: Bits in the CECC3 register
Bits CTFLG, CTABTFLG, CRFLG, CRD8FLG, and CRSTFLG: Bits in the CECFLG register
Bits CCRBE and CCRBAI: Bits in the CCRB2 register
CCTBE bit: Bit in the CCTB2 register

The above diagram applies under the following conditions:

- The CTISEL1 bit in the CISEL register is set to 1 (transmit arbitration lost interrupt enabled).
- The CFIL bit in the CECC2 register is set to 0 (filter enabled).
- The CRISEL0 bit in the CISEL register is set to 0 (8th bit receive interrupt disabled).
- The CRISEL1 bit in the CISEL register is set to 1 (10th bit receive interrupt enabled).
- The CRISELS bit in the CISEL register is set to 1 (reception start bit interrupt enabled).

Figure 26.16 Transmission Example (When an Arbitration Lost Detected)

26.4 Interrupts

The CEC function has CEC1 interrupt and CEC2 interrupt. Table 26.9 and Table 26.10 list CEC Interrupt Sources. These sources cause a request of CEC1 interrupt or CEC2 interrupt. When the CRISELM bit in the CISEL register is set to 1, the 8th/10th bit receive interrupt request is generated if the received Destination address is either one of the following case:

- Matches the address selected by the CRADRI1 or CRADRI2 register.
- Broadcast (1111b)

Figure 26.17 shows CEC Function Interrupt.

Table 26.9 CEC1 Interrupt Sources

Type	Source	Interrupt Request Timing	Interrupt Enable Bit
Transmit interrupt	8th bit transmitted	When the CTD8FLG bit change from 0 to 1.	CRISEL0
	10th bit transmitted	When the CTD8FLG bit changes from 1 to 0.	CRISEL1
Transmit error interrupt	Arbitration lost	When the CTABTFLG bit changes from 0 to 1.	CTISEL2
	NACK received (Directly address) ACK received (Broadcast)	When the CTNACKFLG bit changes from 0 to 1.	

CTD8FLG, CTABTFLG, CTNACKFLG: Bits in the CECFLG register

Table 26.10 CEC2 Interrupt Sources

Type	Source	Interrupt Request Timing	Interrupt Enable Bit
Receive interrupt	8th bit received	When the CRD8FLG bit changes from 0 to 1 (1)	CRISEL0
	10th bit received	When the CRD8FLG bit changes from 1 to 0 (1)	CRISEL1
	Start bit detected	When the CRSTFLG bit changes from 0 to 1	CRISELS
Receive error interrupt	Nonstandard signal received	Wen the CRERRFLG bit changes from 0 to 1	CRISEL2

CRD8FLG, CRSTFLG, CRERRFLG: Bits in the CECFLG register

Note:

1. The CRISELM bit in the CISEL register affects the interrupt.

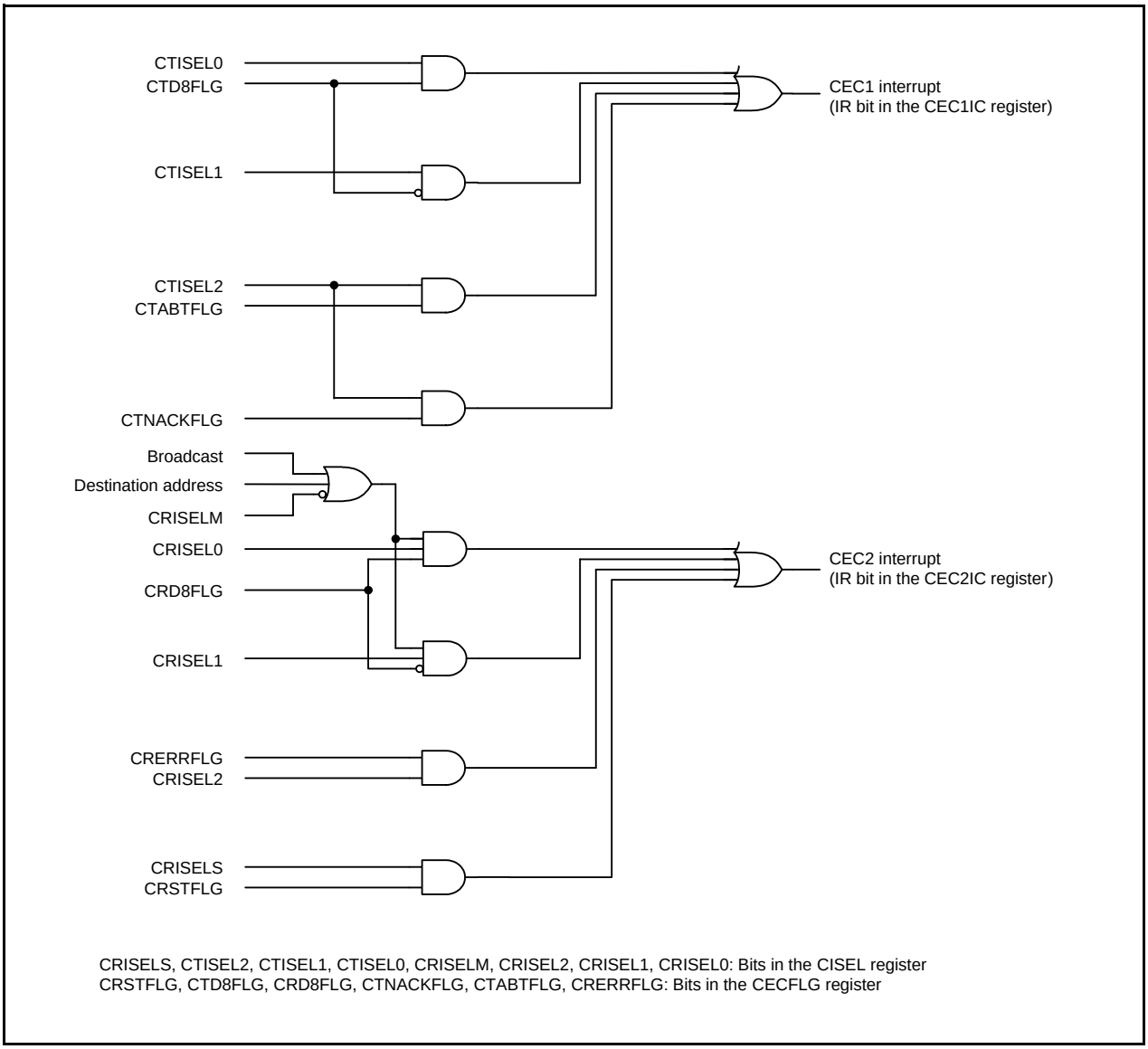


Figure 26.17 CEC Function Interrupt

For the interrupt request timing, refer to the operation examples.
For interrupt control, refer to 14.7 “Interrupt Control”. Table 26.11 lists CEC Function Interrupt-Associated Registers.

Table 26.11 CEC Function Interrupt-Associated Registers

Address	Register Name	Register Symbol	After Reset
006Bh	CEC1 Interrupt Control Register	CEC1IC	XXXX X000b
006Ch	CEC2 Interrupt Control Register	CEC2IC	XXXX X000b
0205h	Interrupt Source Select Register 3	IFSR3A	00h

The CEC function shares the interrupt vectors and the interrupt control registers with other peripheral functions. To use CEC1 interrupt, set the IFSR33 bit in the IFSR3A register to 1 (CEC1). To use CEC2 interrupt, set the IFSR34 bit in the IFSR3A register to 1 (CEC2).

26.5 Notes on CEC (Consumer Electronics Control)

26.5.1 Registers and Bit Operation

The registers and the bits of the CEC function are synchronized with the count source. Therefore, the internal circuit starts to operate from the next count source timing, while the contents of the register is changed immediately after rewriting the value of the register.
When changing the value of the same bit successively or reading the bit changed under the influence of another bit, wait for one or more cycles of the count source.

Example: when changing the value of the same bit successively
(1) Change the bit to 0.
(2) Wait for one or more cycles of the count source.
(3) Change the same bit to 1.

Example: when reading the bit changed under the influence of another bit
(after the reception is disabled, to ensure that the CRERRFLG bit in the CECFLG register becomes 0 (no reception error detected)).
(1) Set the CRXDEN bit in the CECC3 register to 0 (reception disabled)
(2) Wait for one or more cycles of the count source
(3) Read the CRERRFLG bit in the CECFLG register.

27. A/D Converter

27.1 Introduction

A/D converter consists of one 10-bit successive approximation A/D converter.
Table 27.1 shows A/D Converter Specifications, Figure 27.1 shows an A/D Converter Block Diagram.

Table 27.1 A/D Converter Specifications

Item	Specification
A/D conversion method	Successive approximation
Analog input voltage	0 V to AVCC (VCC1)
Operating clock ϕAD	f1, f1 divided by 2, f1 divided by 3, f1 divided by 4, f1 divided by 6, f1 divided by 12, fOCO40M divided by 2, fOCO40M divided by 3, fOCO40M divided by 4, fOCO40M divided by 6, or fOCO40M divided by 12
Resolution	10 bits
Integral nonlinearity error	AVCC = VREF = 5 V AN0 to AN7, AN0_0 to AN0_7, or AN2_0 to AN2_7 input: ±3 LSB ANEX0 or ANEX1 input: ±3 LSB AVCC = VREF = 3.0 V AN0 to AN7, AN0_0 to AN0_7, or AN2_0 to AN2_7 input: ±3 LSB ANEX0 or ANEX1 input: ±3 LSB
Operation modes	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, repeat sweep mode 1
Analog input pins	8 pins (AN0 to AN7) + 2 pins (ANEX0 and ANEX1) + 8 pins (AN0_0 to AN0_7) + 8 pins (AN2_0 to AN2_7)
A/D conversion start conditions	• Software trigger The ADST bit in the ADCON0 register is set to 1 (A/D conversion start). • External trigger (retrigger is enabled) Input to the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1(A/D conversion start).
Conversion rate per pin	Minimum 43 ϕAD cycles

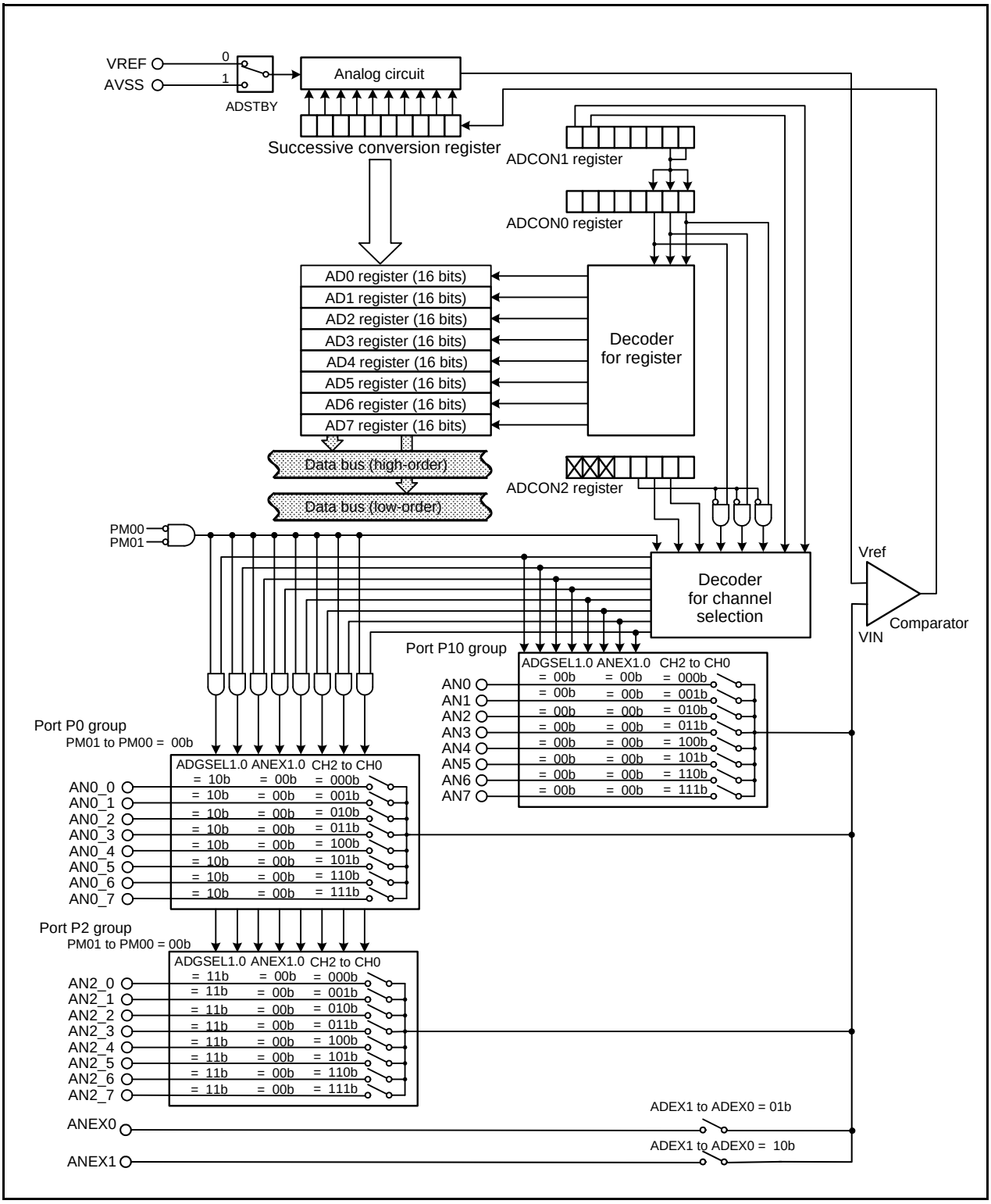


Figure 27.1 A/D Converter Block Diagram

Table 27.2 I/O Pins

Pin Name	Input/Output	Function
AN0 to AN7	Input	Analog input
ANEX0, ANEX1	Input	Analog input
AN0_0 to AN0_7	Input	Analog input
AN2_0 to AN2_7	Input	Analog input
$\overline{\text{ADTRG}}$	Input	Trigger input

Note:
1. Set the direction bit of the ports sharing a port to 0 (input mode).

27.2 Registers

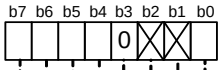
Table 27.3 lists registers associated with A/D converter. Set the CKS3 bit in the ADCON2 register before setting other registers associated with A/D converter excluding the PCR register. However, bits in the ADCON2 register and the CKS3 bit can be set simultaneously. After changing the CKS3 bit, set the registers in the same way again.
The PCR register can be set before setting the CKS3 bit. After changing the CKS3 bit, the PCR register does not need to be set again.

Table 27.3 Register Structure

Address	Register Name	Register Symbol	After Reset
0366h	Port Control Register	PCR	0000 0XX0b
03A2h	Open-Circuit Detection Assist Function Register	AINRST	XX00 0000b
03C0h 03C1h	A/D Register 0	AD0	XXXX XXXXb 0000 00XXb
03C2h 03C3h	A/D Register 1	AD1	XXXX XXXXb 0000 00XXb
03C4h 03C5h	A/D Register 2	AD2	XXXX XXXXb 0000 00XXb
03C6h 03C7h	A/D Register 3	AD3	XXXX XXXXb 0000 00XXb
03C8h 03C9h	A/D Register 4	AD4	XXXX XXXXb 0000 00XXb
03CAh 03CBh	A/D Register 5	AD5	XXXX XXXXb 0000 00XXb
03CCh 03CDh	A/D Register 6	AD6	XXXX XXXXb 0000 00XXb
03CEh 03CFh	A/D Register 7	AD7	XXXX XXXXb 0000 00XXb
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b

27.2.1 Port Control Register (PCR)

Port Control Register



Symbol: PCR | Address: 0366h | After Reset: 0000 0XX0b

Bit Symbol	Bit Name	Function	RW
PCR0	Port P1 control bit	Operation performed when the P1 register is read 0 : When the port is set to input, the input levels of pins P1_0 to P1_7 are read. When set to output, the port latch is read. 1 : The port latch is read regardless of whether the port is set to input or output.	RW
— (b2-b1)	No register bits. If necessary, set to 0. Read as undefined		—
— (b3)	Reserved bit	Set to 0	RW
PCR4	CEC output enable bit	0 : CEC output disabled 1 : CEC output enabled	RW
PCR5	$\overline{INT6}$ input enable bit	0 : Enabled 1 : Disabled	RW
PCR6	$\overline{INT7}$ input enable bit	0 : Enabled 1 : Disabled	RW
PCR7	Key input enable bit	0 : Enabled 1 : Disabled	RW

PCR5 ($\overline{INT6}$ Input Enable Bit) (b5)

Set the PCR5 bit to 1 ($\overline{INT6}$ input disabled) when using the AN2_4 pin is used for analog input.

PCR6 ($\overline{INT7}$ Input Enable Bit) (b6)

Set the PCR6 bit to 1 ($\overline{INT7}$ input disabled) when using AN2_5 pin is used for analog input.

PCR7 (key Input Enable Bit) (b7)

Set the PCR7 bit to 1 (key input disabled) when using pins AN4 to AN7 are used for analog input.

27.2.2 Open-Circuit Detection Assist Function Register (AINRST)

Open-Circuit Detection Assist Function Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol: AINRST
Address: 03A2h
After Reset: XX00 0000b

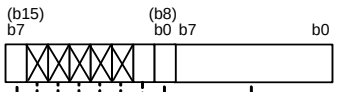
Bit Symbol	Bit Name	Function	RW
— (b3-b0)	No register bits. If necessary, set to 0. Read as undefined value		—
AINRST0	Open-circuit detection assist function enable bit	b5 b4 0 0 : Open-circuit detection disabled 0 1 : Precharge before conversion 1 0 : Discharge before conversion 1 1 : Do not set	RW
AINRST1			RW
— (b7-b6)	No register bits. If necessary, set to 0. Read as undefined value		—

AINRST1-AINRST0 (Open-circuit Detection Assist Function Enable Bit) (b5-b4)

To enable the A/D open-circuit detection assist function, set the AINRST0 bit or AINRST1 bit to 1, and then set the ADST bit in the ADCON0 register to 1 (A/D conversion) after waiting for one cycle of ϕAD.

27.2.3 AD Register i (ADi) (i = 0 to 7)

A/D Register (i = 0 to 7)



Symbol	Address	After Reset
AD0	03C1h to 03C0h	0000 00XX XXXX XXXXb
AD1	03C3h to 03C2h	0000 00XX XXXX XXXXb
AD2	03C5h to 03C4h	0000 00XX XXXX XXXXb
AD3	03C7h to 03C6h	0000 00XX XXXX XXXXb
AD4	03C9h to 03C8h	0000 00XX XXXX XXXXb
AD5	03CBh to 03CAh	0000 00XX XXXX XXXXb
AD6	03CDh to 03CCh	0000 00XX XXXX XXXXb
AD7	03CFh to 03CEh	0000 00XX XXXX XXXXb

Function		RW
Eight low-order bits of A/D conversion result		RO
Two high-order bits of A/D conversion result		RO
No register bits. If necessary, set to 0. Read as 0		—
Reserved bit	Read as 0	RO

The A/D conversion result is stored in the ADi register corresponding to pins ANi, ANEXi, AN0_i, and AN2_i. Table 27.4 lists Analog Pin and A/D Conversion Result Storing Register.

Table 27.4 Analog Pin and A/D Conversion Result Storing Register

Analog Pin				A/D Conversion Result Storing Register
AN0	ANEX0	AN0_0	AN2_0	AN0 register
AN1	ANEX1	AN0_1	AN2_1	AN1 register
AN2		AN0_2	AN2_2	AN2 register
AN3		AN0_3	AN2_3	AN3 register
AN4		AN0_4	AN2_4	AN4 register
AN5		AN0_5	AN2_5	AN5 register
AN6		AN0_6	AN2_6	AN6 register
AN7		AN0_7	AN2_7	AN7 register

27.2.4 A/D Control Register 2 (ADCON2)

A/D Control Register 2

b7	b6	b5	b4	b3	b2	b1	b0
	0	0		X			X

Symbol	Address	After Reset
ADCON2	03D4h	0000 X00Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	No register bit. If necessary, set to 0. Read as undefined value		—
ADGSEL0	A/D input group select bit	b2 b1 0 0 : AN0 to AN7 0 1 : Do not set 1 0 : AN0_0 to AN0_7 1 1 : AN2_0 to AN2_7	RW
ADGSEL1			RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
CKS2	Frequency select bit 2	Refer to the CKS0 bit in the ADCON0 register.	RW
— (b6-b5)	Reserved bits	Set to 0	RW
CKS3	fAD select bit	0: f1 1: fOCO40M	RW

If the ADCON2 register is rewritten during A/D conversion, the conversion result is undefined.

ADGSEL1-ADGSEL0 (A/D Input Group Select Bit) (b2-b1)

AN0_0 to AN0_7 are used as analog input pins even if bits PM01 to PM00 are set to 01b (memory expansion mode) and bits PM05 to PM04 are 11b (multiplexed bus is allocated to the entire $\overline{CS}$ space).

CKS3 (fAD Select Bit) (b7)

Set the CKS3 bit while A/D conversion stops.
Set the CKS3 bit, and then set other A/D converter related registers. Also, after changing the CKS3 bit, set the A/D converter related registers again. Note that bits in the ADCON2 register and the CKS3 bit can be set simultaneously.

27.2.5 A/D Control Register 0 (ADCON0)

A/D Control Register 0

Symbol	Address	After Reset
ADCON0	03D6h	0000 0XXXb

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Function varies with operation mode	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 0 0 : One-shot mode 0 1 : Repeat mode 1 0 : Single sweep mode 1 1 : Repeat sweep mode 0 or repeat sweep mode 1	RW
MD1			RW
TRG	Trigger select bit	0 : Software trigger 1 : ADTRG trigger	RW
ADST	A/D conversion start flag	0 : A/D conversion stop 1 : A/D conversion start	RW
CKS0	Frequency select bit 0	Refer to the next page.	RW

If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.

MD1-MD0 (A/D Operation Mode Select Bit) (b4-b3)

A/D operation mode is selected by a combination of bits MD1 to MD0 and the MD2 bit in the ADCON1 register. Table 27.5 lists A/D Operation Mode.

Table 27.5 A/D Operation Mode

Bit Setting			A/D Operation Mode
ADCON1 Register	ADCON0 Register		
MD2	MD1	MD0	
0	0	0	One-shot mode
0	0	1	Repeat mode
0	1	0	Single sweep mode
0	1	1	Repeat sweep mode 0
1	1	1	Repeat sweep mode 1

Do not set bit combinations not listed above.

CKS0 (Frequency Select Bit) (b7)

ϕAD frequency is selected by a combination of the CKS0 bit in the ADCON0 register, the CKS1 bit in the ADCON1 register, and bits CKS3 and CKS2 in the ADCON2 register. Select bits CKS2 to CKS0 after setting the CKS3 bit in the ADCON2 register. Note that bits CKS3 and CKS2 can be set simultaneously. Table 27.6 lists ϕ A/D Frequency.

Table 27.6 ϕ A/D Frequency

CKS3	CKS2	CKS1	CKS0	ϕA/D
0	0	0	0	fAD(f1) divided by 4
	0	0	1	fAD(f1) divided by 2
	0	1	0	fAD(f1)
	0	1	1	
	1	0	0	fAD(f1) divided by 12
	1	0	1	fAD(f1) divided by 6
	1	1	0	fAD(f1) divided by 3
	1	1	1	
1	0	0	0	fAD(fOCO40M) divided by 4
	0	0	1	fAD(fOCO40M) divided by 2
	1	0	0	fAD(fOCO40M) divided by 12
	1	0	1	fAD(fOCO40M) divided by 6
	1	1	0	fAD(fOCO40M) divided by 3
	1	1	1	

Note:
1. Do not set bit combinations not listed above.

27.2.6 A/D Control Register 1 (ADCON1)

A/D Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
				X			

Symbol	Address	After Reset
ADCON1	03D7h	0000 X000b

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit	Function varies with operation mode	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	0 : Any mode other than repeat sweep mode 1 1 : Repeat sweep mode 1	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
CKS1	Frequency select bit 1	Refer to the CKS0 bit in the ADCON0 register	RW
ADSTBY	A/D standby bit	0 : A/D operation stopped (standby) 1 : A/D operation enabled	RW
ADEX0	Extended pin select bit	Function varies with operation mode	RW
ADEX1			RW

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

MD2 (A/D Operation Mode Select Bit 1) (b2)

A/D operation mode is selected by a combination of bits MD1 to MD0 in the ADCON0 register and the MD2 bit. Refer to Table 27.5 “A/D Operation Mode”.

ADSTBY (A/D Standby Bit) (b5)

If the ADSTBY bit is changed from 0 (A/D operation stopped) to 1 (A/D operation enabled), wait for 1 ϕA/D cycle or more before starting A/D conversion.

When the A/D converter is not used, no current flows in the A/D converter by setting the ADSTBY bit to 0 (A/D operation stopped: standby). This helps the power consumption to be reduced.

27.3 Operations

27.3.1 A/D Conversion Cycle

A/D conversion cycle is based on fAD and ϕAD. Figure 27.2 shows fAD and ϕAD.
When the CKS3 bit in the ADCON2 register is 1 (fOCO40M is fAD), do not set the CKS2 bit in the ADCON2 register to 0 and the CKS1 bit in the ADCON1 register to 1 (fDA = ϕAD).
Set the A/D converter related registers after setting the CKS3 bit.

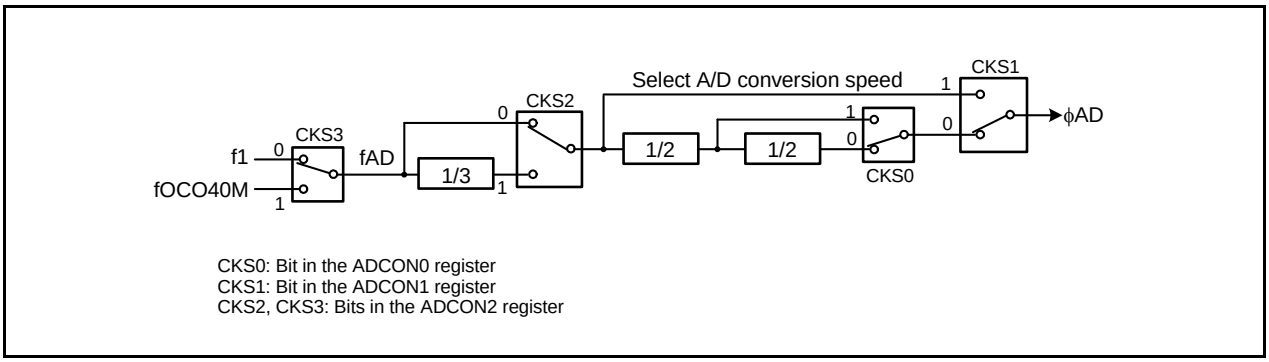


Figure 27.2 fAD and ϕAD

Figure 27.3 shows A/D Conversion Timing.

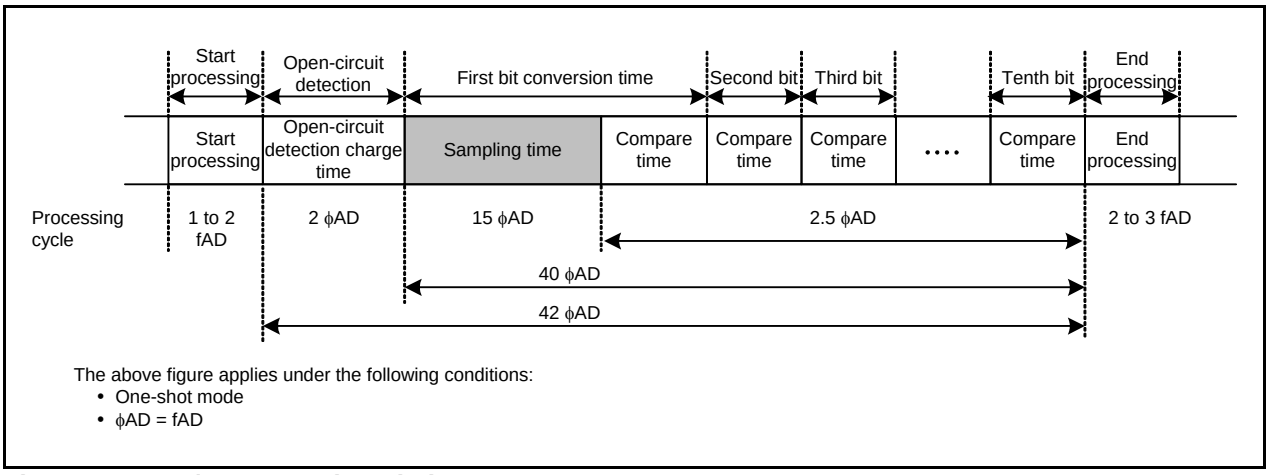


Figure 27.3 A/D Conversion Timing

Table 27.7 lists Cycles of A/D Conversion Item. A/D conversion period is as follows.
Start processing time depends on which ϕAD is selected.
A/D conversion starts after the start processing time elapses by setting the ADST bit in the ADCON0 register to 1 (A/D conversion start). When reading the ADST bit before starting A/D conversion, 0 (A/D conversion stop) is read.
When selecting multiple pins and in A/D conversion repeat mode, between-execution processing time is inserted between A/D conversions.
In one-shot mode and single sweep mode, the ADST bit becomes 0 at the end processing time and the last A/D conversion result is stored in the ADi register.

One-shot mode:
Start processing time + A/D conversion execution time + end processing time
Two pins are selected in single sweep mode:
Start processing time + (A/D conversion execution time + between-execution processing time + A/D conversion execution time) + end processing time

Table 27.7 Cycles of A/D Conversion Item

A/D Conversion Item		Cycle
Start processing time	ϕAD = fAD	1 to 2 cycles of fAD
	ϕAD = fAD divided by 2	2 to 3 cycles of fAD
	ϕAD = fAD divided by 3	3 to 4 cycles of fAD
	ϕAD = fAD divided by 4	3 to 4 cycles of fAD
	ϕAD = fAD divided by 6	4 to 5 cycles of fAD
	ϕAD = fAD divided by 12	7 to 8 cycles of fAD
A/D conversion execution time	Open-circuit detection disabled	40 cycles of ϕAD
	Open-circuit detection enabled	42 cycles of ϕAD
Between-execution processing time		1 cycle of ϕAD
End processing time		2 to 3 cycles of fAD

27.3.2 A/D Conversion Start Conditions

An A/D conversion start trigger has a software trigger and an external trigger. Figure 27.4 shows A/D Conversion Start Trigger.

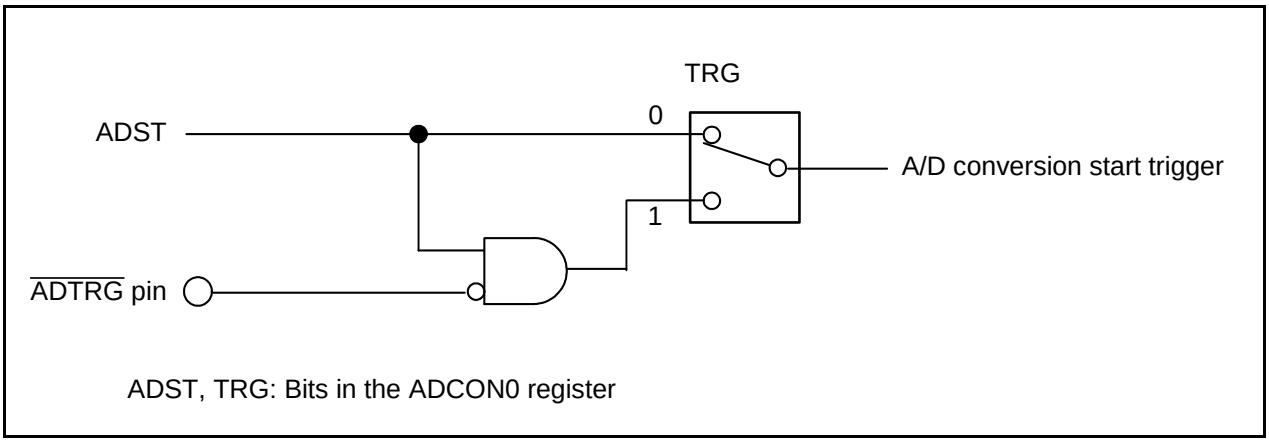


Figure 27.4 A/D Conversion Start Trigger

27.3.2.1 Software Trigger

When the TRG bit in the ADCON0 register is 0 (software trigger), A/D conversion starts by setting the ADST bit in the ADCON0 register to 1 (A/D conversion start).

27.3.2.2 External Trigger

When the TRG bit in the ADCON0 register is 1 ($\overline{\text{ADTRG}}$ trigger), A/D conversion starts if the input level at the $\overline{\text{ADTRG}}$ pin changes from high to low under the following conditions:

- The direction bit of the port sharing a pin is set to 0 (input mode)
- The TRG bit in the ADCON0 register is set to 1 ($\overline{\text{ADTRG}}$ trigger)
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion start)

Under the above conditions, when input to the $\overline{\text{ADTRG}}$ pin is changed from high to low, the A/D conversion starts.

Set the high- and low-level durations of the pulse input to the ADTRG pin to two or more cycles of fAD.

27.3.3 A/D Conversion Result

When reading the ADi register before A/D conversion is completed, the undefined value is read. Read the ADi register after completing A/D conversion. Use the following procedure to detect the completion of A/D conversion.

- In one-shot mode and single sweep mode:
  The IR bit in the ADIC register becomes 1 (interrupt requested) at the completion of A/D conversion. Ensure that the IR bit becomes 1 to read the ADi register.
  when not using A/D interrupt, set the IR bit to 0 (interrupt not requested) by a program after reading the ADi register.

- In repeat mode, repeat sweep mode 0, and repeat sweep mode 1:
  The IR bit remain unchanged (no interrupt request is generated). At first, read the ADi register after one A/D conversion period elapses (refer to 27.3.1 “A/D Conversion Cycle”). After that, whenever the ADi register is read, the conversion result which has been obtained before reading is read.
  The ADi register is overwritten in every A/D conversion. Read the value before the ADi register is overwritten.

27.3.4 Extended Analog Input Pins

In one-shot mode and repeat modes, pins ANEX0 and ANEX1 can be used as analog input pins by setting bits ADEX1 to ADEX0 in the ADCON1 register.
The A/D conversion result of pins ANEX0 and ANEX1 are respectively stored in registers AD0 and AD1.

27.3.5 Current Consumption Reduce Function

When the A/D converter is not in use, the power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stopped: standby) to shut off any analog circuit current flow.
To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for 1 ϕAD cycle or more before setting the ADST bit in the ADCON0 register to 1 (A/D conversion start). Do not set bits ADST and ADSTBY to 1 at the same time.
Also, do not set the ADSTBY bit to 0 (A/D operation stopped: standby) during A/D conversion.

27.3.6 Open-Circuit Detection Assist Function

The A/D converter has a function to set charge of the sampling capacitor to a predefined state (AVCC or AVSS) before A/D conversion starts in order to prevent the effect of analog input voltage of previous conversion. This function enables to detect open-circuit of a trace connected to the analog input pin certainly.
Figure 27.5 shows A/D Open-Circuit Detection Example on AVCC (Precharge) and Figure 27.6 shows A/D Open-Circuit Detection Example on AVSS (Predischarge).
The conversion result in open-circuit depends on the external circuit. Use this function only after careful evaluation for the system.

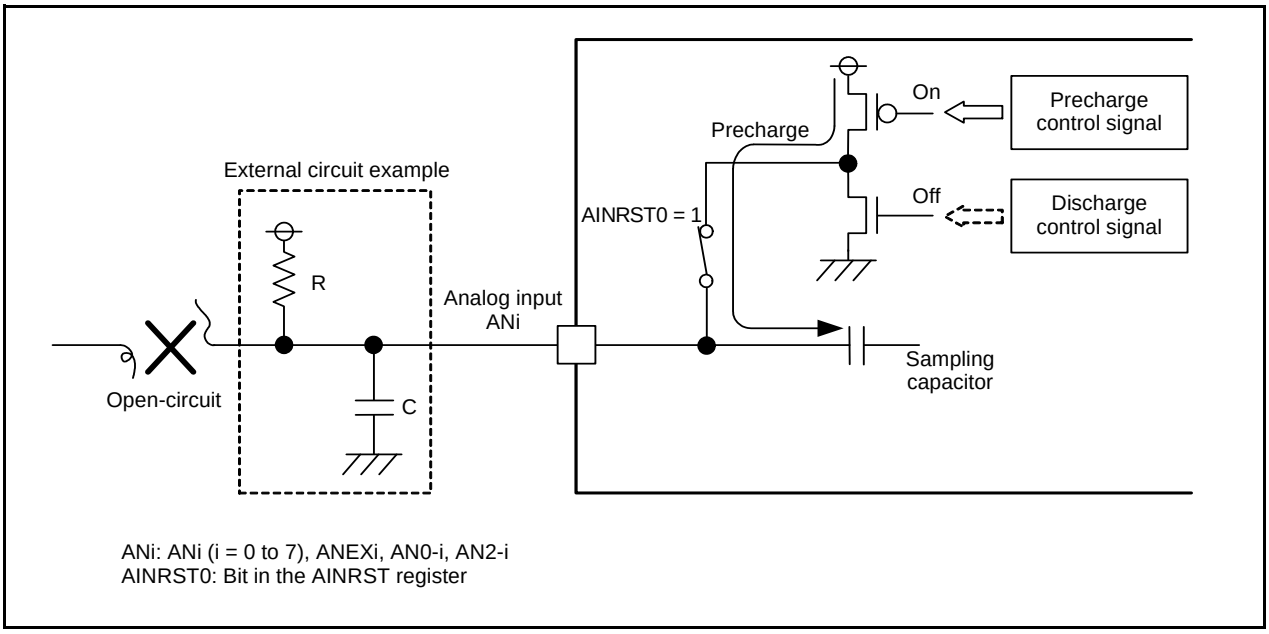


Figure 27.5 A/D Open-Circuit Detection Example on AVCC (Precharge)

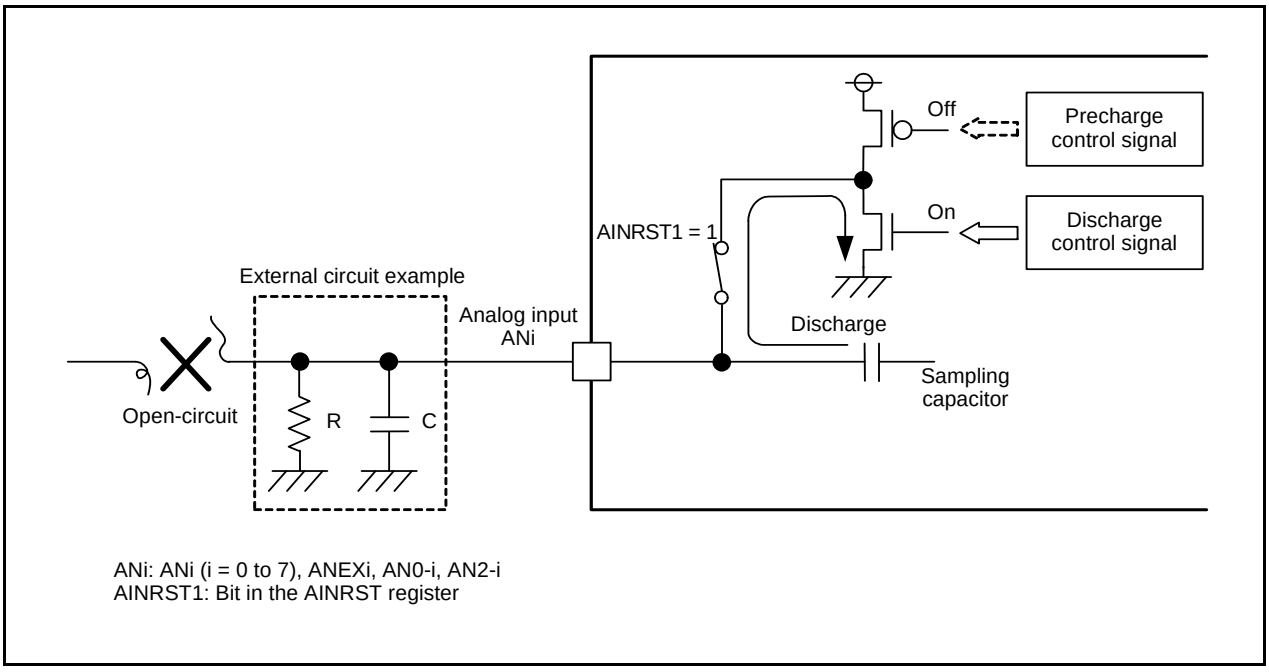


Figure 27.6 A/D Open-Circuit Detection Example on AVSS (Predischarge)

27.4 Operational Modes

27.4.1 One-Shot Mode

In one-shot mode, the analog voltage applied to a selected pin is converted to a digital code once. Table 27.8 shows One-Shot Mode Specifications.

Table 27.8 One-Shot Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register, or bits ADEX1 to ADEX0 in the ADCON1 register are used to select a pin. The analog voltage applied to the pin is converted to a digital code once.
A/D conversion start conditions	• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts). • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger) input level at the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
A/D conversion stop conditions	• Completion of A/D conversion (if a software trigger is selected, the ADST bit becomes 0 (A/D conversion stop)). • Set the ADST bit to 0.
Interrupt request generation timing	Completion of A/D conversion.
Analog input pin	Select one pin from among AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, and ANEX1.
Reading of A/D conversion result	Read the register among AD0 to AD7 that corresponds to the selected pin.

27.4.1.1 A/D Control Register 0 (ADCON0) (In One-Shot Mode)

A/D Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
			0	0			

Symbol	Address	After Reset
ADCON0	03D6h	0000 0XXXb

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	b2 b1 b0 0 0 0 : AN0 0 0 1 : AN1 0 1 0 : AN2 0 1 1 : AN3 1 0 0 : AN4 1 0 1 : AN5 1 1 0 : AN6 1 1 1 : AN7	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 0 0 : One-shot mode	RW
MD1			RW
TRG	Trigger select bit	0 : Software trigger 1 : ADTRG trigger	RW
ADST	A/D conversion start flag	0 : A/D conversion stop 1 : A/D conversion start	RW
CKS0	Frequency select bit 0	Refer to the CKS0 bit in the ADCON0 register	RW

If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.

CH2-CH0 (analog input pin select bit) (b2-b0)

AN0_0 to AN0_7 and AN2_0 to AN2_7 can be used in the same way as AN0 to AN7. Use bits ADGSEL1 to ADGSEL0 in the ADCON2 register to select the desired group.

27.4.1.2 A/D Control Register 1 (ADCON1) (In One-Shot Mode)

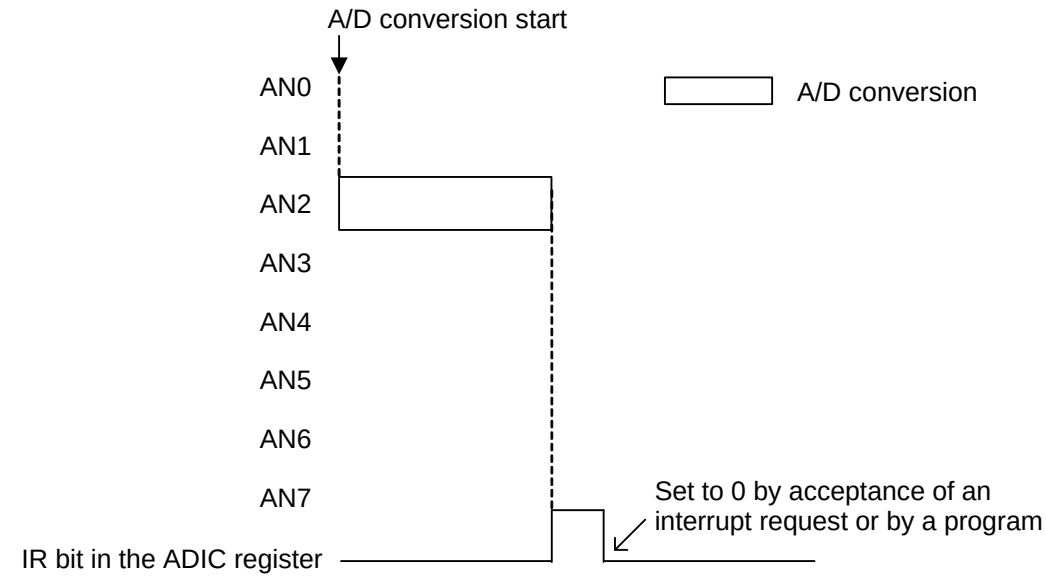
A/D Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
		1		X	0		

Symbol	Address	After Reset
ADCON1	03D7h	0000 X000b

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit	Invalid in one-shot mode	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	Set to 0 in one-shot mode.	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
CKS1	Frequency select bit 1	Refer to the CKS0 bit in the ADCON2 register	RW
ADSTBY	A/D standby bit	Set to 1 (A/D operation enabled)	RW
ADEX0	Extended pin select bit	b7 b6 0 0: ANEX0 and ANEX1 are not used 0 1: ANEX0 input is A/D converted 1 0: ANEX1 input is A/D converted 1 1: Do not set	RW
ADEX1			RW

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.



The above diagram applies under the following conditions:
- Bits CH2 to CH0 in the ADCON0 register are set to 010b (AN2).
- Bits ADGSEL1 to ADGSEL0 in the ADCON2 register are set to 00b (AN0 to AN7).

Figure 27.7 Operation Example in One-Shot Mode

27.4.2 Repeat Mode

In repeat mode, the analog voltage applied to a selected pin is repeatedly converted to a digital code. Table 27.9 lists Repeat Mode Specifications.

Table 27.9 Repeat Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register, or bits ADEX1 to ADEX0 in the ADCON1 register are used to select a pin. The analog voltage applied to the pin is repeatedly converted to a digital code.
A/D conversion start conditions	• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start). • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger) input level at the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
A/D conversion stop condition	Set the ADST bit to 0 (A/D conversion stop).
Interrupt request generation timing	No interrupt requests generated
Analog input pin	Select one pin from among AN0 to AN7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, and ANEX1.
Reading of A/D conversion result	Read the register among AD0 to AD7 that corresponds to the selected pin.

27.4.2.1 A/D Control Register 0 (ADCON0) (In Repeat Mode)

A/D Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
			0	1			

Symbol	Address	After Reset
ADCON0	03D6h	0000 0XXXb

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	b2 b1 b0 0 0 0: AN0 0 0 1: AN1 0 1 0: AN2 0 1 1: AN3 1 0 0: AN4 1 0 1: AN5 1 1 0: AN6 1 1 1: AN7	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 0 1: Repeat mode	RW
MD1			RW
TRG	Trigger select bit	0: Software trigger 1: ADTRG trigger	RW
ADST	A/D conversion start flag	0: A/D conversion stop 1: A/D conversion start	RW
CKS0	Frequency select bit 0	Refer to the CKS0 bit in the ADCON2 register	RW

If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.

CH2-CH0 (analog input pin select bit) (b2-b0)

AN0_0 to AN0_7 and AN2_0 to AN2_7 can be used in the same way as AN0 to AN7. Use bits ADGSEL1 to ADGSEL0 in the ADCON2 register to select the desired group.

27.4.2.2 A/D Control Register 1 (ADCON1) (In Repeat Mode)

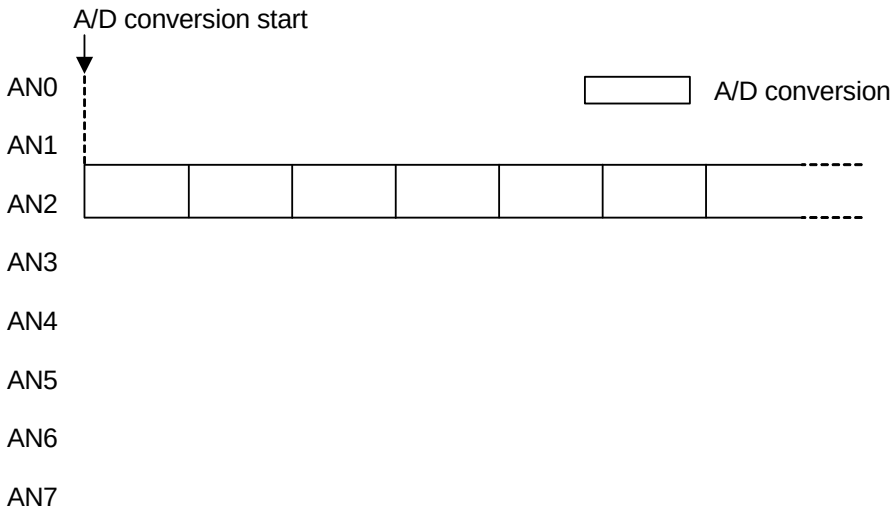
A/D Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
		1		X	0		

Symbol	Address	After Reset
ADCON1	03D7h	0000 X000b

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit	Invalid in repeat mode	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	Set to 0 in repeat mode.	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
CKS1	Frequency select bit 1	Refer to the CKS0 bit in the ADCON0 register	RW
ADSTBY	A/D standby bit	Set to 1 (A/D operation enabled)	RW
ADEX0	Extended pin select bit	b7 b6 0 0: ANEX0 and ANEX1 are not used 0 1: ANEX0 input is A/D converted 1 0: ANEX1 input is A/D converted 1 1: Do not set	RW
ADEX1			RW

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.



The above diagram applies under the following conditions.
- Bits CH2 to CH0 in the ADCON0 register are set to 010b (AN2).
- Bits ADGSEL1 to ADGSEL0 in the ADCON2 register are set to 00b (AN0 to AN7).

Figure 27.8 Operation Example in Repeat Mode

27.4.3 Single Sweep Mode

In single sweep mode, the analog voltage applied to selected pins is converted one-by-one to a digital code. Table 27.10 shows the Single Sweep Mode Specifications.

Table 27.10 Single Sweep Mode Specifications

Item	Specification
Function	Bits SCAN1 to SCAN0 in the ADCON1 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select pins. The analog voltage applied to the pins is converted one-by-one to a digital code.
A/D conversion start conditions	• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start). • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger) input level at the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
A/D conversion stop conditions	• Completion of A/D conversion (if a software trigger is selected, the ADST bit is set to 0 (A/D conversion stop)). • Set the ADST bit to 0.
Interrupt request generation timing	Completion of A/D conversion
Analog input pin	Select from AN0 and AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), and AN0 to AN7 (8 pins). AN0_0 to AN0_7 and AN2_0 to AN2_7 can be selected in the same way.
Reading of A/D conversion result	Read the registers among AD0 to AD7 that corresponds to the selected pin.

27.4.3.1 A/D Control Register 0 (ADCON0) (In Single Sweep Mode)

A/D Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
			1	0			

Symbol: ADCON0 — Address: 03D6h — After Reset: 0000 0XXXb

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Invalid in single sweep mode	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 1 0 : Single sweep mode	RW
MD1			RW
TRG	Trigger select bit	0 : Software trigger 1 : $\overline{\text{ADTRG}}$ trigger	RW
ADST	A/D conversion start flag	0 : A/D conversion stop 1 : A/D conversion start	RW
CKS0	Frequency select bit 0	Refer to the CKS0 bit in the ADCON0 register	RW

If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.

27.4.3.2 A/D Control Register 1 (ADCON1) (In Single Sweep Mode)

A/D Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
		1		X	0		

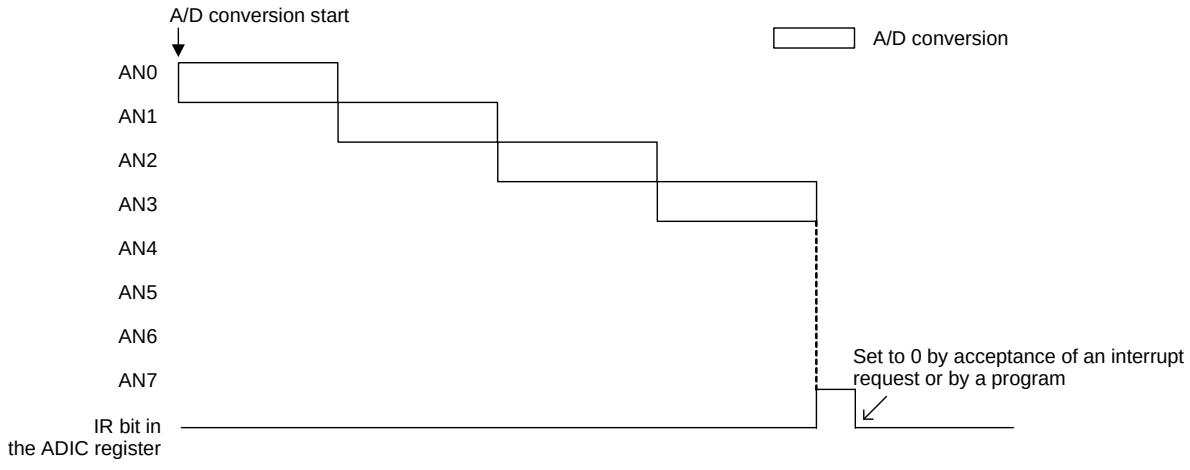
Symbol	Address	After Reset
ADCON1	03D7h	0000 X000b

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit	When single sweep mode is selected b1 b0 0 0: AN0 to AN1 (2 pins) 0 1: AN0 to AN3 (4 pins) 1 0: AN0 to AN5 (6 pins) 1 1: AN0 to AN7 (8 pins)	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	Set to 0 in single sweep mode.	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
CKS1	Frequency select bit 1	Refer to the CKS0 bit in the ADCON0 register	RW
ADSTBY	A/D standby bit	Set to 1 (A/D operation enabled)	RW
ADEX0	Extended pin select bit	b7 b6 0 0: ANEX0 and ANEX1 are not used 0 1: Do not set 1 0: Do not set 1 1: Do not set	RW
ADEX1			RW

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

SCAN1-SCAN0 (A/D sweep pin select bit) (b1-b0)

AN0_0 to AN0_7 and AN2_0 to AN2_7 can be used in the same way as AN0 to AN7. Use bits ADGSEL1 to ADGSEL0 in the ADCON2 register to select the desired group.



The above diagram applies under the following conditions:
- Bits SCAN1 to SCAN0 in the ADCON1 register are set to 01b (AN0 to AN3 (4 pins)).
- Bits ADGSEL1 to ADGSEL0 in the ADCON2 register are set to00b (AN0 to AN7).

Figure 27.9 Operation Example in Single Sweep Mode

27.4.4 Repeat Sweep Mode 0

In repeat sweep mode 0, the analog voltage applied to selected pins is repeatedly converted to a digital code. Table 27.11 shows the Repeat Sweep Mode 0 Specifications.

Table 27.11 Repeat Sweep Mode 0 Specifications

Item	Specification
Function	Bits SCAN1 to SCAN0 in the ADCON1 register and bits ADGSEL1 to ADGSEL0 in the ADCON2 register are used to select pins. Analog voltage applied to the pins is repeatedly converted to a digital code.
A/D conversion start conditions	• When the TRG bit in the ADCON0 register is 0 (software trigger) the ADST bit in the ADCON0 register is set to 1 (A/D conversion start). • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger) input level at the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
A/D conversion stop condition	Set the ADST bit to 0 (A/D conversion stop).
Interrupt request generation timing	No interrupt requests generated
Analog input pin	Select from AN0 and AN1 (2 pins), AN0 to AN3 (4 pins), AN0 to AN5 (6 pins), and AN0 to AN7 (8 pins)· AN0_0 to AN0_7 and AN2_0 to AN2_7 can be selected in the same way.
Reading of A/D conversion result	Read the registers among AD0 to AD7 that corresponds to the selected pins.

27.4.4.1 A/D Control Register 0 (ADCON0) (In Repeat Sweep Mode 0)

A/D Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
			1	1			

Symbol	Address	After Reset
ADCON0	03D6h	0000 0XXXb

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Invalid in repeat sweep mode 0	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 1 1 : Repeat sweep mode 0 or repeat sweep mode 1	RW
MD1			RW
TRG	Trigger select bit	0 : Software trigger 1 : $\overline{\text{ADTRG}}$ trigger	RW
ADST	A/D conversion start flag	0 : A/D conversion stop 1 : A/D conversion start	RW
CKS0	Frequency select bit 0	Refer to the CKS0 bit in the ADCON0 register	RW

If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.

27.4.4.2 A/D Control Register 1 (ADCON1) (In Repeat Sweep Mode 0)

A/D Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
		1		X	0		

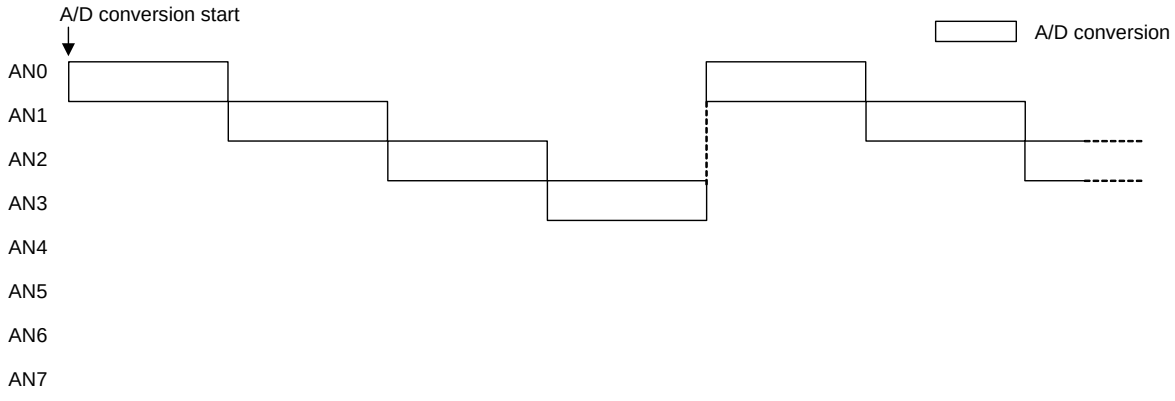
Symbol	Address	After Reset
ADCON1	03D7h	0000 X000b

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit	When repeat sweep mode 0 is selected b1 b0 0 0: AN0 to AN1 (2 pins) 0 1: AN0 to AN3 (4 pins) 1 0: AN0 to AN5 (6 pins) 1 1: AN0 to AN7 (8 pins)	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	Set to 0 in repeat sweep mode 0	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
CKS1	Frequency select bit 1	Refer to the CKS0 bit in the ADCON0 register	RW
ADSTBY	A/D standby bit	Set to 1 (A/D operation enabled)	RW
ADEX0	Extension pin select bit	b7 b6 0 0: ANEX0 and ANEX1 are not used 0 1: Do not set 1 0: Do not set 1 1: Do not set	RW
ADEX1			RW

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

SCAN1-SCAN0 (A/D sweep pin select bit) (b1-b0)

AN0_0 to AN0_7 and AN2_0 to AN2_7 can be used in the same way as AN0 to AN7. Use bits ADGSEL1 to ADGSEL0 in the ADCON2 register to select the desired group.



The above diagram applies under the following conditions:
- Bits SCAN1 to SCAN0 in the ADCON1 are set to 01b (AN0 to AN3 (4 pins)).
- Bits ADGSEL1 to ADGSEL0 in the ADCON2 are set to 00b (AN0 to AN7).

Figure 27.10 Operation Example in Repeat Sweep Mode 0

27.4.5 Repeat Sweep Mode 1

In repeat sweep mode 1, the analog voltage applied to eight selected pins including some prioritized pins is repeatedly converted to a digital code. Table 27.12 lists the Repeat Sweep Mode 1 Specifications.

Table 27.12 Repeat Sweep Mode 1 Specifications

Item	Specification
Function	The input voltage of all eight pins selected by bits ADGSEL1 to ADGSEL0 in the ADCON2 register is repeatedly converted to a digital code. One to four pins selected by SCAN1 to SCAN0 in the ADCON1 register is/are converted by priority. Example: If AN0 is prioritized, input voltage is converted to a digital code in the following order: AN0→AN1→AN0→AN2→AN0→AN3 •••
A/D conversion start conditions	• When the TRG bit in the ADCON0 register is 0 (software trigger), the ADST bit in the ADCON0 register is set to 1 (A/D conversion start). • When the TRG bit is 1 ($\overline{\text{ADTRG}}$ trigger), input level at the $\overline{\text{ADTRG}}$ pin changes from high to low after the ADST bit is set to 1 (A/D conversion start).
A/D conversion stop condition	Set the ADST bit to 0 (A/D conversion stop).
Interrupt request generation timing	No interrupt requests generated
Analog input pins to be given priority when A/D converted	Select from AN0 (1 pin), AN0 and AN1 (2 pins), AN0 to AN2 (3 pins), and AN0 to AN3 (4 pins). AN0_0 to AN0_3 and AN2_0 to AN2_3 can be selected in the same way.
Reading of A/D conversion result	Read the registers among AD0 to AD7 that corresponds to the selected pins.

27.4.5.1 A/D Control Register 0 (ADCON0) (In Repeat Sweep Mode 1)

A/D Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
			1	1			

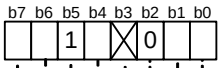
Symbol	Address	After Reset
ADCON0	03D6h	0000 0XXXb

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Invalid in repeat sweep mode 1	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 1 1 : Repeat sweep mode 0 or repeat sweep mode 1	RW
MD1			RW
TRG	Trigger select bit	0 : Software trigger 1 : $\overline{\text{ADTRG}}$ trigger	RW
ADST	A/D conversion start flag	0 : A/D conversion stop 1 : A/D conversion start	RW
CKS0	Frequency select bit 0	Refer to the CKS0 bit in the ADCON0 register	RW

If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.

27.4.5.2 A/D Control Register 1 (ADCON1) (In Repeat Sweep Mode 1)

A/D Control Register 1



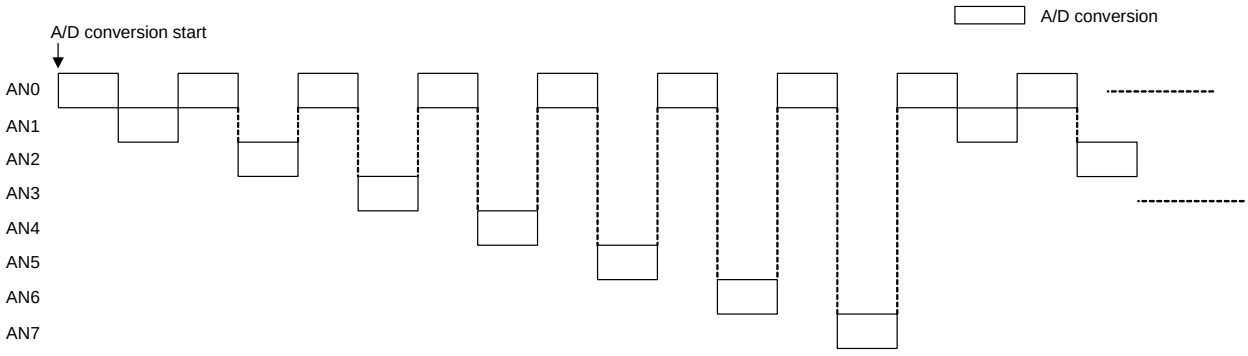
Symbol	Address	After Reset
ADCON1	03D7h	0000 X000b

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit	When repeat sweep mode 1 is selected b1 b0 0 0: AN0 (1 pin) 0 1: AN0 to AN1 (2 pins) 1 0: AN0 to AN2 (3 pins) 1 1: AN0 to AN3 (4 pins)	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	1 : Repeat sweep mode 1	RW
— (b3)	No register bit. If necessary, set to 0. Read as undefined value		—
CKS1	Frequency select bit 1	Refer to the CKS0 bit in the ADCON0 register	RW
ADSTBY	A/D standby bit	Set to 1 (A/D operation enabled)	RW
ADEX0	Extended pin select bit	b7 b6 0 0: ANEX0 and ANEX1 are not used 0 1: Do not set 1 0: Do not set 1 1: Do not set	RW
ADEX1			RW

If the ADCON0 register is rewritten during A/D conversion, the conversion result is undefined.

SCAN1-SCAN0 (A/D sweep pin select bit) (b1-b0)

AN0_0 to AN0_7 and AN2_0 to AN2_7 can be used in the same way as AN0 to AN7. Use bits ADGSEL1 to ADGSEL0 in the ADCON2 register to select the desired group.



The above diagram applies under the following conditions.
- Bits SCAN1 to SCAN0 in the ADCON1 register are set to 00b (AN0 (one pin)).
- Bits ADGSEL1 to ADGSEL0 in the ADCON2 register are set to 00b (A0 to AN7).

Figure 27.11 Operation Example in Repeat Sweep Mode

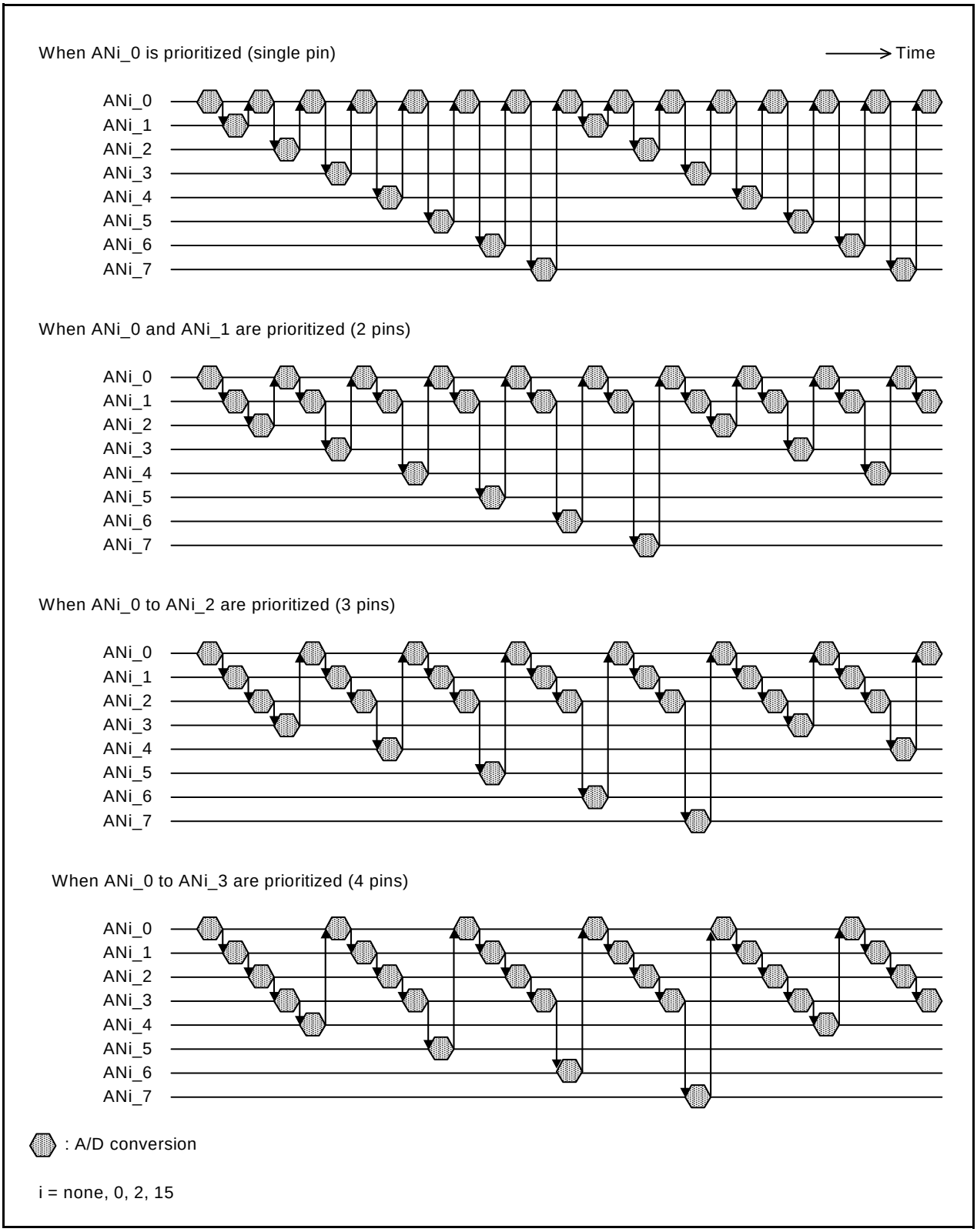


Figure 27.12 Transition Diagram of Pins Used in A/D Conversion in Repeat Sweep Mode 1

27.5 External Sensor

Figure 27.13 shows Analog Input Pin and External Sensor Equivalent Circuit. R_1 in Figure 27.13 is obtained by the following formulas.

$$I_2 = \frac{C_2(E_x - V_{samp})}{C_{in} \times R_1 + C_2(R_1 + R_2)} \exp\left[\frac{-t_{samp}}{C_{in} \times R_1 + C_2(R_1 + R_2)}\right]$$

Time required to charge C_2:

Sampling time $-t_{samp} > C_{in} \times R_1 + C_2(R_1 + R_2)$

$$R1 < \frac{t_{samp} - C_2 \times R_2}{C_{in} + C_2} \qquad t_{samp} = \frac{15}{\phi AD}$$

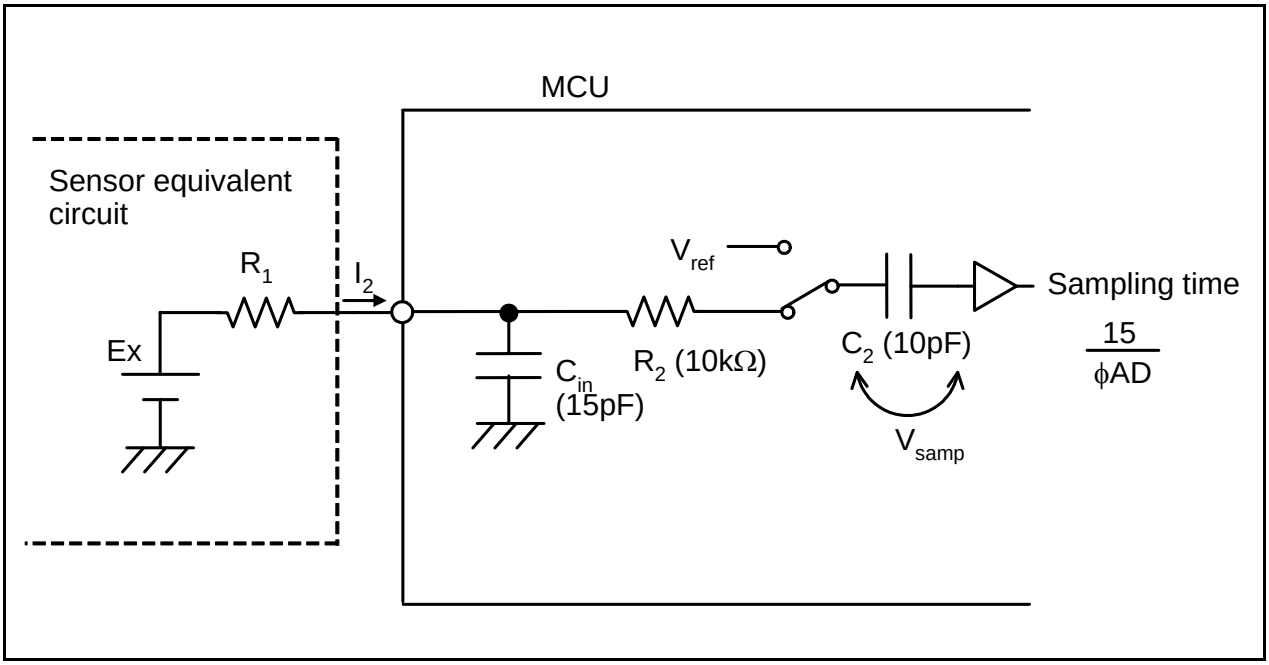


Figure 27.13 Analog Input Pin and External Sensor Equivalent Circuit

C_{in} : Input pin capacity
C_2 : Sampling capacity
R_1 : Sensor output resistance
R_2 : Selector resistance
E_x : Sensor output voltage
V_{samp} : Sampled voltage
V_{ref} : A/D converter reference voltage

When capacitor C_1 is connected, C_1 is obtained by the following formulas. Figure 27.14 shows Analog Input Pin and External Sensor Equivalent Circuit (Capacitor is Connected).
If R_1 is infinite, C_2 is charged from C_1.
When the difference of voltages generated by divided capacitor, C_1 and C_2 is V_P:

$$V_P = \frac{C_2}{C_1 + C_2} \times (E_x - V_{samp}) \ldots (1)$$

When the difference generated by the conversion is V_{p1}:

$$V_P = V_{P1} \times \frac{1}{2^i} < \frac{VREF}{A \times 2^x} \ldots (2)$$

X = 10 (bits)

A: $V_{P1} = \frac{1}{A}$ LSB (e.g. when V_{P1} = 0.1 LSB, A = 10)

From (1) and (2)

$$C_1 = C_2 \times \left(\frac{E_x - V_2}{V_{P1}} - 1 \right) \ldots (3)$$

$$\therefore C_1 > C_2 \left(A \times 2^x \frac{1}{2^i} - 1 \right) \ldots (4)$$

In 10-bit resolution A/D converter, C_1 is 0.21 μF or more when C_2 = 10 pF.

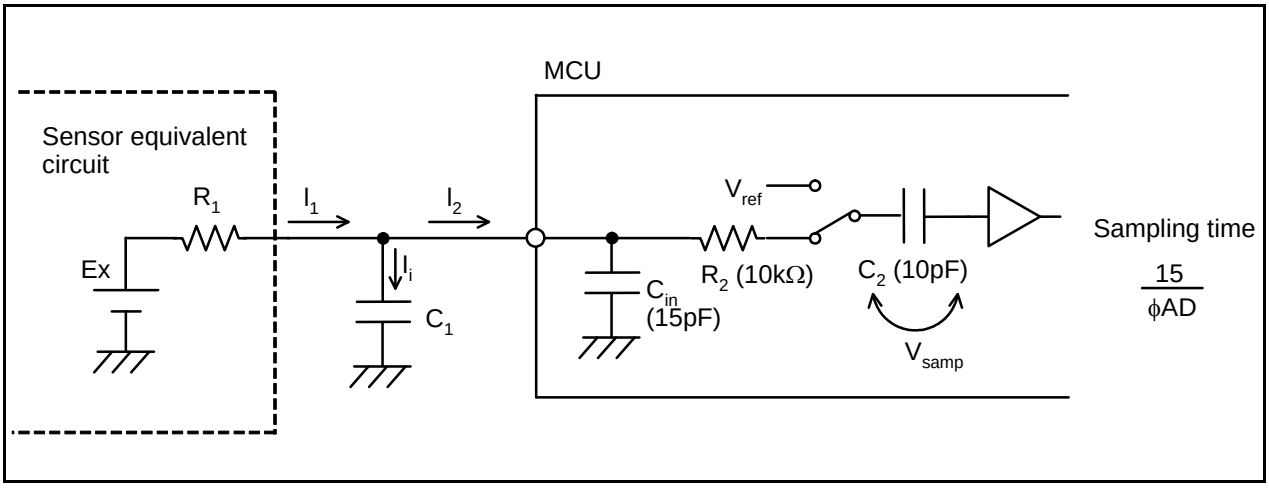


Figure 27.14 Analog Input Pin and External Sensor Equivalent Circuit (Capacitor is Connected)

C_1 : Board parasitic capacitance
C_{in} : Input pin capacity
C_2 : Sampling capacity
R_1 : Sensor output resistance
R_2 : Selector resistance
E_x : Sensor output voltage
V_{samp} : Sampled voltage
V_{ref} : A/D converter reference voltage

27.6 Interrupt

Refer to the operation examples for timing of generating interrupt requests.
Also, refer to 14.7 “Interrupt Control” for details. Table 27.13 lists Registers Associated with A/D Converter Interrupt.

Table 27.13 Registers Associated with A/D Converter Interrupt

Address	Register Name	Register Symbol	After Reset
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b

27.7 Notes on A/D Converter

27.7.1 Analog Input Pin

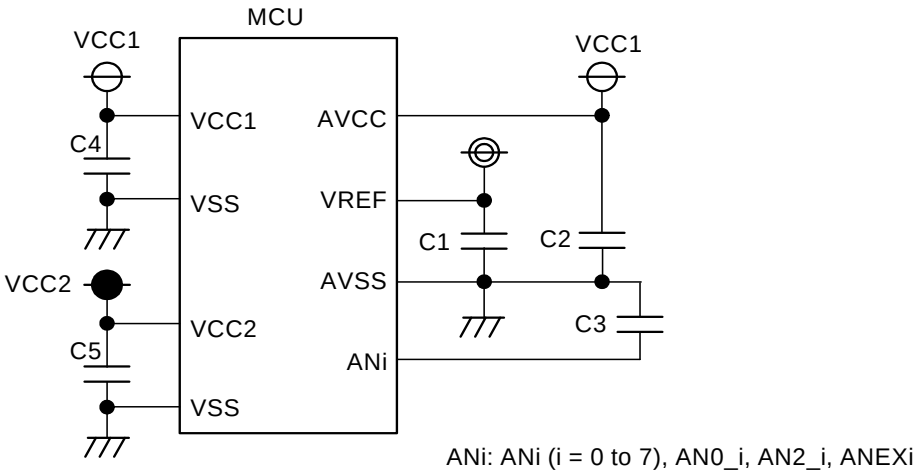
When VCC1 ≥ VCC2, set analog input voltage as follows:
analog input voltage (AN_0 to AN_7, ANEX0, and ANEX1) ≤ VCC1
analog input voltage (AN0_0 to AN0_7 and AN2_7 to AN2_7) ≤ VCC2
Do not use any of four pins AN4 to AN7 as analog input pins if a key input interrupt is to be used (key input interrupt request is generated when analog input voltage becomes low level).

27.7.2 ϕAD Frequency

Set ϕAD to 2 MHz or more, but an upper limit is set as follows:
4.0 ≤ VCC1 ≤ 5.5V: ϕAD ≤ 25 MHz
3.2 ≤ VCC1 ≤ 4.0V: ϕAD ≤ 16 MHz
3.0 ≤ VCC1 ≤ 3.2V: ϕAD ≤ 10 MHz

27.7.3 Pin Configuration

Three capacitors should be respectively put between pins AVCC, VREF, analog input (ANi (i = 0 to 7), ANEXi, AN0_i, and AN2_i) and the AVSS pin to protect from error operations caused by noise, latchup, or to reduce conversion errors. Also, a capacitor between the VCC1 pin and the VSS pin. Figure 27.15 shows Example of Pin Configuration.



Notes:
1.C1 ≥ 0.1 μF, C2 ≥ 0.1 μF, C3 ≥ 100pF, C4 ≥ 0.1 μF, C5 ≥ 0.1 μF (reference values).
2.The traces for the capacitor and MCU should be short and wide as much as physically possible.

Figure 27.15 Example of Pin Configuration

27.7.4 Register Access

Set registers ADCON0 (exclude bit 6), ADCON1, and ADCON2 when A/D conversion stops (before trigger is generated).
Set the ADSTBY bit which is 1 to 0 after A/D conversion stops.

27.7.5 A/D Conversion Start

If the ADSTBY bit in the ADCON1 is changed from 0 (A/D operation stopped) to 1 (A/D operation enabled), wait for 1 ϕA/D cycle or more before starting A/D conversion.

27.7.6 A/D Operation Mode Change

When A/D operation mode has been changed, re-select analog input pins by using bits CH2 to CH0 in the ADCON0 register or bits SCAN1 to SCAN0 in the ADCON1 register.

27.7.7 State When Forcibly Terminated

If A/D conversion in progress is halted by setting the ADST bit in the ADCON0 register to 0, the conversion result is undefined. In addition to that, the unconverted ADi register may also become undefined. Do not use any ADi registers when setting the ADST bit to 0 by a program during A/D conversion.

27.7.8 A/D Open-Circuit Detection Assist Function

The conversion result in open-circuit depends on the external circuit. Use this function only after careful evaluation for the system. Do not use this function when VCC1 > VCC2.

When A/D conversion starts after changing the AINRST register, follow these procedures:

(1) Change bits AINRST1 to AINRST0 in the AINRST register.
(2) Wait for one cycle of ϕAD.
(3) Set the ADST bit in the ADCON0 register to 1 (A/D conversion start).

27.7.9 Detection of Completion of A/D Conversion

In one-shot mode and single sweep mode, use the IR bit in the ADIC register to detect completion of A/D conversion. When not using interrupt, set the IR bit to 0 by a program after the detection.

When 1 is written to the ADST bit in the ADCON0 register, the ADST bit becomes 1 (A/D conversion start) after start processing time (refer to Table 27.7 “Cycles of A/D Conversion Item”) elapses. When reading the ADST bit shortly after writing 1, 0 (A/D conversion stop) may be read.

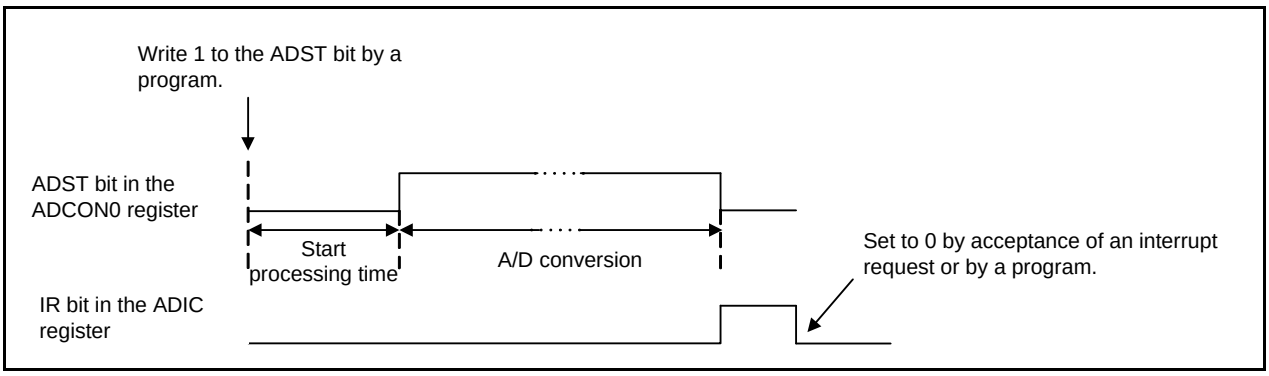


Figure 27.16 ADST Bit Operation

27.7.10 Register Settings

Set the CKS3 bit, and then set other A/D converter related registers. Also, after changing the CKS3 bit, set the A/D converter related registers again. Note that bits in the ADCON2 register and the CKS3 bit can be set simultaneously.

28. D/A Converter

28.1 Introduction

The D/A converter consists of two independent 8-bit R-2R type D/A converters.
Table 28.1 lists D/A Converter Specifications and Figure 28.1 shows D/A Converter Block Diagram.

Table 28.1 D/A Converter Specifications

Item	Specification
D/A conversion method	R-2R
Resolution	8 bits

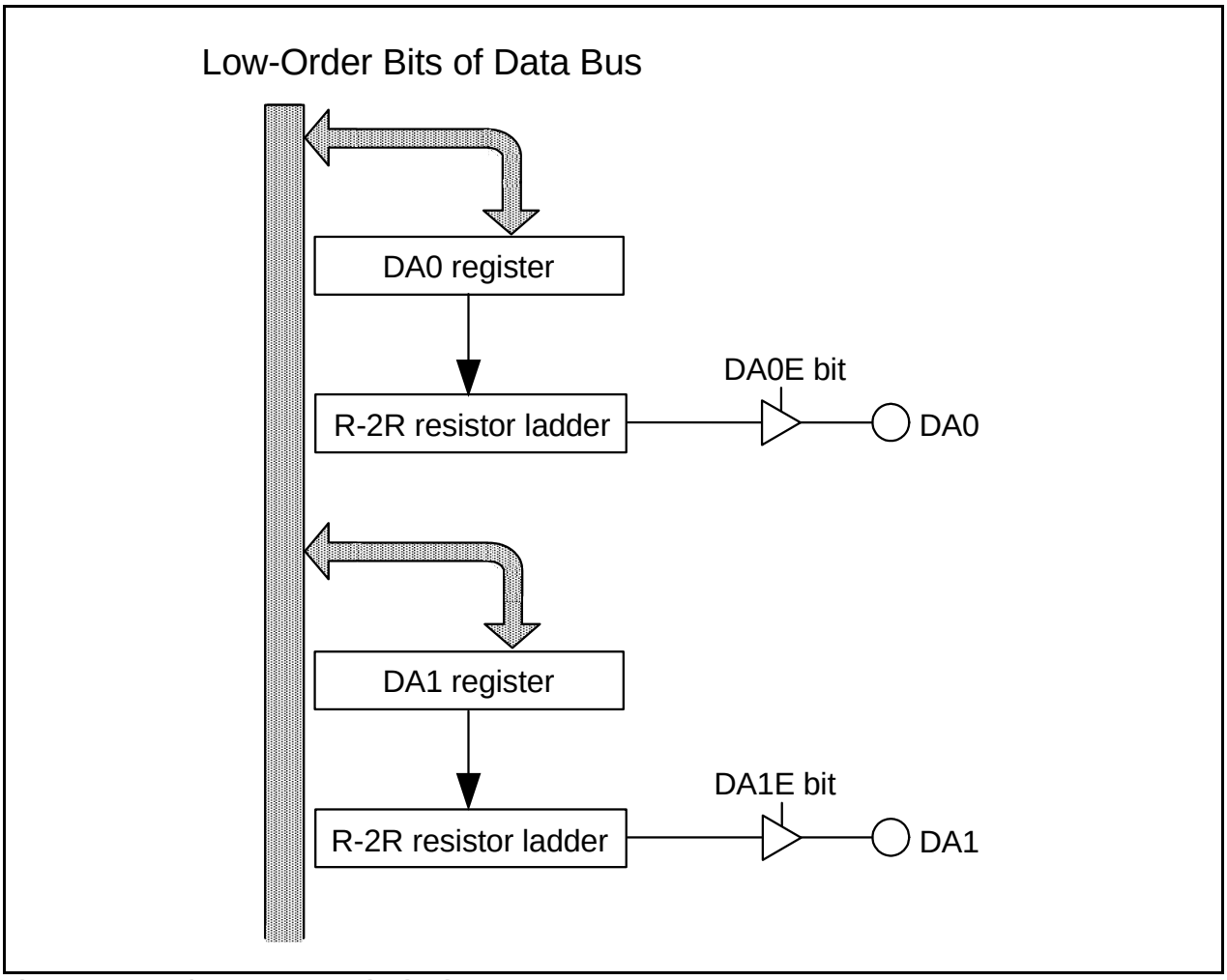


Figure 28.1 D/A Converter Block Diagram

Table 28.2 Input Pin

Pin Name	Input/Output	Function
DA0	Output (1)	D/A comparator output
DA1		

Note:
1. Set the direction bit of the ports sharing a pin to 0 (input mode). When the DAiE bit is se to 1, the corresponding port cannot be pulled up.

28.2 Registers

Table 28.3 Register Structure

Address	Register Name	Register Symbol	After Reset
03D8h	D/A0 Register	DA0	00h
03DAh	D/A1 Register	DA1	00h
03DCh	D/A Control Register	DACON	00h

28.2.1 D/Ai Register (DAi) (i = 0 to 1)

D/Ai Register (i = 0 to 1)

b7 b0

Symbol	Address	After Reset
DA0	03D8h	00h
DA1	03DAh	00h

Function	Setting Range	RW
Output value of D/A conversion	00h to FFh	RW

28.2.2 D/A Control Register (DACON)

D/A Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
DACON	03DCh	00h

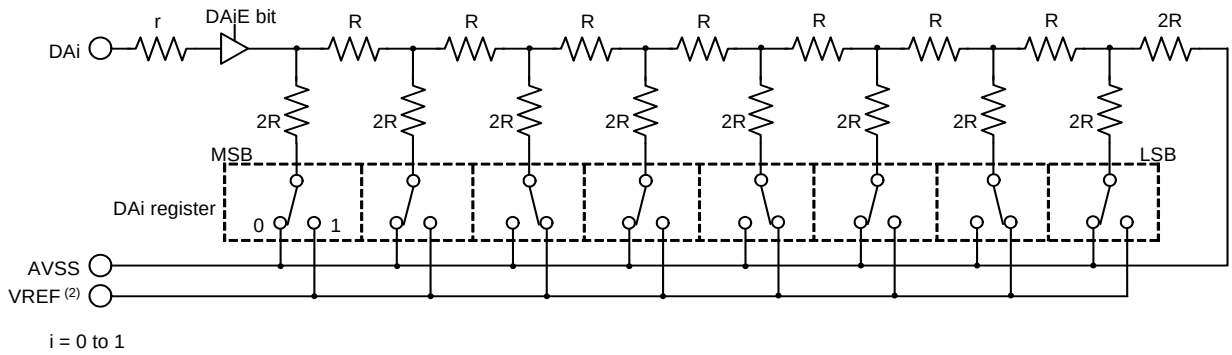
Bit Symbol	Bit Name	Function	RW
DA0E	D/A 0 output enable bit	0 : Output disabled 1 : Output enabled	RW
DA1E	D/A 1 output enable bit	0 : Output disabled 1 : Output enabled	RW
— (b7-b2)	No register bits. If necessary, set to 0. Read as 0		—

28.3 Operations

D/A conversion is performed by writing a value to the DAi register (i = 0 to 1).
Output analog voltage (V) is determined by the value n (n = decimal) set in the DAi register.

$$V = VREF \times \frac{n}{256} \quad (n = 0 \text{ to } 255)$$

VREF: Reference voltage
Figure 28.2 shows D/A Converter Equivalent Circuit.



Notes:
1. The above diagram applies when the DAi register is set to 2Ah.
2. VREF is not related to the ADSTBY bit in the ADCON1 register.

Figure 28.2 D/A Converter Equivalent Circuit

28.4 Notes on D/A Converter

28.4.1 Not Using D/A Converter

When the D/A converter is not used, set the DAiE bit (i = 0 to 1) to 0 (output disabled) and the DAi register to 00h in order to minimize unnecessary current consumption and prevent the flow of a current to R-2R resistor.

29. CRC Calculator

29.1 Introduction

The CRC (Cyclic Redundancy Check) calculator detects errors in data blocks. This CRC calculator is enhanced by additional feature, CRC snoop, in order to monitor reads from and writes to a certain SFR address, and perform CRC calculations automatically on the data read from and data written to the aforementioned SFR address. Figure 29.1 shows CRC Calculator Block Diagram. Figure 29.2 shows CRC Operation (CRC-CCITT).

Table 29.1 CRC Calculator Specification

Item	Specification
Operation polynomial	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) or CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
Selectable function	• MSB/LSB selectable • CRC snoop

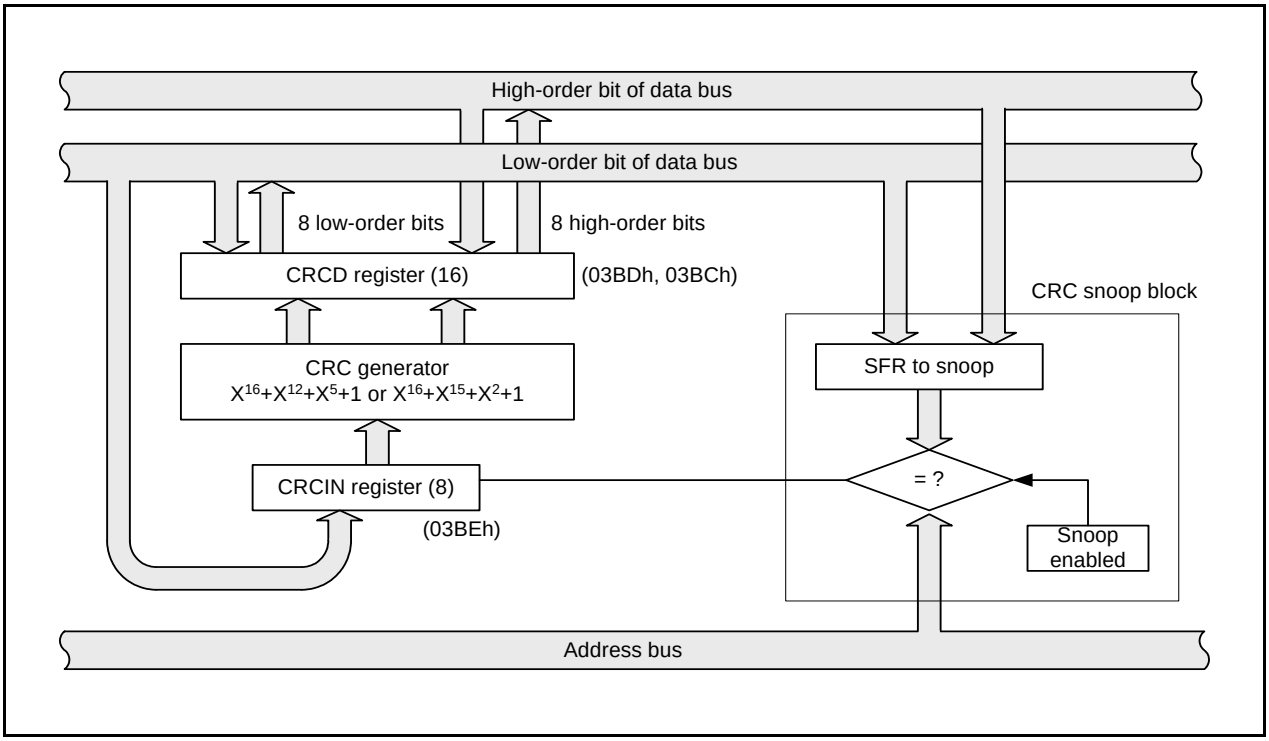


Figure 29.1 CRC Calculator Block Diagram

29.2 Registers

Table 29.2 Register Structure

Address	Register Name	Symbol	After Reset
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh

29.2.1 CRC Data Register (CRCD)

CRC Data Register

(b15) (b8)
b7 b0 b7 b0

Symbol	Address	After Reset
CRCD	03BDh to 03BCh	Undefined

Function	Setting Range	RW
When data is written to the CRCIN register after setting the initial value in the CRCD register, the CRC can be read out from this register.	0000h to FFFFh	RW

29.2.2 CRC Input Register (CRCIN)

CRC Input Register

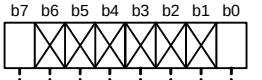
b7 b0

Symbol	Address	After Reset
CRCIN	03BEh	Undefined

Function	Setting Range	RW
Data input	00h to FFh	RW

29.2.3 CRC Mode Register (CRCMR)

CRC Mode Register

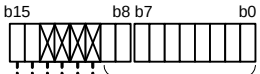


Symbol: CRCMR | Address: 03B6h | After Reset: 0XXX XXX0b

Bit Symbol	Bit Name	Function	RW
CRCPS	CRC polynomial select bit	0: $X^{16}+X^{12}+X^{5}+1$ (CRC-CCITT) 1: $X^{16}+X^{15}+X^{2}+1$ (CRC-16)	RW
— (b6-b1)	No register bits. If necessary, set to 0. Read as undefined value		—
CRCMS	CRC mode select bit	0: LSB first 1: MSB first	RW

29.2.4 SFR Snoop Address Register (CRCSAR)

SFR Snoop Address Register



Symbol: CRCSAR | Address: 03B5 to 03B4h | After Reset: 00XX XXXX XXXX XXXXb

Bit Symbol	Bit Name	Function	RW
CRCSAR9 to CRCSAR0	SFR snoop address bit	Set the SFR address to snoop	RW
— (b13-b10)	No register bits. If necessary, set to 0. Read as undefined value.		—
CRCSR	Snoop-on-read enable bit	0: Disabled 1: Enabled	RW
CRCSW	Snoop-on-write enable bit	0: Disabled 1: Enabled	RW

CRCSR (CRC Snoop On Read Enable Bit) (b14)

Do not set bits CRCSR and CRCSW to 1 simultaneously. When the CRCSW bit is set to 1, set the CRCSR bit to 0.

CRCSW (Snoop On Write Enable Bit) (b15)

Do not set bits CRCSR and CRCSW to 1 simultaneously. When the CRCSR bit is set to 1, set the CRCSW bit to 0.

29.3 Operations

29.3.1 Basic Operation

The CRC (Cyclic Redundancy Check) calculation detects an error in data blocks. The MCU uses two generator polynomials of CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) and CRC-16 ($X^{16} + X^{15} + X^2 + 1$) to generate CRC.
The CRC is 16-bit code generated for a given length of a data block in 8 bits unit. After setting the default value in the CRCD register, the CRC is stored in the CRCD register every time one-byte of data is written to the CRCIN register. CRC generation for one-byte data is completed in two CPU clock cycles.

29.3.2 CRC Snoop

CRC snoop monitors reads from and writes to a certain SFR address and performs CRC calculation on the data read from and written to the aforementioned SFR address automatically. Because CRC snoop recognizes writes to and reads from a certain SFR address as a trigger to perform CRC calculation automatically, there is no need to write data to the CRCIN register. All SFR addresses from 0020h to 03FFh are subject to the CRC snoop. The CRC snoop is useful to monitor writes to the UART TX buffer, and reads from the UART RX buffer.

To use this function, write a target SFR address to bits CRCSAR9 to CRCSAR0 in the CRCSAR register. Then, set the CRCSW bit in the CRCSAR register to 1 to enable snooping on writes to the target or the CRCSR bit in the CRCSAR register to 1 to enable snooping on reads from the target.

When setting the CRCSW bit to 1, and writing data to a target SFR address by CPU or DMA, CRC calculator stores the data into the CRCIN register and performs CRC calculation. Similarly, when setting the CRCSR bit to 1, and reading data in a target SFR address by CPU or DMA, CRC calculator stores the data into the CRCIN register and performs CRC calculation.

The CRC calculation is performed on one-byte at a time. When the target SFR address is accessed in word (16 bits), CRC is generated on the lower byte (one byte) of data.

CRC calculation and setting procedure to generate CRC, 80C4h, with CRC-CCITT (LSB first selected)

- CRC operation specification

CRC: remainder of a division, $\frac{\text{inverted value of the CRCIN register}}{\text{generator polynomial}}$

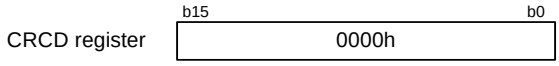
Generator polynomial: $X^{16} + X^{12} + X^5 + 1$ (1 0001 0000 0010 0001b)

- Setting procedures

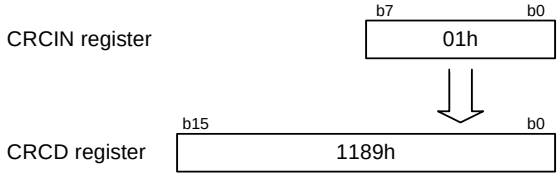
(1) Reverse the bit position of the value 80C4h by a program in 1-byte units.

80h → 01h, C4h→23h

(1) Write 0000h (initial value) to the CRCD register

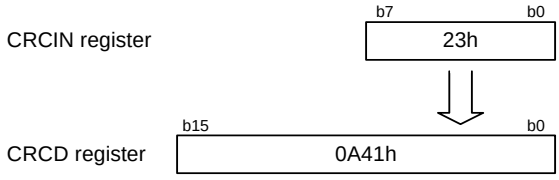


(2) Write 01h (reversed value of 80h) to the CRCIN register



After two cycles, "1189h", which is a bit-position-reverse value of "9188h" (CRC for "80h") is stored in the CRCD register.

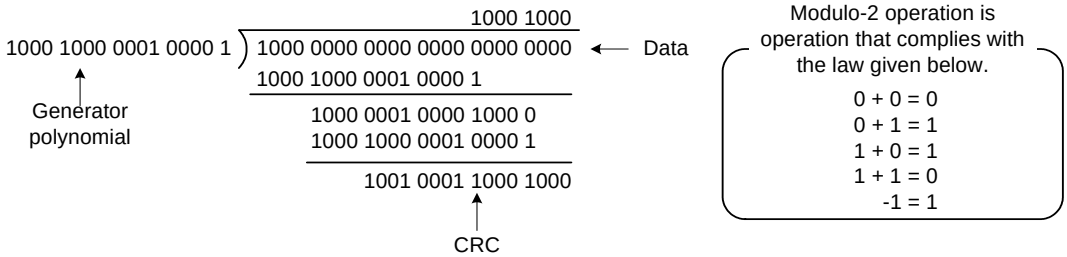
(3) Write 23h (reversed value of C4h) to the CRCIN register



After two cycles, "0A41h", which is a bit-position-reverse value of "8250h" (CRC for "80C4h") is stored in the CRCD register.

- Details on CRC calculation

As shown in (3) above, bit position of 01h (0000 0001b) written to the CRCIN register is reversed and becomes 80h (1000 0000b). Add 1000 0000 0000 0000 0000 0000b, as 1000 0000b plus 16 digits, to 0000 0000 0000 0000 0000 0000b, as 0000 0000 0000 0000b plus 8 digits as the default value of the CRCD register to perform the modulo-2 division.



0001 0001 1000 1001b (1189h), the remainder 1001 0001 1000 1000b (9188h) with inversed bit position, can be read from the CRCD register.

When going on to (4) above, 23h(0010 0011b) written in the CRCIN register is inversed and becomes C4h (1100 0100b). Add 1100 0100 0000 0000 0000 0000b, as 1100 0100b plus 16 digits, to 1001 0001 1000 1000 0000 0000b, as 1001 0001 1000 1000b plus 8 digits as a remainder of (3) left in the CRCD register to perform the modulo-2 division. 0000 1010 0100 0001b (0A41h), the remainder 1000 0010 0101 0000b (8250h) with inversed bit position, can be read from the CRCD register.

Figure 29.2 CRC Operation (CRC-CCITT)

CRC calculation and setting procedure to generate CRC, 80C4h with CRC-16 (MSB first selected)

- CRC operation specification

  CRC: remainder of a division, $\frac{\text{the CRCIN register}}{\text{generator polynomial}}$

  Generator polynomial: $X^{16} + X^{15} + X^2 + 1$(1 1000 0000 0000 0101b)

- Setting procedures

  (1) Write 0000h (initial value) to the CRCD register

  CRCD register: b15 … b0 = 0000h

  (2) Write 80h to the CRCIN register

  CRCIN register: b7 … b0 = 80h

  ⇓ After two cycles, "8303h" (CRC for 80h) is stored into the CRCD register.

  CRCD register: b15 … b0 = 8303h

  (3) Write C4h to the CRCIN register

  CRCIN register: b7 … b0 = C4h

  ⇓ After two cycles, "0292h" (CRC for 80C4h) is stored into the CRCD register.

  CRCD register: b15 … b0 = 0292h

- Details on CRC calculation

  As shown in (2) above, add 1000 0000 0000 0000 0000 0000b, as 80h (1000 0000b) written in the CRCIN register plus 16 digits, to 0000 0000 0000 0000 0000 0000b, as 0000 0000 0000 0000b plus 8 digits as the default value of the CRCD register. Perform the modulo-2 division on the result. The remainder, 1000 0011 0000 0011b (8303h) can be read from the CRCD register.

  When going on to (3) above, add 1100 0100 0000 0000 0000 0000b, as C4h (1100 0100b) written in the CRCIN register plus 16 digits, to 1000 0011 0000 0011 0000 0000b, as 8303h (1000 0011 0000 0011b) plus 8 digits as a remainder of (2) left in the CRCD register to perform the modulo-2 division.
  The remainder, 0000 0010 1001 0010b (0292h) can be read from the CRCD register.

Figure 29.3 CRC Operation (CRC-16)

30. Flash Memory

Note

P1, P4_4 to P4_7, P7_2 to P7_5, P9_1 of the 80-pin package have no external connections. There are no P11 to P14 in the 80-pin and 100-pin packages. For the 80-pin and 100-pin packages, do not use these pins for the entry of user boot function.

30.1 Introduction

Flash memory is used as ROM in this product. The flash memory in this chapter indicates the flash memory inside a microcomputer.
In this product, the flash memory can perform in three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.
Table 30.1 lists Flash Memory Specifications (see to Table 1.1 to Table 1.6 “Specifications” for the items not listed in Table 30.1.

Table 30.1 Flash Memory Specifications

Item		Specification
Flash memory rewrite mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Erase block	Program ROM 1	See Figure 30.1 “Flash Memory Block Diagram”.
	Program ROM 2	1 block (16 Kbytes)
	Data flash	2 blocks (4 Kbytes each)
Program method		In units of 2 words
Erase method		Block erase
Program and erase control method		Program and erase controlled by software command
Suspend function (under review)		Program suspend and erase suspend
Protect method		A lock bit protects each block
Number of commands		8 commands
Program and erase cycles	Program ROM 1 and program ROM 2	1,000 times (1)
	Data flash	10,000 times (1)
Data retention		20 years
Flash memory rewrite disable function		Parallel I/O mode ROM code protect function Standard serial I/O mode ID code check function, forced erase function, and standard serial I/O mode disable function
User boot function		User boot mode

Note:
1. Definition of program and erase cycles
The program and erase cycles is the number of erase operations performed on a per-block basis. For example, assume a case where a 4-Kbyte block is programmed in 1,024 operations, writing two words at a time, and erased thereafter. In this case, the block is reckoned as having been programmed and erased once.
If the program and erase cycles are 1,000 times, each block can be erased up to 1,000 times.

Table 30.2 Flash Memory Rewrite Modes Overview

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	The flash memory is rewritten when the CPU executes software commands. EW0 mode: Rewritable in areas other than the flash memory EW1 mode: Rewritable in the flash memory	The flash memory is rewritten using a dedicated serial programmer. Standard serial I/O mode 1: Clock synchronous serial I/O Standard serial I/O mode 2: Two-wire clock asynchronous serial I/O	The flash memory is rewritten using a dedicated parallel programmer.
Areas which can be rewritten	Program ROM 1, program ROM 2, and data flash	Program ROM 1, program ROM 2, and data flash	Program ROM 1, program ROM 2, and data flash
ROM programmer	None	Serial programmer	Parallel programmer

30.2 Memory Map

The flash memory is used as ROM in this product. The flash memory comprises program ROM 1, program ROM 2, and data flash. Figure 30.1 shows a Flash Memory Block Diagram.

The flash memory is divided into several blocks, each of which can be protected (locked) from programming or erasing. The flash memory can be rewritten in CPU rewrite, standard serial I/O, and parallel I/O modes.

If the size of program ROM 1 is over 512 Kbytes, blocks 8 to 11 can be used when the IRON bit in the PRG2C register is 1 (program ROM 1 addresses 40000h to 7FFFFh enabled).

Program ROM 2 can be used when the PRG2C0 bit in the PRG2C register is set to 0 (program ROM 2 enabled). Program ROM 2 includes a user boot code area.

Data flash can be used when the PM10 bit in the PM1 register is set to 1 (0E000h to 0FFFFh: data flash). Data flash is divided into block A and block B.

Table 30.3 lists the differences among program ROM 1, program ROM 2, and data flash.

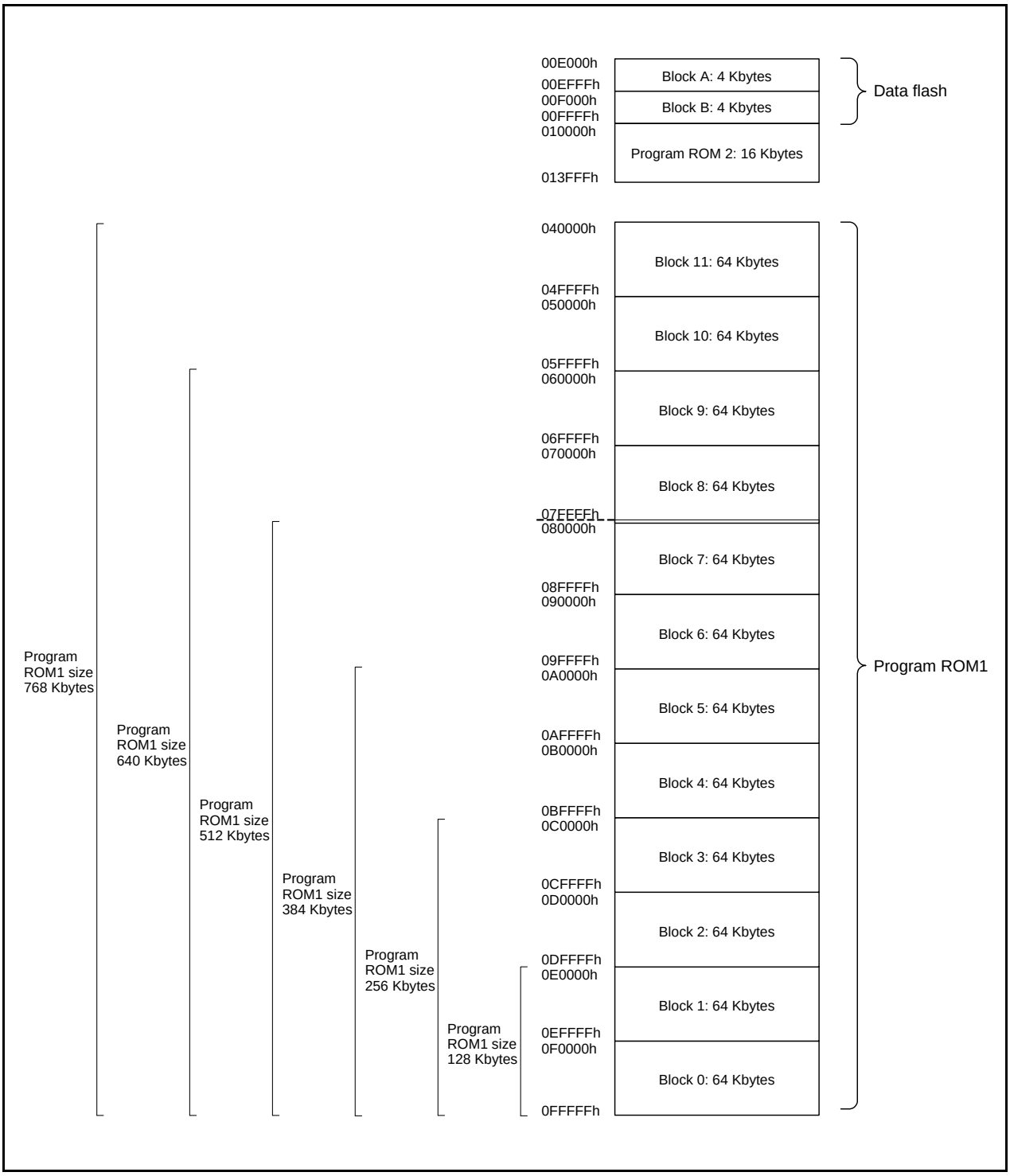


Figure 30.1 Flash Memory Block Diagram

Table 30.3 Program ROM 1, Program ROM 2, and Data Flash

Item	Flash Memory		
	Program ROM 1	Program ROM 2	Data Flash
Program and erase cycles	1,000 times		10,000 times
Forced erase function	Enabled		Disabled
Frequency limit when reading	No		Yes

30.3 Registers

Table 30.4 Register Structure

Address	Register Name	Register Symbol	After Reset
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h	Flash Memory Control Register 3	FMR3	XXXX 0000b
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b

30.3.1 Flash Memory Control Register 0 (FMR0)

Flash Memory Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
		0	0				

Symbol: FMR0 — Address: 0220h — After Reset: 0000 0001b (other than user boot mode), 0010 0001b (user boot mode)

Bit Symbol	Bit Name	Function	RW
FMR00	RY/$\overline{BY}$ status flag	0 : Busy (being written or erased) 1 : Ready	RO
FMR01	CPU rewrite mode select bit	0 : CPU rewrite mode disabled 1 : CPU rewrite mode enabled	RW
FMR02	Lock bit disable select bit	0 : Lock bit enabled 1 : Lock bit disabled	RW
FMSTP	Flash memory stop bit	0 : Flash memory operation enabled 1 : Flash memory operation stopped (low power-mode, flash memory initialized)	RW
— (b4)	Reserved bit	Set to 0	RW
— (b5)	Reserved bit	Set to 0 in other than user boot mode Set to 1 in user boot mode	RW
FMR06	Program status flag	0 : Completed as expected 1 : Completed in error	RO
FMR07	Erase Status Flag	0 : Completed as expected 1 : Completed in error	RO

FMR00 (RY/$\overline{BY}$ Status Flag) (b0)

This bit indicates the flash memory operating state.
Condition to become 0:
During the following commands execution:
Program, block erase, lock bit program, read lock bit status, and block blank check
Condition to become 1:
Other than those above.

FMR01 (CPU Rewrite Mode Select Bit) (b1)

Commands can be accepted by setting the FMR01 bit to 1 (CPU rewrite mode enabled).
To set the FMR01 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers will occur before writing 1 after writing 0.
While in EW0 mode, write to this bit from a program in an area other than flash memory.
Enter read array mode, and then set this bit to 0.

FMR02 (Lock Bit Disable Select Bit) (b2)

The lock bit is disabled by setting the FMR02 bit to 1 (lock bit disabled) (Refer to 30.8.2 “Data Protect Function”).
The FMR02 bit does not change the lock bit data but disables the lock bit function. If an erase command is executed when the FMR02 bit is set to 1, the lock bit data status changes from 0 (locked) to 1 (unlocked) after command execution is completed.
To set the FMR02 bit to 1, write 0 and then 1 in succession when the FMR01 bit is 1. Make sure no interrupts or DMA transfers will occur before writing 1 after writing 0.

FMSTP (Flash Memory Stop Bit) (b3)

The FMSTP bit resets flash memory control circuits and minimizes current consumption in the flash memory. Access to the internal flash memory is disabled when the FMSTP bit is set to 1 (flash memory operation stopped). Set the FMSTP bit by a program located in an area other than the flash memory.
Set the FMSTP bit to 1 under the following condition.

- A flash memory access error occurs while erasing or programming in EW0 mode (the FMR00 bit does not switch back to 1 (ready)).

Use the following steps to rewrite the FMSTP bit.
To stop the flash memory:
(1)Set the FMSTP bit to 1.
(2)Wait the wait time to stabilize flash memory circuit (tps).
To restart the flash memory:
(1)Set the FMSTP bit to 0.
(2)Wait the wait time to stabilize flash memory circuit (tps).

The FMSTP bit is valid when the FMR01 bit is 1 (CPU rewrite mode). If the FMR01 bit is 0, although the FMSTP bit can be set to 1 by writing 1, the flash memory is neither placed in low-power mode nor initialized.
When the FMR23 bit is set to 1 (low-current consumption read mode enabled), do not set the FMSTP bit in the FMR0 register to 1 (flash memory operation stopped). Also, when the FMSTP bit is set to 1, do not set the FMR23 bit to 1.

FMR06 (Program Status Flag) (b6)

This bit indicates the auto-program operation state.
Condition to become 0:

- Execute the clear status command.

Condition to become 1:

- Refer to 30.8.5.4 “Full Status Check”.

The following commands cannot be accepted when the FMR06 bit is 1:
Program, block erase, lock bit program, read lock bit status, and block blank check.

FMR07 (Erase Status Flag) (b7)

This bit indicates the auto-erase operation state.
Condition to become 0:

- Execute the clear status command

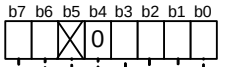
Condition to become 1:

- Refer to 30.8.5.4 “Full Status Check”.

The following commands cannot be accepted when the FMR07 bit is 1:
Program, block erase, lock bit program, read lock bit status, and block blank check.

30.3.2 Flash Memory Control Register 1 (FMR1)

Flash Memory Control Register 1



Symbol: FMR1 | Address: 0221h | After Reset: 00X0 XX0Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	Read as undefined value	RO
FMR11	Write to FMR6 register enable bit	0 : Disabled 1 : Enabled	RW
— (b3-b2)	Reserved bits	Read as undefined value	RO
— (b4)	Reserved bit	Set to 0	RW
— (b5)	No register bit. If necessary, set to 0. Read as undefined value		RW
FMR16	Lock bit status flag	0 : Lock 1 : Unlock	RO
FMR17	Data flash wait bit	0 : 1 wait 1 : Follow the setting of the PM17 bit	RW

FMR16 (Lock Bit Status Flag) (b6)

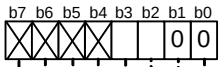
This bit indicates the execution result of the read lock bit status command.

FMR17 (Data Flash Wait Bit) (b7)

This bit is used to select the number of wait states for data flash.

30.3.3 Flash Memory Control Register 2 (FMR2)

Flash Memory Control Register 2



Symbol: FMR2 | Address: 0222h | After Reset: XXXX 0000b

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0	RW
FMR22	Slow read mode enable bit	0 : Disabled 1 : Enabled	RW
FMR23	Low-current consumption read mode enabled bit	0 : Disabled 1 : Enabled	RW
— (b7-b4)	No register bits. If necessary, set to 0. Read as undefined value.		—

FMR22 (Slow Read Mode Enable Bit) (b2)

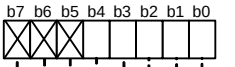
Refer to 9.4 “Power Control in Flash Memory”.

FMR23 (Low-current Consumption Read Mode Enable Bit) (b3)

Refer to 9.4 “Power Control in Flash Memory”.

30.3.4 Flash Memory Control Register 3 (FMR3)

Flash Memory Control Register 3



Symbol	Address	After Reset
FMR3	0223h	XXXX 0000b

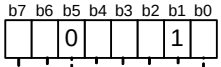
Bit Symbol	Bit Name	Function	RW
FMR30	Suspend function enable bit	0 : Disabled 1 : Enabled	RW
FMR31	Suspend request bit	0 : Command restart 1 : Suspend request	RW
FMR32	Erase suspend status flag	0 : Erase suspend not accepted 1 : Erase suspend accepted	RO
FMR33	Program suspend status flag	0 : Program suspend not accepted 1 : Program suspend accepted	RO
— (b4)	Reserved bit	Read as undefined value	RO
— (b7-b5)	No register bits. If necessary, set to 0. Read as undefined value		—

FMR30 (Suspend Function Enable Bit) (b0)

To set the FMR30 bit to 1, write 0 and then 1 in succession. Make sure no interrupts or DMA transfers will occur before writing 1 after writing 0.

30.3.5 Flash Memory Control Register 6 (FMR6)

Flash Memory Control Register 6



Symbol: FMR6 | Address: 0230h | After Reset: XX0X XX00b

Bit Symbol	Bit Name	Function	RW
FMR60	EW1 mode select bit	0 : EW0 mode 1 : EW1 mode	RW
FMR61	Reserved bit	Set to 1	RW
— (b4-b2)	Reserved bits	Read as undefined value	RO
— (b5)	Reserved bit	Set to 0	RW
— (b7-b6)	Reserved bits	Read as undefined value	RO

FMR60 (EW1 Mode Select Bit) (b0)

To set the FMR60 bit to 1, write 1 when both bits FMR01 and FMR11 are 1.

FMR61 (b1)

Set the FMR61 bit to 1 when using CPU rewrite mode.

30.4 Optional Function Select Address 1 (OFS1)

In an option function select area, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected.

The option function select area is not a special function register (SFR), and therefore cannot be rewritten by a program. Set a proper value when writing a program in the flash memory. The whole option function select area is set to FFh when the block including the option function select area is erased.

Optional Function Select Address 1

b7	b6	b5	b4	b3	b2	b1	b0
			1			1	

Symbol	Address	Factory Setting
OFS1	FFFFFh	FFh

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Watchdog timer starts automatically after reset. 1 : Watchdog timer is in a stopped state after reset.	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect cancel bit	0 : ROM code protection cancelled. 1 : ROMCP1 bit enabled.	RW
ROMCP1	ROM code protect bit	0 : ROM code protection enabled. 1 : ROM code protection disabled.	RW
— (b4)	Reserved bit	Set to 1.	RW
VDSEL1	Vdet0 select bit 1	0 : 2.85 V (Vdet0_2) 1 : 1.90 V (Vdet0_0)	RW
LVDAS	Voltage detection 0 circuit start bit	0 : Voltage monitor 0 reset enabled after hardware reset. 1 : Voltage monitor 0 reset disabled after hardware reset.	RW
CSPROINI	After-reset count source protection mode select bit	0 : Count source protection mode enabled after reset. 1 : Count source protection mode disabled after reset.	RW

ROMCR (ROM Code Protect Disable Bit) (b2)
ROMCP1 (ROM Code Protect Bit) (b3)

These bits are used to inhibit the flash memory from being read or rewritten during parallel I/O mode.

Table 30.5 ROM Code Protect

Bit Setting		ROM Code Protect
ROMCR bit	ROMCP1 bit	
0	0	Disabled
0	1	
1	0	Enabled
1	1	Disabled

30.5 Flash Memory Rewrite Disable Function

This function inhibits the flash memory from being read, written, and erased. The details are shown for each mode.

Parallel I/O mode

ROM code protect function

Standard serial I/O mode

ID code check function, forced erase function, and standard serial I/O mode disable function

30.6 Boot Mode

A hardware reset occurs while a low-level signal is applied to the P5_5 pin and a high-level signal is applied to pins CNVSS and P5_0. After reset, the MCU enters boot mode. In boot mode, user boot mode or standard serial I/O mode is selected in accordance with the content of a user boot code area.

30.7 User Boot Function

User boot mode can be selected by the status of a port when the MCU starts in boot mode. Table 30.6 shows the User Boot Function Specifications.

Table 30.6 User Boot Function Specifications

Item	Specification
Entry pin	None or select a port from P0 to P14
User boot start level	Select high or low
User boot start address	Address 10000h (the start address of program ROM 2)

Set “UserBoot” in ASCII code to the addresses 13FF0h to 13FF7h in the user boot code area, select a port for entry from addresses 13FF8h to 13FF9h and 13FFAh, and select the start level with the address 13FFBh. After starting boot mode, user boot mode or standard serial I/O mode is selected in accordance with the level of the selected port.

In addition, if addresses 13FF0h to 13FF7h are set to “UserBoot” in ASCII code and addresses 13FF8h to 13FFBh are set to “00h”, user boot mode is selected.

In user boot mode, the program of address 10000h (the start address of program ROM2) is executed. The content of the OFS1 address is valid.

Figure 30.2 shows User Boot Code Area, Table 30.7 lists Start Mode (When the Port Pi_j is Selected for Entry) (1), Table 30.8 lists “UserBoot” in ASCII Code, and Table 30.9 lists Addresses of Selectable Ports for Entry.

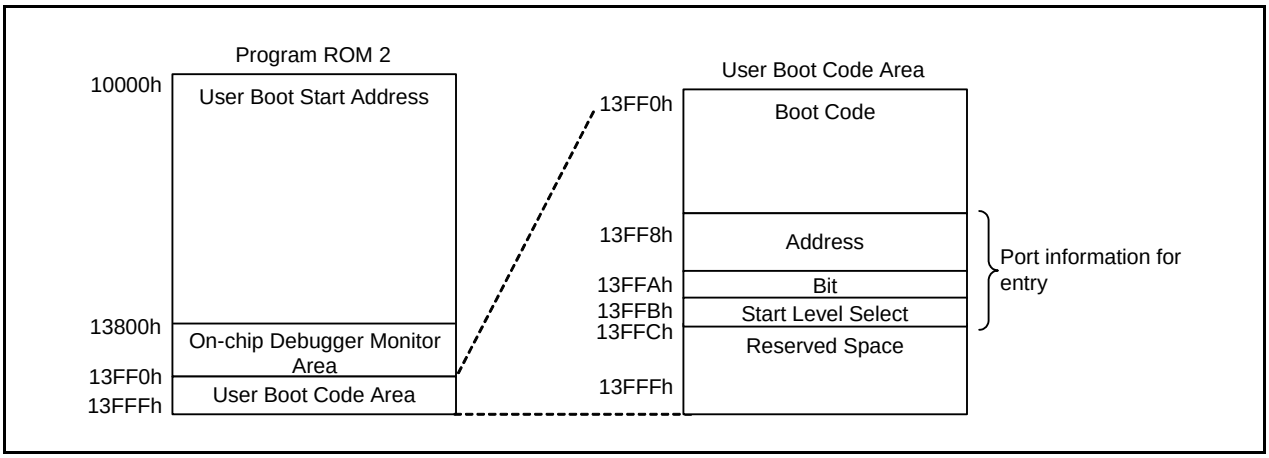


Figure 30.2 User Boot Code Area

Table 30.7 Start Mode (When the Port Pi_j is Selected for Entry) (1)

Boot Code (13FF0h to 13FF7h)	Port information for entry			Port Pi_j input level	Start Mode
	Address (13FF8h to 13FF9h)	Bit (13FFAh)	Start level Select (13FFBh)		
"UserBoot" in ASCII code (2)	0000h	00h	00h	–	User boot mode
	Pi register address (3)	00h to 07h (value of j)	00h	high	Standard serial I/O mode
				low	User boot mode
	Pi register address (3)	00h to 07h (value of j)	01h	high	User boot mode
				low	Standard serial I/O mode
Other than "UserBoot" in ASCII code	–	–	–	–	Standard serial I/O mode

i=0 to 14, j=0 to 7 (when i = 14, j = 0, 1)

Notes:
1. Do not use the combinations of values not listed in Table 30.7.
2. Refer to Table 30.8 ""UserBoot" in ASCII Code"
3. Refer to Table 30.9 "Addresses of Selectable Ports for Entry"

Table 30.8 "UserBoot" in ASCII Code

Address	ASCII Code
13FF0h	55h (upper-case U)
13FF1h	73h (lower-case s)
13FF2h	65h (lower-case e)
13FF3h	72h (lower-case r)
13FF4h	42h (upper-case B)
13FF5h	6Fh (lower-case o)
13FF6h	6Fh (lower-case o)
13FF7h	74h (lower-case t)

Table 30.9 Addresses of Selectable Ports for Entry

Port	Address	Port	Address	Port	Address
P0	03E0h	P6	03ECh	P12	03F8h
P1	03E1h	P7	03EDh	P13	03F9h
P2	03E4h	P8	03F0h	P14	03FCh
P3	03E5h	P9	03F1h	-	-
P4	03E8h	P10	03F4h		
P5	03E9h	P11	03F5h		

30.8 CPU Rewrite Mode

In CPU rewrite mode, the flash memory can be rewritten when the CPU executes software commands. Program ROM 1, program ROM 2, and data flash can be rewritten with the MCU mounted on a board and without using a ROM programmer.
The program and block erase commands are executed only in individual block areas of program ROM 1, program ROM 2, and data flash.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode. Table 30.10 lists the differences between EW0 mode and EW1 mode.

Table 30.10 EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	• Single-chip mode • Memory expansion mode	Single-chip mode
Rewrite control Program allocatable area	• Program ROM 1 • Program ROM 2 • External area	• Program ROM 1 • Program ROM 2
Rewrite Control Program Executable Area	The rewrite control program must be transferred to an area other than the flash memory (e.g., RAM) before being executed.	The rewrite control program can be executed in program ROM 1 and program ROM 2.
Rewritable area	• Program ROM 1 • Program ROM 2 • Data flash	• Program ROM 1 • Program ROM 2 • Data flash Excluding blocks with the rewrite control program
Software command restriction	None	• Program and block erase commands Do not execute in a block with the rewrite control program. • Read status register command Do not execute.
Mode after program or erase	Read status register mode	Read array mode
State during auto write and auto erase	Hold state is not maintained.	Hold state is maintained. (I/O ports maintains the state before the command execution) (1)
Flash memory status detection	• Read bits FMR00, FMR06, and FMR07 in the FMR0 register by a program. • Execute the read status register command, and then read bits SR7, SR5 and SR4 in the status register.	Read bits FMR00, FMR06, and FMR07 in the FMR0 register by a program.

Note:
1. Do not generate an interrupt (except $\overline{\text{NMI}}$ interrupt) or start a DMA transfer.

30.8.1 Operating Speed

Set a CPU clock frequency of 10 MHz or less by the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to 1 (wait state).

30.8.2 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR02 bit to 0 (lock bit enabled). The lock bit allows blocks to be individually protected (locked) against programming and erasure. This prevents data from being inadvertently written to or erased from the flash memory. Table 30.11 lists Lock Bit and Block State.

Table 30.11 Lock Bit and Block State

FMR02 Bit in the FMR0 Register	Lock Bit	Block State
0 (enabled)	0 (locked)	Protected against programming and erasure
	1 (unlocked)	Can be programmed or erased
1 (disabled)	0 (locked)	Can be programmed or erased
	1 (unlocked)	

Condition to become 0:
- Execute the lock bit command

Condition to become 1:
- Execute the block erase command while the FMR02 bit in the FMR0 register is set to 1 (lock bit disabled).

If the block erase command is executed while the FMR02 bit is set to 1, the target block is erased regardless of lock bit status. The lock bit data can be read by the read lock bit status command.
Refer to 30.8.4 “Software Command”, for details on each command.

30.8.3 Suspend Function (under review)

The suspend function suspends automatic programming and erasure. It can be used for an interrupt operation because program ROM1, program ROM2, and data flash can be read while automatic programming or erasure is suspended. Enable the interrupts used to enter suspend mode beforehand.
The program command, erase command, and lock bit program command are subjects for suspend. Suspend operation is the same for the program command and lock bit program command, so both commands are described together as program suspend.
Do not suspend again in suspend mode. Table 30.12 lists Operation after the Program, Erase, or Lock Bit Program Command is Issued during Suspend.

Table 30.12 Operation after the Program, Erase, or Lock Bit Program Command is Issued during Suspend

Suspend	Command	Operation	
		Blocks erased or programmed before the suspend mode is entered	Other blocks
Erase suspend	Program command	Commands are not executed. Command sequence error occurs.	Program command is executed. Program suspend does not start or an error does not occur even when the FMR31 bit is set to 1 (suspend request).
	Erase command	Commands are not executed. Command sequence error occurs.	
	Lock bit program command	Commands are not executed. Command sequence error occurs.	Lock bit program can be executed.
Program suspend	Program command	Commands are not executed. Command sequence error occurs.	
	Erase command		
	Lock bit program command		

30.8.4 Software Command

Table 30.13 and show Software Commands. Read or write commands and data in 16-bit units. When command code is written, the 8 high-order bits (D15 to D8) are ignored.

Table 30.13 Software Commands (Program ROM 1 is not over 512 Kbytes)

Command	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)
Read array	Write	x	xxFFh						
Read status register	Write	x	xx70h	Read	x	SRD			
Clear status register	Write	x	xx50h						
Program	Write	WA	xx41h	Write	WA	WD0	Write	WA	WD1
Block erase	Write	x	xx20h	Write	BA	xxD0h			
Lock bit program	Write	BA	xx77h	Write	BA	xxD0h			
Read lock bit status	Write	x	xx71h	Write	BA	xxD0h			
Block blank check	Write	x	xx25h	Write	BA	xxD0h			

SRD : Data in the status register (D7 to D0)
WA : Write address (Set the end of the address to 0, 4, 8, or C (hexadecimal).)
WD0 : Write data low-order word (16 bits)
WD1 : Write data high-order word (16 bits)
BA : Highest-order block address (even address)
x : Any even address in program ROM 1, program ROM 2, or data flash
xx : Eight high-order bits of command code (ignored)

Table 30.14 Software Commands (Program ROM 1 is over 512 Kbytes)

Command	First Bus Cycle			Second Bus Cycle			Third Bus Cycle			Fourth Bus Cycle		
	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)	Mode	Address	Data (D15 to D0)
Read array	Write	B0-7	xxFFh	Write	B8	xxFFh	-	-	-	-	-	-
Read status register	Write	BA	xx70h	Read	X	SRD	-	-	-	-	-	-
Clear status register	Write	B0-7	xx50h	Write	B8	xx50h	-	-	-	-	-	-
Program	Write	BX	xx70h	Write	WA	xx41h	Write	WA	WD0	Write	WA	WD1
Block erase	Write	BX	xx70h	Write	BA	xx20h	Write	BA	xxD0h	-	-	-
Lock bit program	Write	BA	xx77h	Write	BA	xxD0h	-	-	-	-	-	-
Read lock bit status	Write	BA	xx71h	Write	BA	xxD0h	-	-	-	-	-	-
Block blank check	Write	BX	xx70h	Write	BA	xx25h	Write	BA	xxD0h	-	-	-

SRD : Data in the status register (D7 to D0)
WA : Write address (Make sure 0, 4, 8 or C (hexadecimal) comes at the end of the write address, e.g. xxxx0h.)
WD0 : Write data low-order word (16 bits)
WD1 : Write data high-order word (16 bits)
BA : Highest-order block address (even address)
x : Any even address in program ROM 1, program ROM 2, or data flash
B0-7 : Any even address in blocks 0 to 7, program ROM 2, or data flash
B8 : Any even address in blocks after 8.
xx : Eight high-order bits of command code (ignored)
BX : Any even address in blocks after block 8 when the target blocks are blocks 0 to 7, program ROM 2, or data flash.
Any even address in blocks 0 to 7, program ROM 2, or data flash when the target blocks are blocks after 8.

Software commands when program ROM1 is not over 512 Kbytes are described below. Refer to 30.8.3 “Suspend Function (under review)” for program, block erase, and lock bit program commands when using suspend function.

30.8.4.1 Read Array Command

The read array command is used to read the flash memory.
By writing the command code xxFFh in the first bus cycle, the flash memory enters read array mode. The content of the specified address can be read in 16-bit units by entering the address to be read after the next bus cycle.
The flash memory remains in read array mode until another command is written. Therefore, the contents of multiple addresses can be read consecutively.

30.8.4.2 Read Status Register Command

The read status register command is used to read the status register.
By writing the command code xx70h in the first bus cycle, the status register can be read in the second bus cycle. (Refer to 30.8.5 “Status Register”). To read the status register, read an even address in the program ROM 1, program ROM 2, or data flash.
Do not execute this command in EW1 mode.

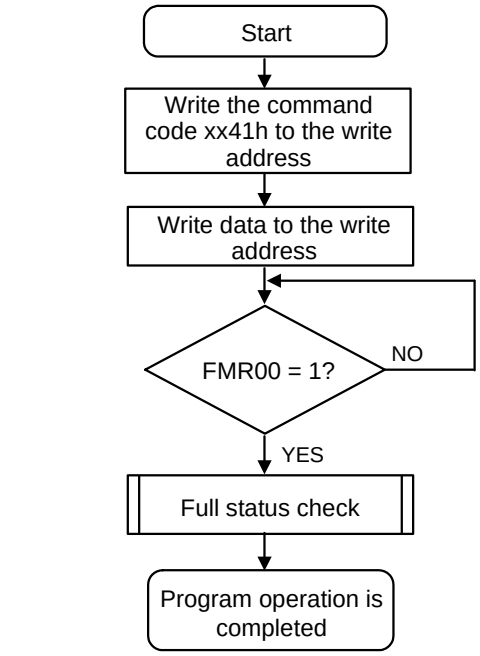
30.8.4.3 Clear Status Register Command

The clear status register command is used to clear the status register.
By writing the command code xx50h in the first cycle, bits FMR07 and FMR06 in the FMR0 register are set to 00b, and bits SR5 and SR4 in the status register are set to 00b.

30.8.4.4 Program Command

The program command is used to write two words (4 bytes) of data to the flash memory.
By writing xx41h in the first bus cycle and data to the write address in the second and third bus cycles, auto-program operation (data program and verify) is started. Make sure 0, 4, 8 or C (hexadecimal) comes at the end of the write address, e.g. xxxx0h.
The FMR00 bit in the FMR0 register indicates whether the auto-program operation has been completed. The FMR00 bit is set to 0 (busy) during the auto-program operation and to 1 (ready) after the auto-program operation is completed.
After the auto-program operation is completed, the FMR06 bit in the FMR0 register indicates whether or not the auto-program operation has been completed as expected. (Refer to 30.8.5.4 “Full Status Check”).
Do not rewrite the addresses already programmed. Figure 30.3 shows a Flow Chart of the Program Command Programming (Suspend Function Disabled).
The lock bit protects individual blocks from being programmed inadvertently. (Refer to 30.8.2 “Data Protect Function”.)

In EW1 mode, do not execute this command on a block to which the rewrite control program is allocated.
In EW0 mode, the flash memory enters read status register mode as soon as the auto-program operation starts. The status register can be read. The SR7 bit in the status register is set to 0 at the same time the auto-program operation starts. It is set to 1 when the auto-program operation is completed. The flash memory remains in read status register mode until the read array command is written. After the auto-program operation is completed, the status register indicates whether or not the auto-program operation has been completed as expected.

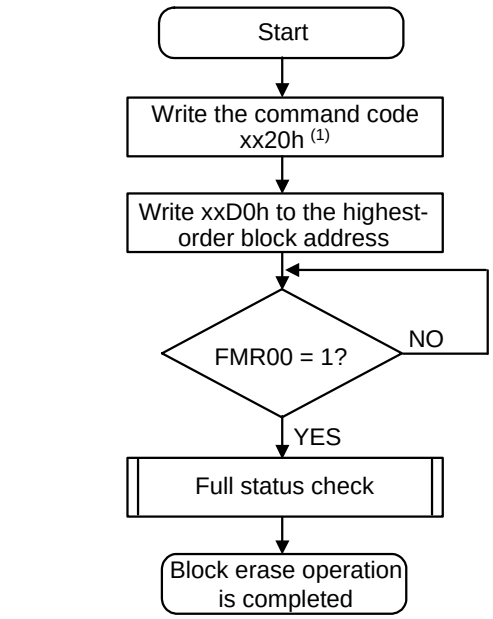


Note:
1. Write the command code and data to even addresses.

Figure 30.3 Program Command (Suspend Function Disabled)

30.8.4.5 Block Erase Command

By writing xx20h in the first bus cycle and xxD0h to the highest-order even address of a block in the second bus cycle, an auto-erase operation (erase and verify) is started on the specified block.
The FMR00 bit in the FMR0 register indicates whether the auto-erase operation has been completed. The FMR00 bit is set to 0 (busy) during the auto-erase operation and to 1 (ready) when the auto-erase operation is completed.
After the auto erase operation is completed, the FMR07 bit in the FMR0 register indicates whether or not the auto erase operation has been completed as expected. (Refer to 30.8.5.4 “Full Status Check”).
Figure 30.4 shows a Flow Chart of the Block Erase Command Programming (Suspend Function Disabled).
The lock bit protects individual blocks from being erased inadvertently. (Refer to 30.8.2 “Data Protect Function”.)
In EW1 mode, do not execute this command on the block to which the rewrite control program is allocated.
In EW0 mode, the flash memory enters read status register mode as soon as the auto-erase operation starts. The status register can be read. The SR7 bit in the status register is set to 0 at the same time an auto erase operation starts. It is set to 1 when the auto-erase operation is completed. The flash memory remains in read status register mode until the read array command or read lock bit status command is written.
If an erase error occurs, execute the clear status register command and then block erase command at least three times until the erase error is not generated.

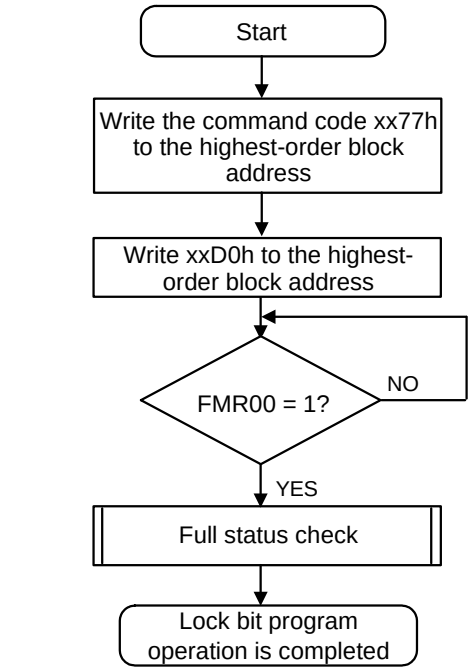


Notes:
1. Write the command code and data to even addresses.

Figure 30.4 Block Erase Command (Suspend Function Disabled)

30.8.4.6 Lock Bit Program Command

The lock bit program command is used to set the lock bit for a specified block to 0 (locked).
By writing xx77h in the first bus cycle and xxD0h to the highest-order even address of a block in the second bus cycle, the lock bit for the specified block is set to 0. The address value specified in the first bus cycle must be the same highest-order address of a block specified in the second bus cycle.
Figure 30.5 shows a Flow Chart of the Lock Bit Program Command Programming (Suspend Function Disabled). Execute the read lock bit status command to read the lock bit state (lock bit data).
The FMR00 bit in the FMR0 register indicates whether a lock bit program operation has been completed.
Refer to 30.8.2 “Data Protect Function”, for details on lock bit functions and how to set it to 1 (unlocked).

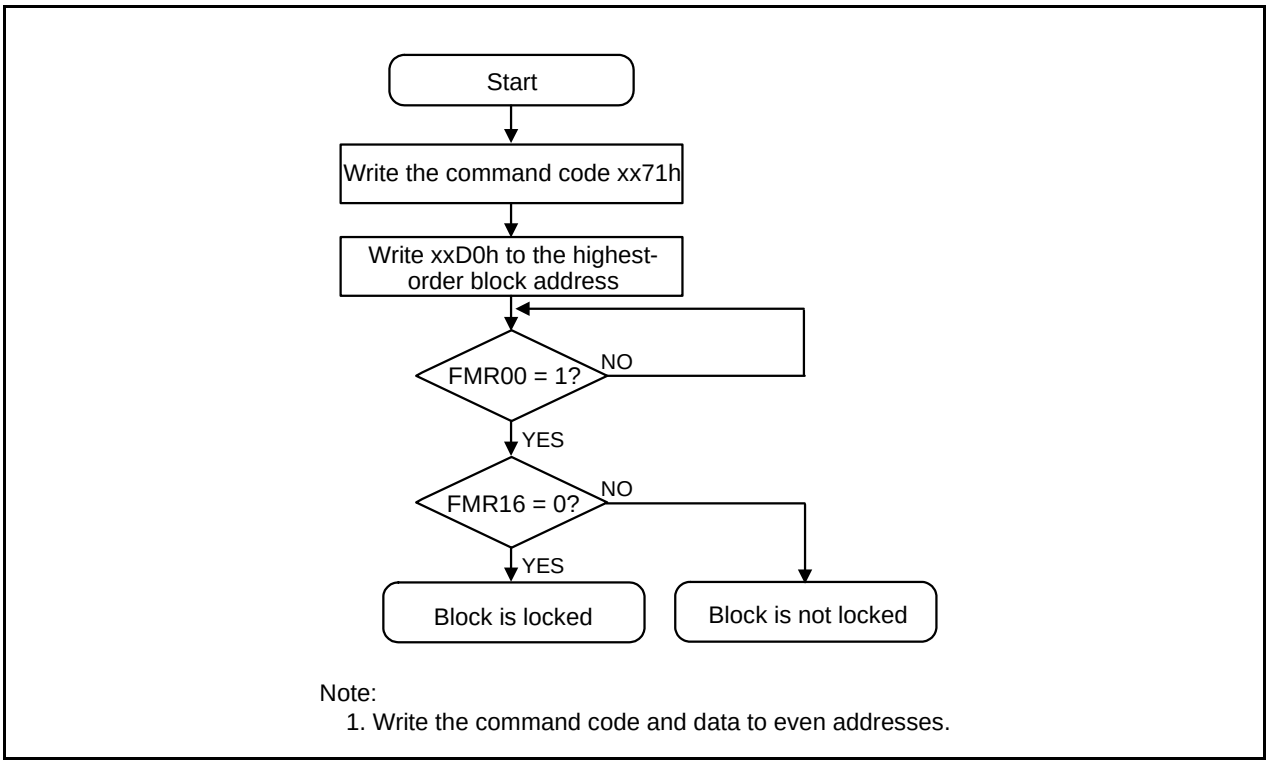


Note:
1. Write the command code and data to even addresses.

Figure 30.5 Lock Bit Program Command (Suspend Function Disabled)

30.8.4.7 Read Lock Bit Status

The read lock bit status command is used to read the lock bit state of a specified block.
By writing xx71h in the first bus cycle and xxD0h to the highest-order even address of a block in the second bus cycle, the FMR16 bit in the FMR1 register stores information on the lock bit status of a specified block. Read the FMR16 bit after the FMR00 bit in the FMR0 register is set to 1 (ready).
Figure 30.6 shows a Flow Chart of the Read Lock Bit Status Command Programming.



Note:
1. Write the command code and data to even addresses.

Figure 30.6 Read Lock Bit Status Command

30.8.4.8 Block Blank Check Command

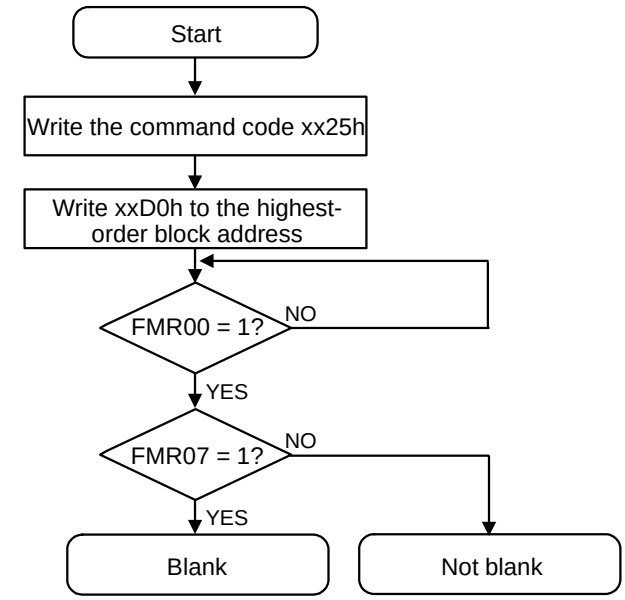
The block blank check command is used to check whether or not a specified block is blank (state after erase).

By writing xx25h in the first bus cycle and xxD0h in the second bus cycle to the highest-order even address of a block, the check result is stored in the FMR07 bit in the FMR0 register. Read the FMR07 bit after the FMR00 bit in the FMR0 register is set to 1 (ready).

The block blank check command is valid for unlocked blocks.

If the block blank check command is executed on a block whose lock bit is 0 (locked), the FMR07 bit (SR5) is set to 1 (not blank) regardless of the FMR02 bit state.

Figure 30.7 shows a Flow Chart of the Block Blank Check Command Programming.



Note:
1. Write the command code and data to even addresses.

Figure 30.7 Block Blank Check Command

30.8.5 Status Register

The status register indicates flash memory operating state and whether or not an erase or program operation has completed as expected.
Bits FMR00, FMR06, and FMR07 in the FMR0 register indicate status register states.
In EW0 mode, the status register can be read in one of the following cases.

- Any even address in program ROM 1, program ROM 2, or data flash is read after the read status register command is written.
- Any even address in the program ROM 1, program ROM 2, or data flash is read from when the program command, block erase command, lock bit program command, or block blank check command is executed until when the read array command is executed.

Table 30.15 shows Status Register.

Table 30.15 Status Register

Bits in Status Register	Bit in FMR0 Register	Status	Definition		Value after Reset
			0	1	
SR0 (D0)	-	Reserved bit	-	-	-
SR1 (D1)	-	Reserved bit	-	-	-
SR2 (D2)	-	Reserved bit	-	-	-
SR3 (D3)	-	Reserved bit	-	-	-
SR4 (D4)	FMR06	Program status	Completed as expected	Completed in error	0
SR5 (D5)	FMR07	Erase status	Completed as expected	Completed in error	0
SR6 (D6)	-	Reserved bit	-	-	-
SR7 (D7)	FMR00	Sequencer status	Busy	Ready	1

D0 to D7: The data buses read when the read status register command is executed.

30.8.5.1 Sequencer Status (Bits SR7 and FMR00)

The sequencer status indicates flash memory operating state.
Condition to become 0:

- During the following commands execution:
  Program, block erase, lock bit program, read lock bit status, block blank check

Condition to become 1:

- Other than those above

30.8.5.2 Erase Status (Bits SR5 and FMR07)

The erase status indicates auto erase state.
Condition to become 0:

- Execute the clear status command

Condition to become 1:

- Refer to 30.8.5.4 “Full Status Check”.
  When the FMR07 bit is 1, the following commands cannot be accepted:
  Program, block erase, lock bit program, read lock bit status, block blank check

30.8.5.3 Program Status (Bits SR4 and FMR06)

The program status indicates auto-program operating state.
Condition to become 0:
- Execute the clear status command

Condition to become 1:
- Refer to 30.8.5.4 “Full Status Check”.

When the FMR06 bit is 1, the following commands cannot be accepted:
Program, block erase, lock bit program, read lock bit status, block blank check

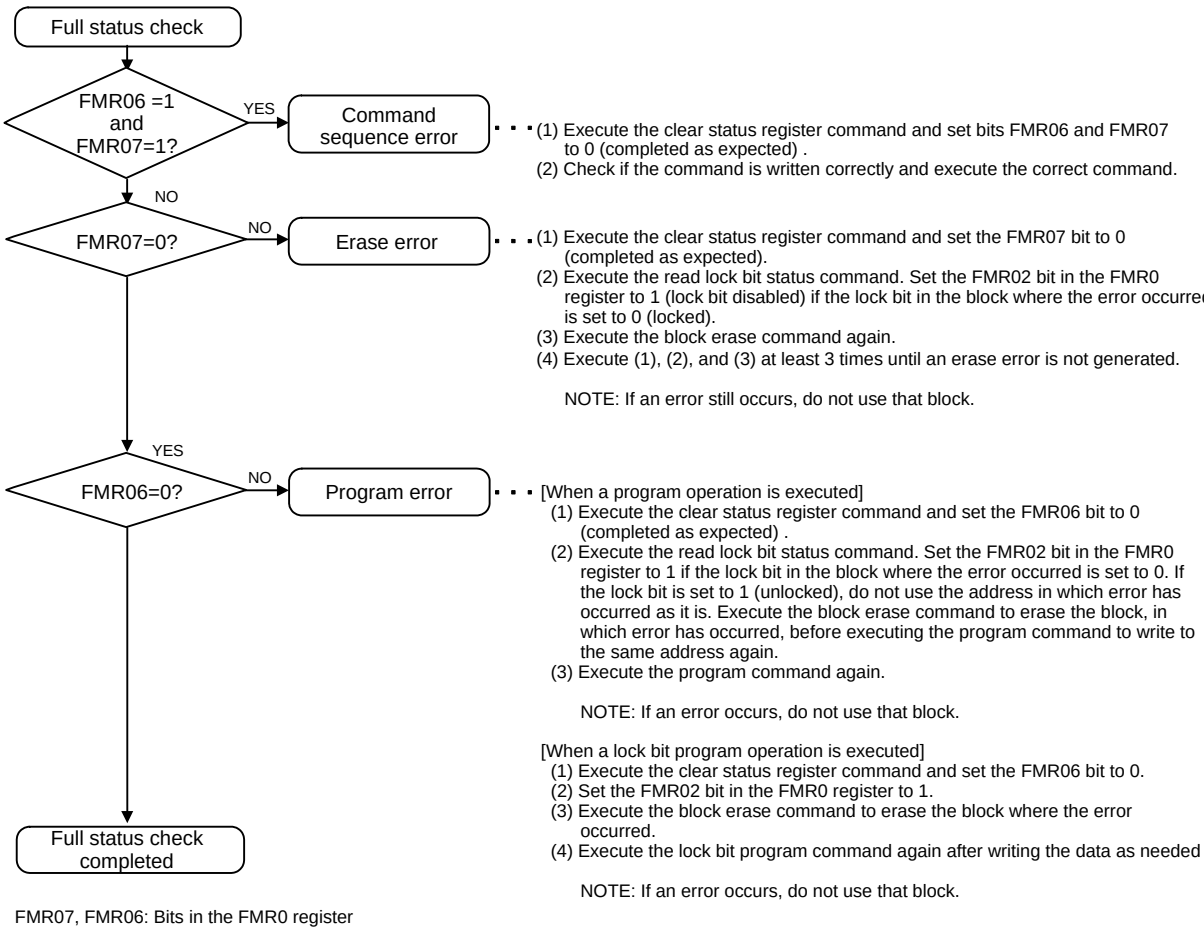
30.8.5.4 Full Status Check

If an error occurs, bits FMR06 and FMR07 in the FMR0 register are set to 1, indicating the occurrence of an error. Therefore, the execution results can be confirmed by checking these status bits (full status check).
Table 30.16 lists Errors and FMR0 Register States and Figure 30.8 shows Full Status Check and Handling Procedure for Errors.

Table 30.16 Errors and FMR0 Register States

FMR00 Register (Status Register) State		Error	Error Occurrence Conditions
FMR07 bit (SR5 bit)	FMR06 bit (SR4 bit)		
1	1	Command Sequence error	• Command is written incorrectly. • Invalid data (data other than xxD0h or xxFFh) is written in the second bus cycle of the lock bit program or block erase command. (1)
1	0	Erase error	• The block erase command is executed on a locked block. (2) • The block erase command is executed on an unlocked block, but the auto-erase operation is not completed as expected. • The block blank check command is executed, and the check result is not blank.
0	1	Program error	• The program command is executed on a locked block. (2) • The program command is executed on an unlocked block, but auto-program operation is not completed as expected. • The lock bit program command is executed, but the lock bit is not written as expected. (2)

Notes:
1. The flash memory enters read array mode by writing command code xxFFh in the second bus cycle of the command. The command code written in the first bus cycle becomes invalid.
2. When the FMR02 bit is set to 1 (lock bit disabled), no error occurs even under the conditions above.



Note: When either FMR06 or FMR07 bit is set to 1 (terminated by error), the program, block erase, lock bit program, block blank check, and read lock bit status commands cannot be accepted. Execute the clear status register command before executing each command.

Figure 30.8 Full Status Check and Handling Procedure for Errors

30.8.6 EW0 Mode

The MCU enters CPU rewrite mode when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled) and is ready to accept commands. EW0 mode is selected by setting the FMR60 bit in the FMR6 register to 0. Figure 30.9 shows Setting and Resetting of EW0 Mode
Software commands control programming and erasing. The FMR0 register or status register indicates whether a program or erase operation is completed as expected or not.

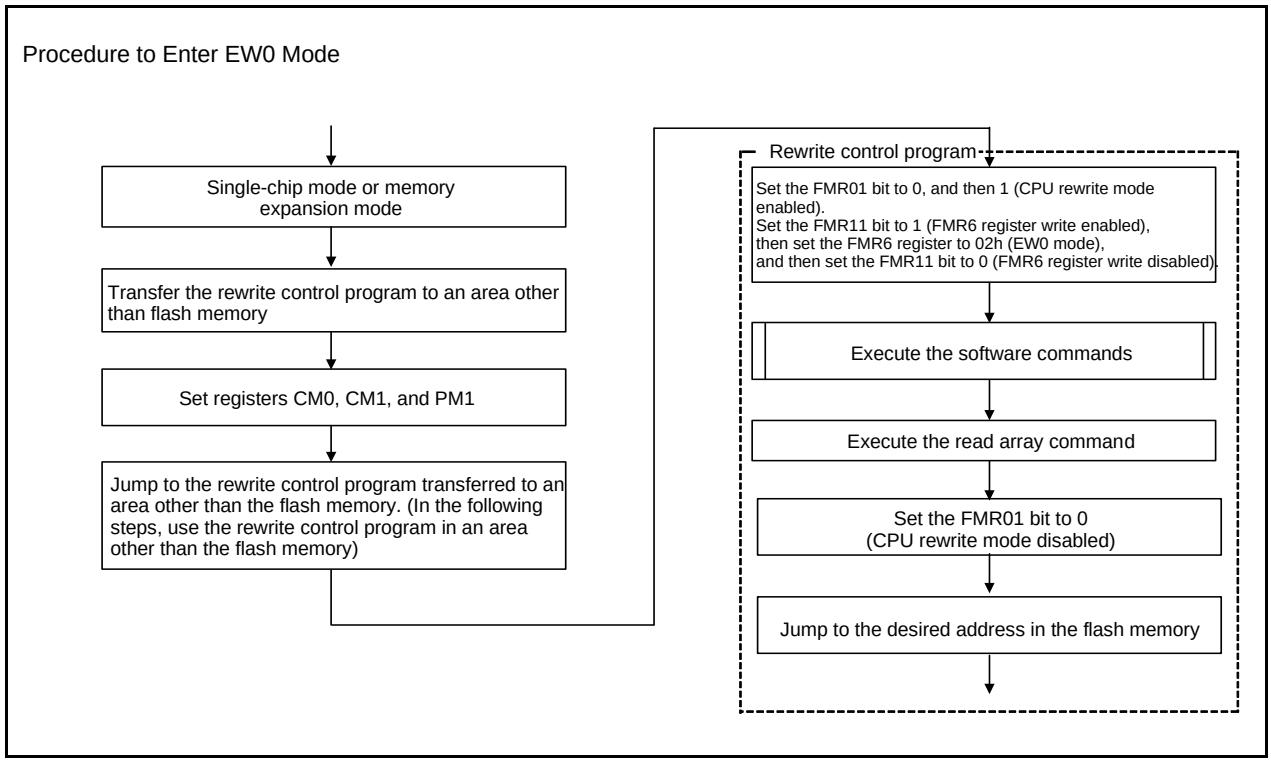


Figure 30.9 Setting and Resetting of EW0 Mode

Do not execute the following instructions:
UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

The following are interrupts which can be used in EW0 mode and operations when the interrupts occur during auto-erase operation or auto-program operation:

- Maskable interrupt (suspend disabled)
  To use the interrupt, allocate a variable vector table in areas other than the flash memory.
- Maskable interrupt (suspend enabled)
  To use the interrupt, allocate a variable vector table in areas other than the flash memory.
  When the FMR00 bit in the FMR0 register is checked in the interrupt routine and the result is 0 (being written or erased), auto-erase operation or auto-program operation suspends after td(SR-SUS) elapses by setting the FMR31 bit in the FMR3 register to 1 (suspend request). Auto-erase operation or auto-program operation restarts by setting the FMR31 bit to 0 (command restart) at the completion of the interrupt.

- $\overline{\text{NMI}}$, watchdog timer, oscillation stop/re-oscillation detect, voltage detect 1, and voltage detect 2 interrupts

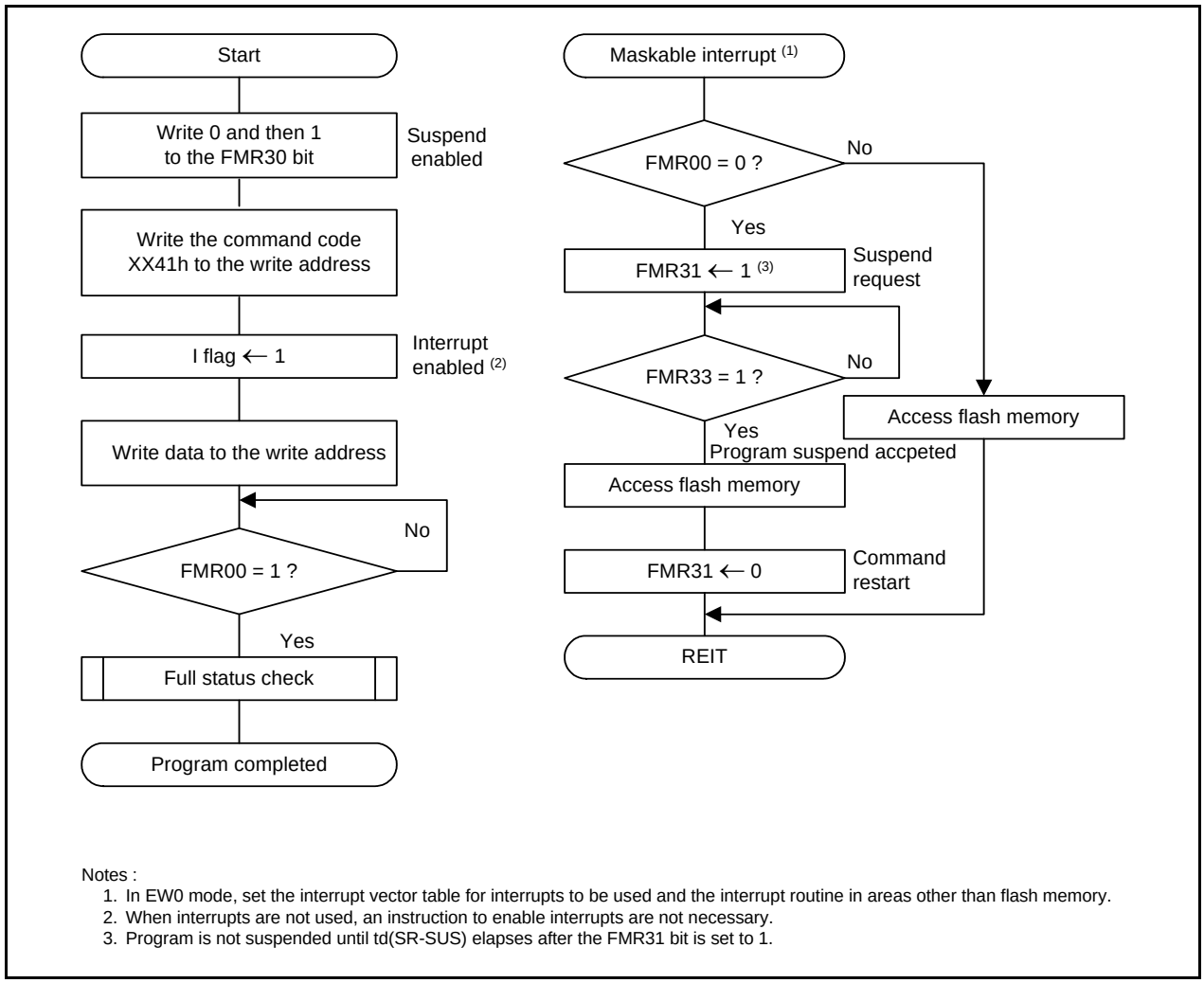
  Auto-erase operation or auto-program operation forcibly stops as soon as the interrupt occurs, and the flash memory is reset. The flash memory restarts after a certain period of time, and then the interrupt process starts.

  After the flash memory restart, execute auto-erase operation again and confirm that it is completed as expected in order to read the correct value.

The watchdog timer is not stopped during the command operation, and the interrupt request can be generated. Initialize the watchdog timer regularly.

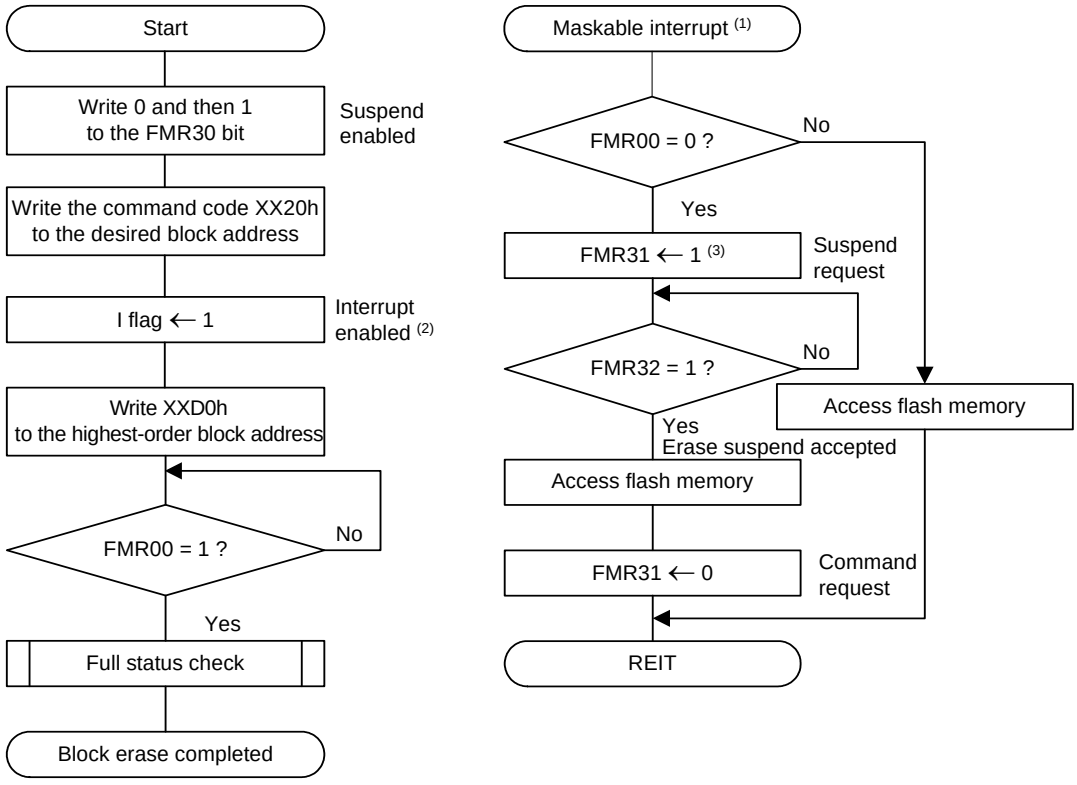
30.8.6.1 Suspend Function (EW0 Mode) (under review)

When using suspend function in EW0 mode, check the status of the flash memory in the interrupt routine and enter suspend mode. Program suspend or erase suspend is not accepted until td (SR-SUS) elapses after the FMR31 bit is set to 1. Access to the flash memory after confirming the acceptance of program suspend or erase suspend by the FMR33 or FMR32 bit. Set the FMR31 bit to 0 (command restart) to restart auto-program and auto-erase operations at the completion of the access to the flash memory. Figure 30.10 to Figure 30.12 show a flow chart in EW0 mode when the suspend function is enabled, and Figure 30.13 shows Suspend Operation Example in EW0 Mode.



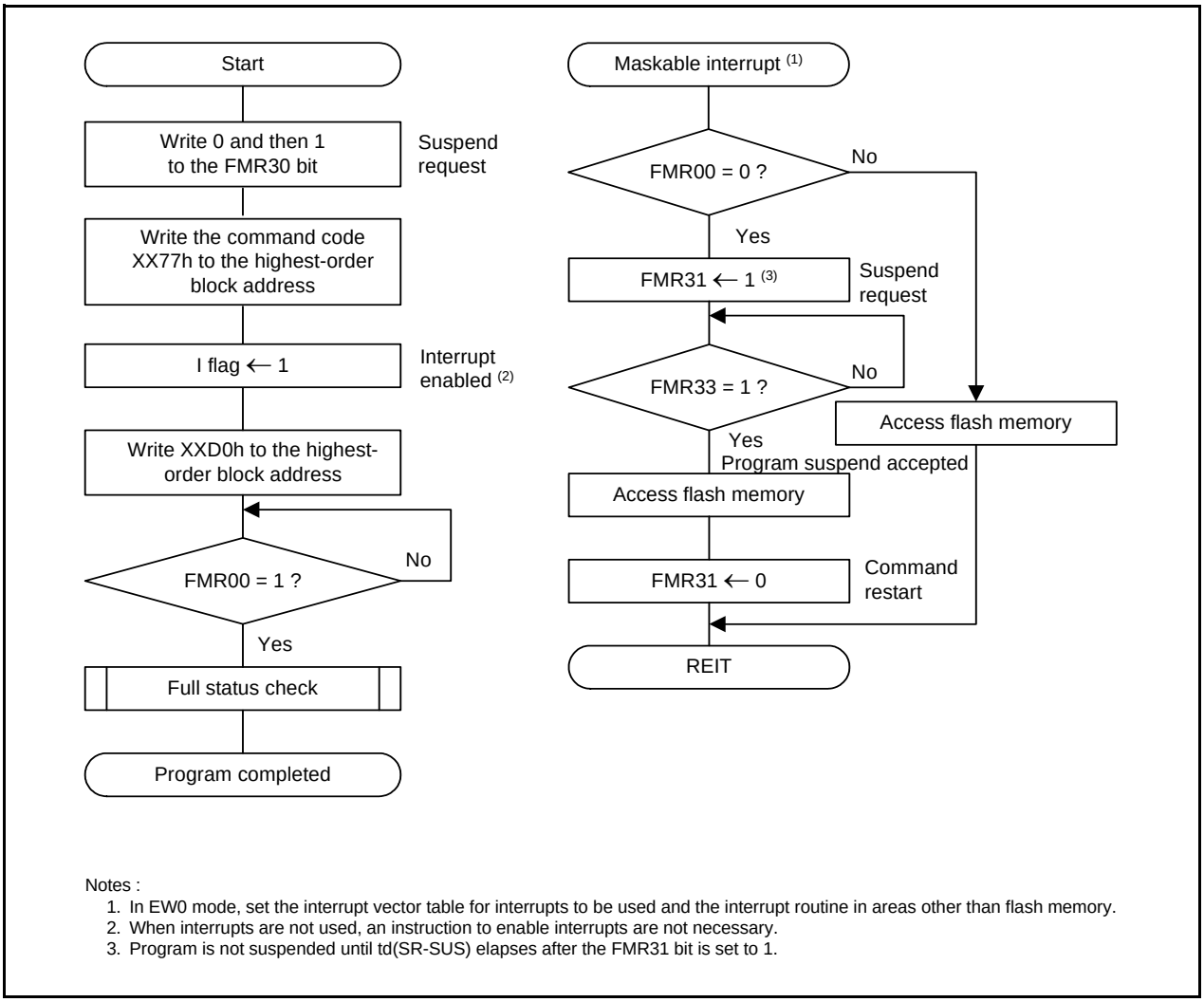
Notes :
1. In EW0 mode, set the interrupt vector table for interrupts to be used and the interrupt routine in areas other than flash memory.
2. When interrupts are not used, an instruction to enable interrupts are not necessary.
3. Program is not suspended until td(SR-SUS) elapses after the FMR31 bit is set to 1.

Figure 30.10 Program Flowchart in EW0 Mode (Suspend Function Enabled)



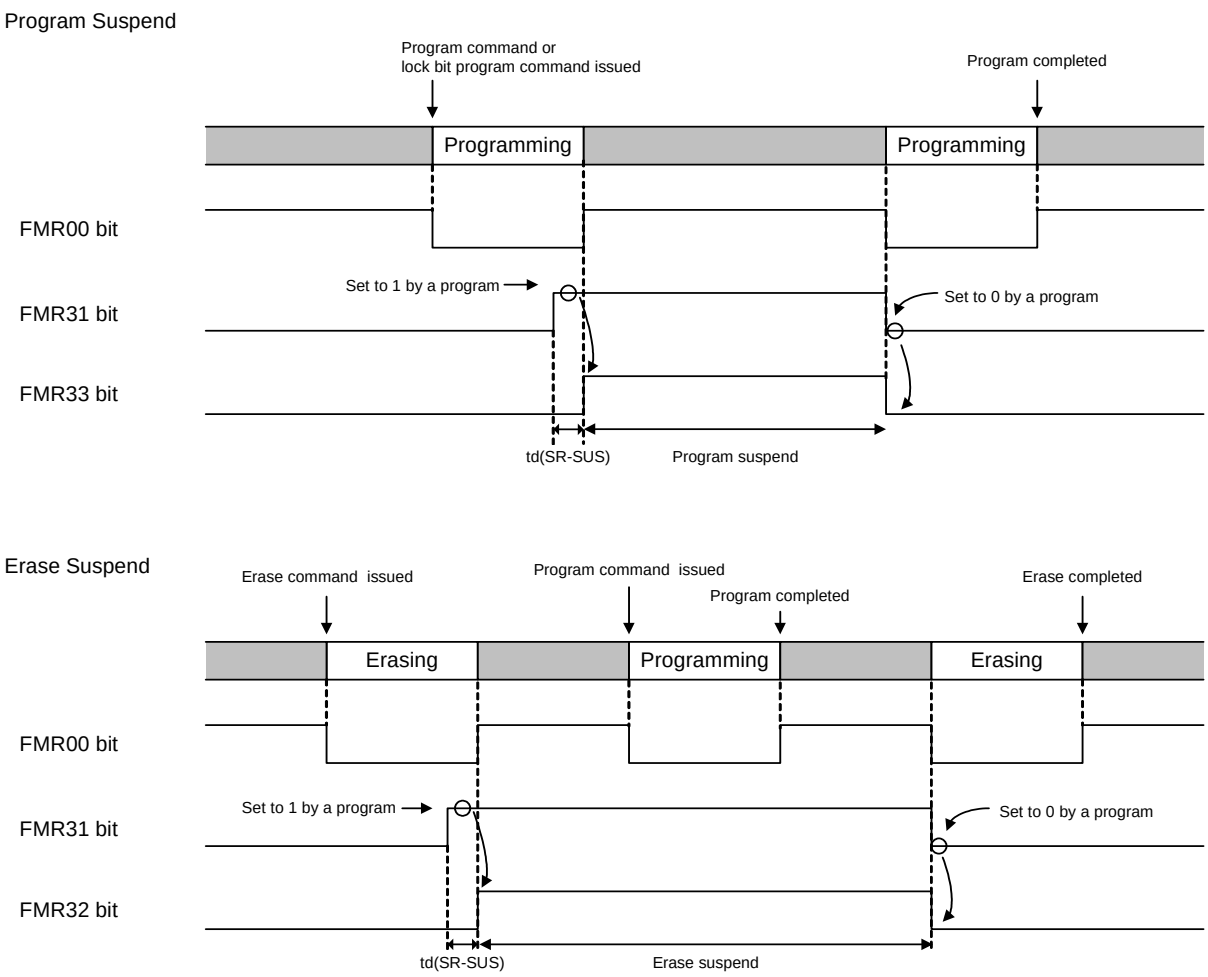
Notes :
1. In EW0 mode, set the interrupt vector table for interrupts to be used and the interrupt routine in areas other than flash memory.
2. When interrupts are not used, an instruction to enable interrupts are not necessary.
3. Erase is not suspended until td(SR-SUS) elapses after the FMR31 bit is set to 1.

Figure 30.11 Block Erase Flowchart in EW0 Mode (Suspend Function Enabled)



Notes :
1. In EW0 mode, set the interrupt vector table for interrupts to be used and the interrupt routine in areas other than flash memory.
2. When interrupts are not used, an instruction to enable interrupts are not necessary.
3. Program is not suspended until td(SR-SUS) elapses after the FMR31 bit is set to 1.

Figure 30.12 Lock Bit Program Flowchart in EW0 Mode (Suspend Function Enabled)



FMR00 : Bit in the FMR0 register
FMR33, FMR32, FMR31 : Bits in the FMR3 register

The above diagram applies under the following condition.
- The FMR30 bit in the FMR3 register is 1 (suspend enabled).

Figure 30.13 Suspend Operation Example in EW0 Mode

30.8.7 EW1 Mode

EW1 mode is selected by setting the FMR60 bit to 1 after setting the FMR01 bit to 1. Figure 30.14 shows Setting and Resetting of EW1 Mode.
The FMR0 register indicates whether or not a program or erase operation has completed as expected. The status register cannot be read in EW1 mode.
When a program or erase operation is initiated, the CPU halts all program execution until the operation is completed.

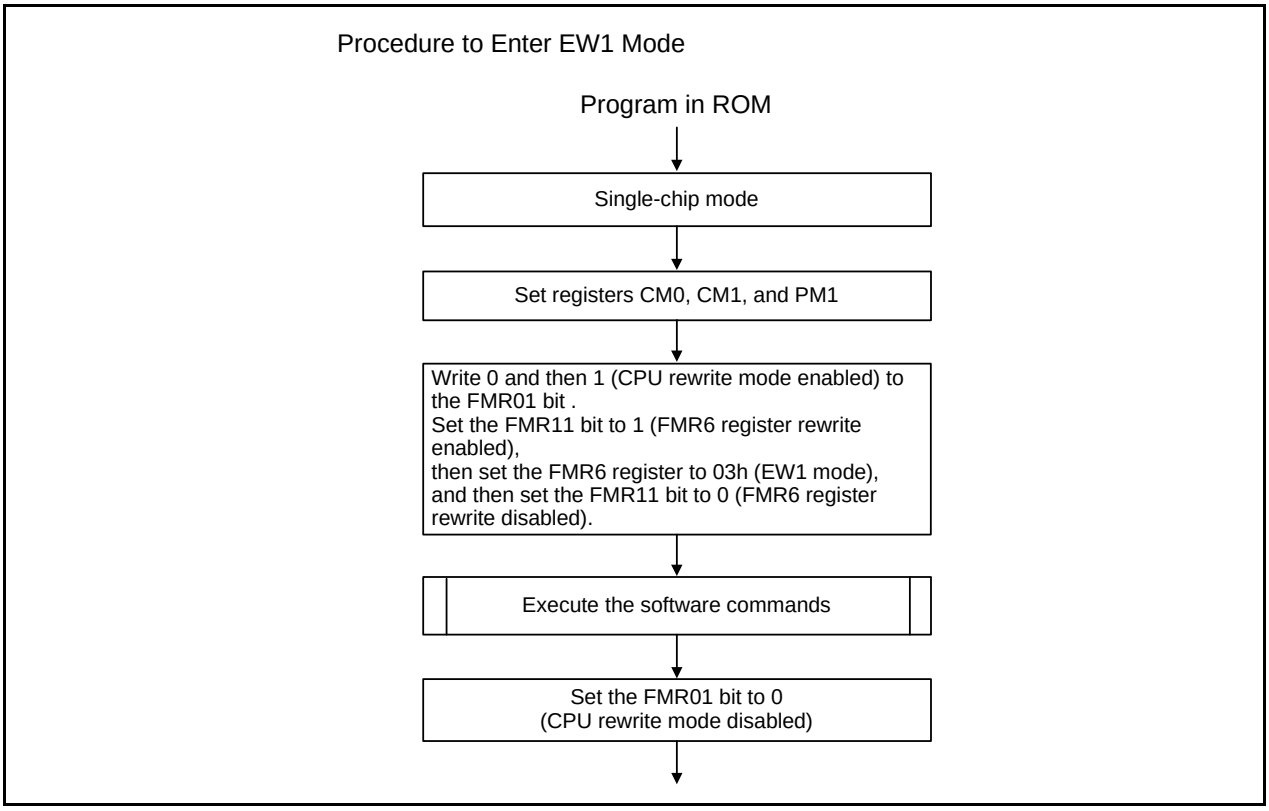


Figure 30.14 Setting and Resetting of EW1 Mode

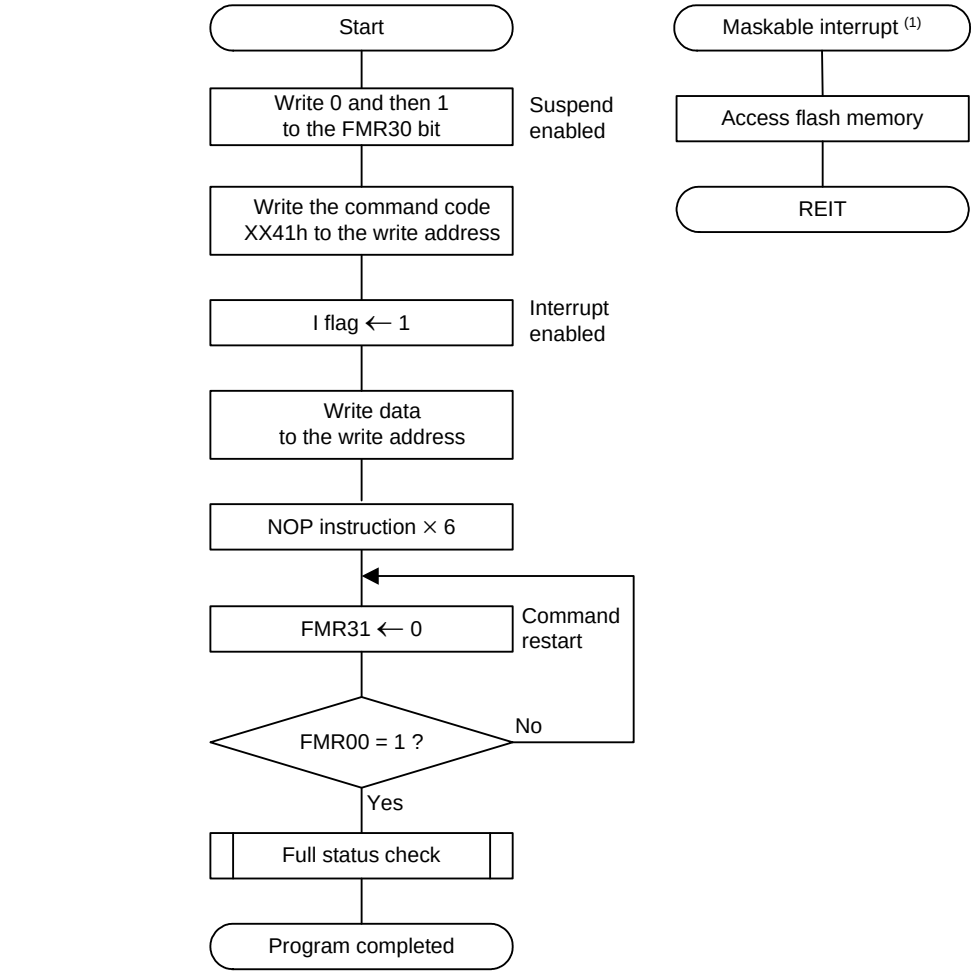
The following are interrupts which can be used in EW1 mode and operations when the interrupts occur during auto-erase operation or auto-program operation:

- Maskable interrupt (suspend function enabled)
  Auto-erase operation or auto-program operation suspends after td(SR-SUS) elapses and the interrupt process is executed. Auto-erase operation or auto-program operation restarts by setting the FMR31 bit in the FMR3 register to 0 (command restart) after the interrupt process is completed.
- Maskable interrupt (suspend function disabled)
  Auto-erase operation or auto-program operation has a higher priority level and the interrupt request has to wait. The interrupt process is executed after auto-erase operation or auto-program operation is completed.
- $\overline{\text{NMI}}$, watchdog timer, oscillation stop/re-oscillation detect, voltage detect 1, and voltage detect 2 interrupts
  Auto-erase operation or auto-program operation forcibly stops as soon as the interrupt occurs, and the flash memory is reset. The flash memory restarts after a certain period of time, and then the interrupt process starts.
  After the flash memory restart, execute auto-erase operation again and confirm that it is completed as expected in order to read the correct value.

The watchdog timer stops its counting during auto-erasure or auto-programming, but counts during erase suspend or program suspend. The interrupt request can be generated. Initialize the watchdog timer regularly by using the suspend function.

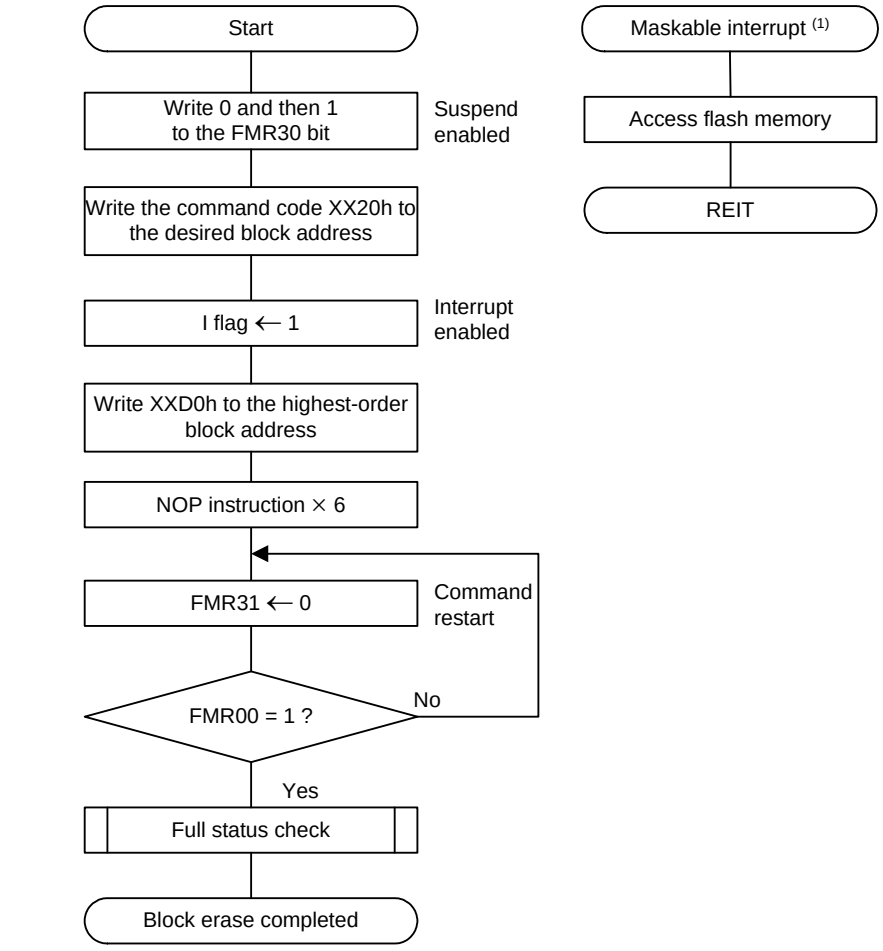
30.8.7.1 Suspend Function (EW1 Mode) (under review)

When using suspend function in EW1 mode, an interrupt request is not accepted until td(SR-SUS) elapses after the interrupt request is generated. When the interrupt request is accepted, the flash memory enters erase suspend or program suspend. Set the FMR31 bit to 0 (command restart) to restart automatic program and erase operations at the completion of the interrupt. Figure 30.15 to Figure 30.17 show a flowchart in EW1 mode when the suspend function is enabled, and Figure 30.18 shows Suspend Operation Example in EW1 Mode.



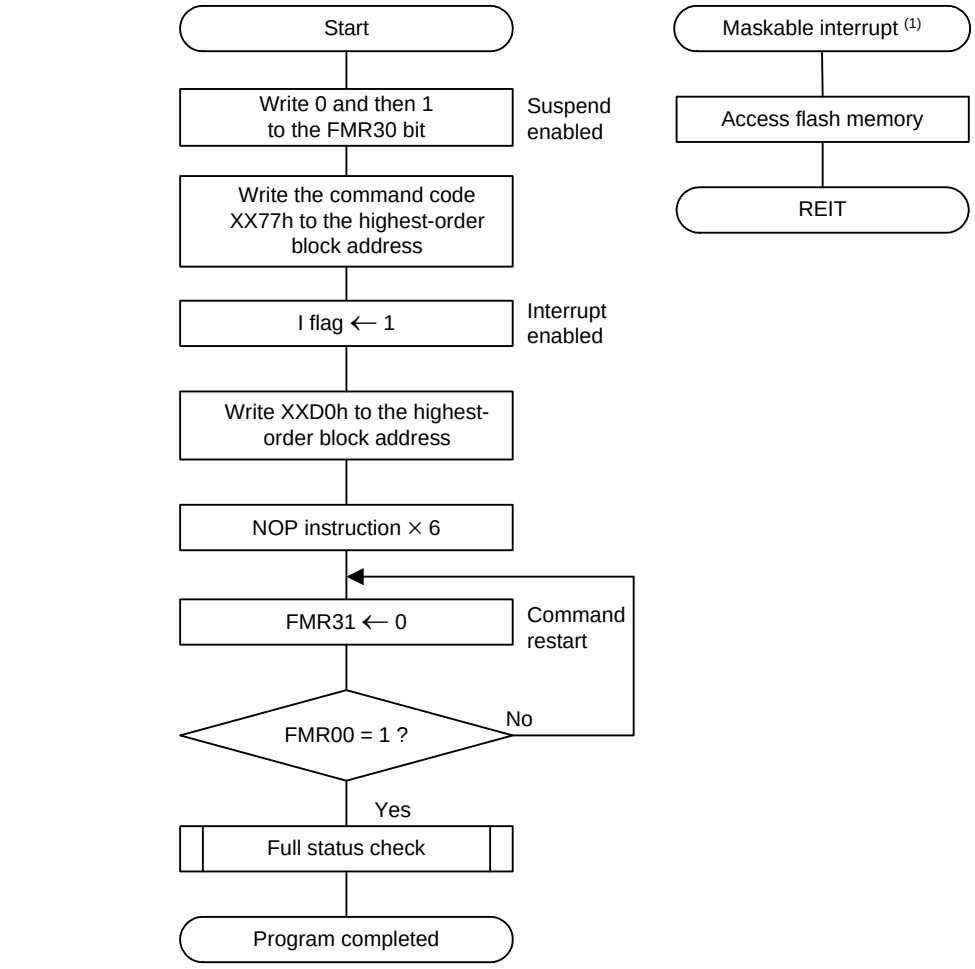
Note :
1. An interrupt request is not accepted until td(SR-SUS) elapses after the interrupt request is generated. Enable interrupts used to enter suspend mode beforehand.

Figure 30.15 Program Flowchart in EW1 Mode (Suspend Function Enabled)



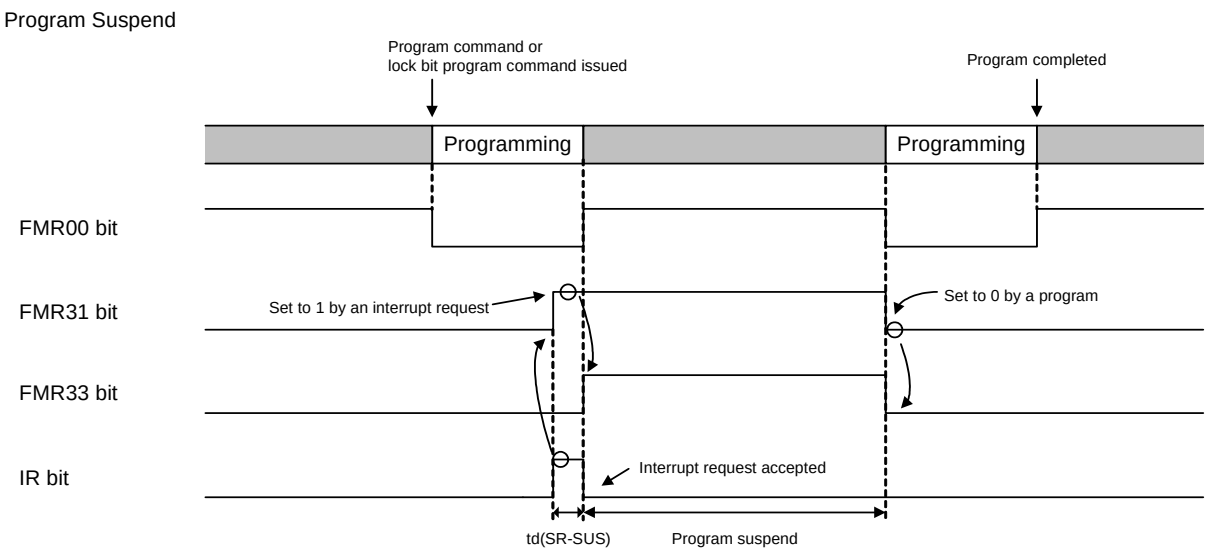
Note :
1. An interrupt request is not accepted until td(SR-SUS) elapses after the interrupt request is generated. Enable interrupts used to enter suspend mode beforehand.

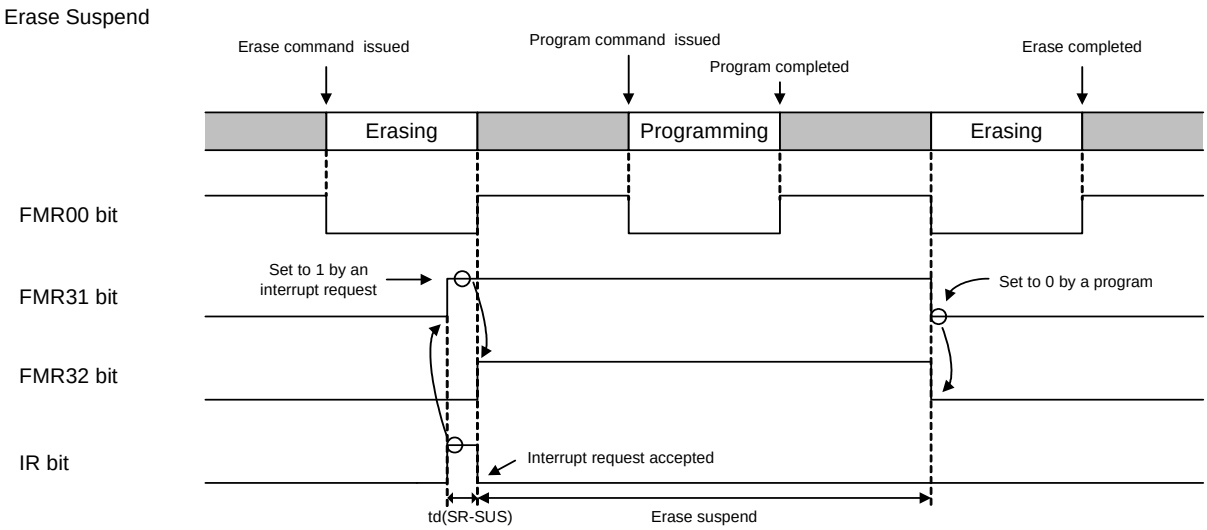
Figure 30.16 Block Erase Flowchart in EW1 Mode (Suspend Function Enabled)



Note :
1. An interrupt request is not accepted until td(SR-SUS) elapses after the interrupt request is generated. Enable interrupts used to enter suspend mode beforehand.

Figure 30.17 Lock Bit Program Flowchart in EW1 Mode (Suspend Function Enabled)





FMR00 : Bit in the FMR0 register
FMR33, FMR32, FMR31 : Bits in the FMR3 register
IR : Interrupt control register to enter suspend mode

The above diagram applies under the following condition.
- The FMR30 bit in the FMR3 register is 1 (suspend enabled).

Figure 30.18 Suspend Operation Example in EW1 Mode

30.9 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer supporting the M16C/65 Group can be used to rewrite program ROM 1, program ROM 2, and data flash while the MCU mounted on a board.
Standard serial I/O mode has the following two modes:

- Standard serial I/O mode 1: The MCU is connected to the serial programmer by using clock synchronous serial I/O
- Standard serial I/O mode 2: The MCU is connected to the serial programmer by using two-wire clock asynchronous serial I/O

For more information about the serial programmers, contact the serial programmer manufacturer. Refer to the user's manual included with your serial programmer for instructions.

30.9.1 ID Code Check Function

Use the ID code check function in standard serial I/O mode. This function determines whether the ID codes sent from the serial programmer match those written in the flash memory. If the ID codes do not match, commands sent from the serial programmer are not accepted. However, if the four bytes of the reset vector are “FFFFFFFFh”, ID codes are not compared, allowing all commands to be accepted.
The ID codes are 7-byte data stored consecutively, starting with the first byte, at addresses 0FFFDFh, 0FFFE3h, 0FFFEBh, 0FFFEFh, 0FFFF3h, 0FFFF7h, and 0FFFFBh. The flash memory must have a program with the ID codes set in these addresses. Figure 30.19 shows ID Code Storage Addresses.
The ID code of “ALeRASE” in ASCII code is used for forced erase function. The ID code of “Protect” in ASCII code is used for standard serial I/O mode disable function. Table 30.17 lists Reserved Word of ID Code. All ID code storage addresses and data must match the combinations listed in Table 30.17. When the forced erase function or standard serial I/O mode disable function is not used, use another combination of ID codes.

Table 30.17 Reserved Word of ID Code

ID Code Storage Address		Reserved word of ID Code (ASCII)	
		ALeRASE	Protect
FFFDFh	ID1	41h (upper-case A)	50h (upper-case P)
FFFE3h	ID2	4Ch (upper-case L)	72h (lower-case r)
FFFEBh	ID3	65h (lower-case e)	6Fh (lower-case o)
FFFEFh	ID4	52h (upper-case R)	74h (lower-case t)
FFFF3h	ID5	41h (upper-case A)	65h (lower-case e)
FFFF7h	ID6	53h (upper-case S)	63h (lower-case c)
FFFFBh	ID7	45h (upper-case E)	74h (lower-case t)

All ID code storage addresses and data must match the combinations listed in Table 30.17.

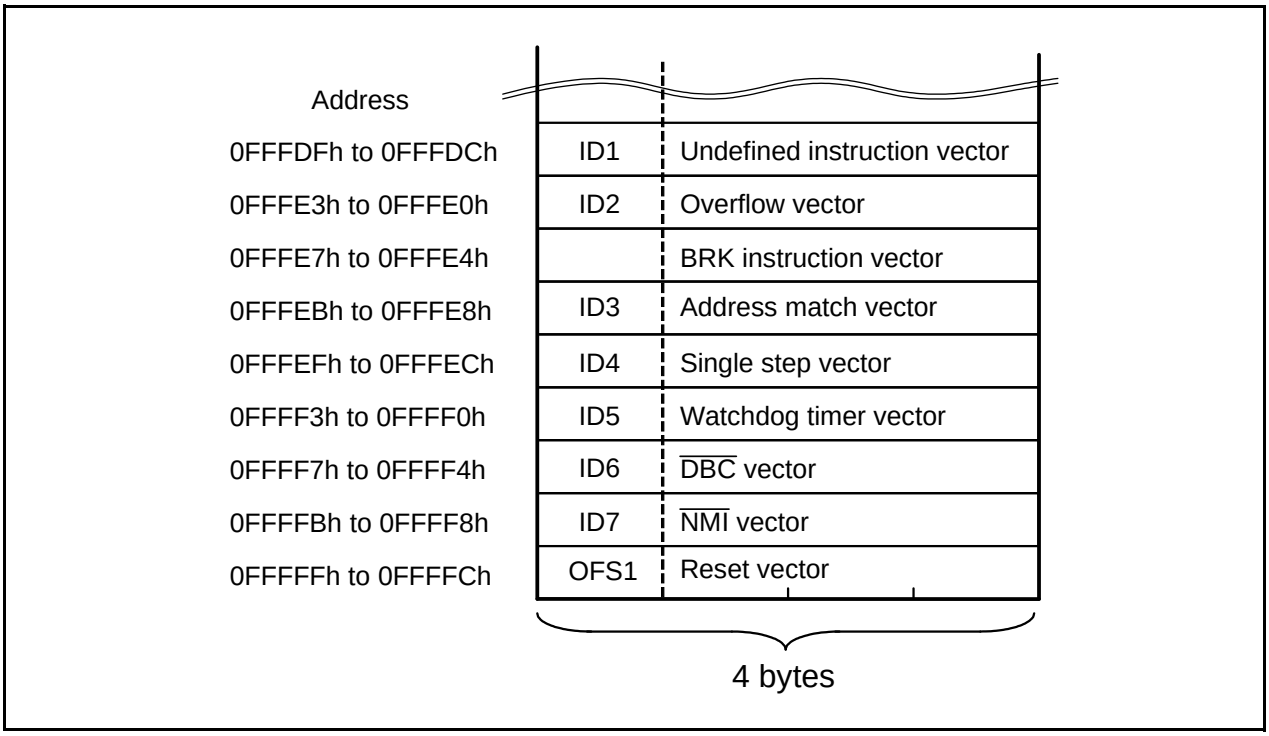


Figure 30.19 ID Code Storage Addresses

30.9.2 Forced Erase Function

Use the forced erase function in standard serial I/O mode. When the reserved word, “ALeRASE” in ASCII code, are sent from the serial programmer as ID codes, the contents of program ROM 1 and program ROM 2 will be erased at once. However, if the ID codes stored in the ID code storage addresses are set to other than a reserved word “ALeRASE” (other than the combination table listed in Table 30.17) when the ROMCP1 bit in the OFS1 address is set to 0 (ROM code protect enabled), forced erase function is ignored and ID code check is executed by ID code check function. Table 30.18 lists conditions and functions for forced erase function.

When both the ID codes sent from the serial programmer and the ID codes stored in the ID code storage addresses correspond to the reserved word “ALeRASE”, program ROM 1 and program ROM 2 will be erased. However, when the serial programmer sends other than “ALeRASE”, even if the ID codes stored in the ID code storage addresses are “ALeRASE”, there is no ID match and any command is ignored. The flash memory cannot be operated.

Table 30.18 Forced Erase Function

Condition			Function
ID code from serial programmer	Code in ID code storage address	ROMCP1 bit in the OFS1 address	
ALeRASE	ALeRASE	–	Program ROM 1 and program ROM 2 all erase (forced erase function)
	Other than ALeRASE (1)	1 (ROM code protect disabled)	
		0 (ROM code protect enabled)	ID code check (ID code check function)
Other than ALeRASE	ALeRASE	–	ID code check (ID code check function. No ID match)
	Other than ALeRASE (1)	–	ID code check (ID code check function)

Note:
1. For the combination of the stored addresses is “Protect”, refer to 30.9.3 “Standard Serial I/O Mode Disable Function”.

30.9.3 Standard Serial I/O Mode Disable Function

Use the standard serial I/O mode disable function in standard serial I/O mode. When the ID codes in the ID code stored addresses are set to “Protect” in ASCII code (refer to Table 30.17 “Reserved Word of ID Code”), the MCU does not communicate with the serial programmer. Therefore, the flash memory cannot be read, written or erased by the serial programmer. User boot mode can be selected, when the ID codes are set to “Protect”.

When the ID codes are set to “Protect” and the ROMCP1 bit in the OFS1 address is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled by the serial programmer. Therefore, the flash memory cannot be read, written or erased by the serial or parallel programmer.

30.9.4 Standard Serial I/O Mode 1

In standard serial I/O mode 1, a serial programmer is connected to the MCU by using clock synchronous serial I/O.

Table 30.19 lists Pin Functions (Flash Memory Standard Serial I/O Mode 1) and Table 30.20 lists Setting of Standard Serial I/O Mode 1.

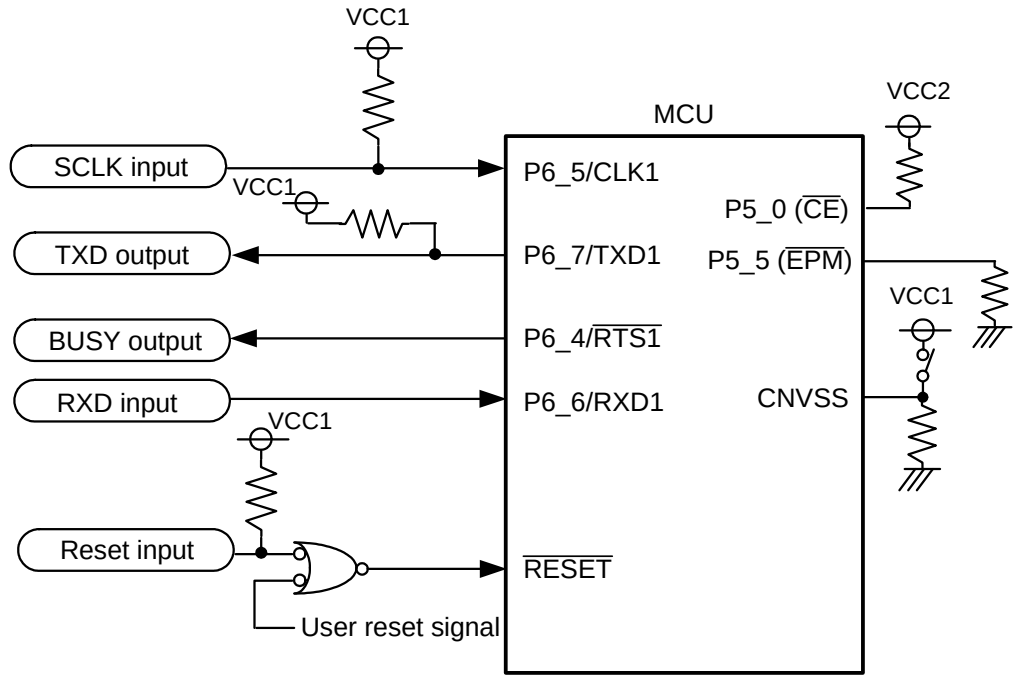
Figure 30.20 shows Circuit Application in Standard Serial I/O Mode 1. Control pins vary by programmer. For more information, refer to the programmer manual.

Table 30.19 Pin Functions (Flash Memory Standard Serial I/O Mode 1)

Pin	Name	I/O	Power Supply	Description
VCC1, VCC2, VSS	Power input		-	Apply the flash program and erase voltage to the VCC1 pin, and VCC2 to the VCC2 pin. The VCC application condition is that VCC2 ≤ VCC1. Apply 0 V to the VSS pin.
CNVSS	CNVSS	I	VCC1	Connect to the VCC1 pin.
$\overline{\text{RESET}}$	Reset input	I	VCC1	Reset input pin. During td(OCOS), input a low-level signal to the $\overline{\text{RESET}}$ pin.
XIN	Clock input	I	VCC1	Input a high-level signal to the XIN pin and open the XOUT pin when a main clock is not used. Connect a ceramic resonator or crystal oscillator between pins XIN and XOUT when the main clock is used. To input an externally generated clock, input it to the XIN pin and open the XOUT pin.
XOUT	Clock output	O		
BYTE	BYTE input	I	VCC1	Connect this pin to VSS or VCC1.
AVCC, AVSS	Analog power supply input			Connect AVCC to VCC1 and AVSS to VSS, respectively.
VREF	Reference voltage input	I		Reference voltage input pin for A/D converter.
P0_0 to P0_7	Input port P0	I	VCC2	Input a high- or low-level signal or leave open.
P1_0 to P1_7	Input port P1	I	VCC2	Input a high- or low-level signal or leave open.
P2_0 to P2_7	Input port P2	I	VCC2	Input a high- or low-level signal or leave open.
P3_0 to P3_7	Input port P3	I	VCC2	Input a high- or low-level signal or leave open.
P4_0 to P4_7	Input port P4	I	VCC2	Input a high- or low-level signal or leave open.
P5_1 to P5_4, P5_6, P5_7	Input port P5	I	VCC2	Input a high- or low-level signal or leave open.
P5_0	$\overline{\text{CE}}$ input	I	VCC2	Input a high-level signal.
P5_5	$\overline{\text{EPM}}$ input	I	VCC2	Input a low-level signal.
P6_0 to P6_3	Input port P6	I	VCC1	Input a high- or low-level signal or leave open.
P6_4 / $\overline{\text{RTS1}}$	BUSY output	O	VCC1	BUSY signal output pin
P6_5/CLK1	SCLK input	I	VCC1	Serial clock input pin
P6_6 / RXD1	RXD input	I	VCC1	Serial data input pin.
P6_7 / TXD1	TXD output	O	VCC1	Serial data output pin.
P7_0 to P7_7	Input port P7	I	VCC1	Input a high- or low-level signal or leave open.
P8_0 to P8_7	Input port P8	I	VCC1	Input a high- or low-level signal or leave open.
P9_0 to P9_7	Input port P9	I	VCC1	Input a high- or low-level signal or leave open.
P10_0 to P10_7	Input port P10	I	VCC1	Input a high- or low-level signal or leave open.
P11_0 to P11_7	Input port P11	I	VCC1	Input a high- or low-level signal or leave open.
P12_0 to P12_7	Input port P12	I	VCC2	Input a high- or low-level signal or leave open.
P13_0 to P13_7	Input port P13	I	VCC2	Input a high- or low-level signal or leave open.
P14_0 to P14_1	Input port P14	I	VCC1	Input a high- or low-level signal or leave open.

Table 30.20 Setting of Standard Serial I/O Mode 1

Signal	Input Level
CNVSS	VCC1
$\overline{EPM}$	VSS
$\overline{RESET}$	VSS → VCC1
$\overline{CE}$	VCC2
SCLK	VCC1



Notes:
1. Control pins and external circuitry will vary depending on the programmer. For more information, refer to the programmer manual.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the CNVSS input with a switch.
3. If in standard serial I/O mode 1 there is a possibility that the user reset signal will go low during serial I/O mode, break the connection between the user reset signal and $\overline{RESET}$ pin by using, for example, a jumper switch.

Figure 30.20 Circuit Application in Standard Serial I/O Mode 1

30.9.5 Standard Serial I/O Mode 2

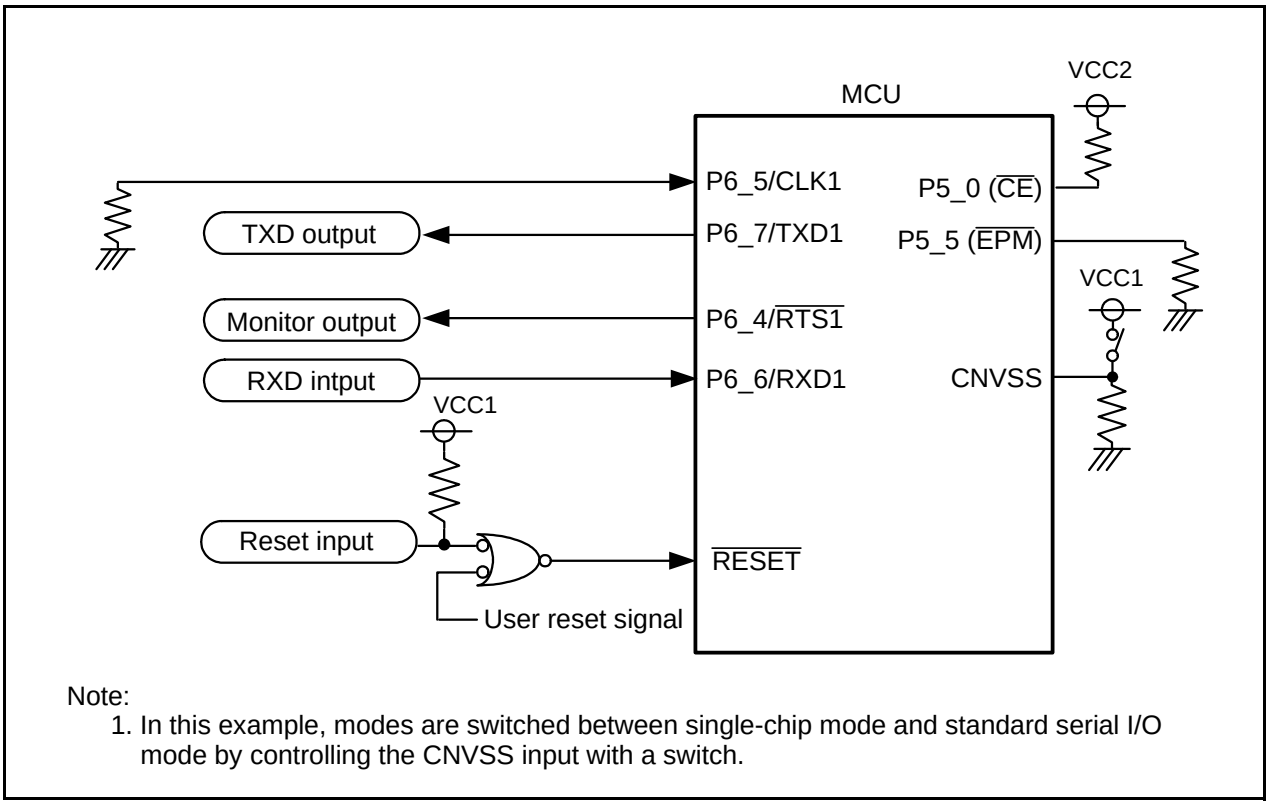
In standard serial I/O mode 2, a serial programmer is connected to the MCU by using two-wire clock asynchronous serial I/O.
Table 30.21 lists Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Table 30.22 lists Setting of Standard Serial I/O Mode 2.
Figure 30.21 shows Circuit Application in Standard Serial I/O Mode 2. Control pins vary by programmer. For more information, refer to the programmer manual.

Table 30.21 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Power Supply	Description
VCC1, VCC2, VSS	Power input		-	Apply the flash program and erase voltage to the VCC1 pin, and VCC2 to the VCC2 pin. The VCC application condition is that VCC2 ≤ VCC1. Apply 0 V to the VSS pin.
CNVSS	CNVSS	I	VCC1	Connect to the VCC1 pin.
$\overline{\text{RESET}}$	Reset input	I	VCC1	Reset input pin. During td(OCOS), input a low-level signal to the $\overline{\text{RESET}}$ pin.
XIN	Clock input	I	VCC1	Input a high-level signal to the XIN pin and open the XOUT pin when a main clock is not used. Connect a ceramic resonator or crystal oscillator between pins XIN and XOUT when the main clock is used. To input an externally generated clock, input it to the XIN pin and open the XOUT pin.
XOUT	Clock output	O	VCC1	
BYTE	BYTE input	I	VCC1	Connect this pin to VSS or VCC1.
AVCC, AVSS	Analog power supply input			Connect AVCC to VCC1 and AVSS to VSS, respectively.
VREF	Reference voltage input	I		Reference voltage input pin for A/D converter.
P0_0 to P0_7	Input port P0	I	VCC2	Input a high- or low-level signal or leave open.
P1_0 to P1_7	Input port P1	I	VCC2	Input a high- or low-level signal or leave open.
P2_0 to P2_7	Input port P2	I	VCC2	Input a high- or low-level signal or leave open.
P3_0 to P3_7	Input port P3	I	VCC2	Input a high- or low-level signal or leave open.
P4_0 to P4_7	Input port P4	I	VCC2	Input a high- or low-level signal or leave open.
P5_1 to P5_4, P5_6, P5_7	Input port P5	I	VCC2	Input a high- or low-level signal or leave open.
P5_0	$\overline{\text{CE}}$ input	I	VCC2	Input a high-level signal.
P5_5	$\overline{\text{EPM}}$ input	I	VCC2	Input a low-level signal.
P6_0 to P6_3	Input port P6	I	VCC1	Input a high- or low-level signal or leave open.
P6_4 / $\overline{\text{RTS1}}$	BUSY output	O	VCC1	Monitor signal output pin for checking the boot program operation.
P6_5/CLK1	SCLK input	I	VCC1	Input a low-level signal
P6_6 / RXD1	RXD input	I	VCC1	Serial data input pin.
P6_7 / TXD1	TXD output	O	VCC1	Serial data output pin.
P7_0 to P7_7	Input port P7	I	VCC1	Input a high- or low-level signal or leave open.
P8_0 to P8_7	Input port P8	I	VCC1	Input a high- or low-level signal or leave open.
P9_0 to P9_7	Input port P9	I	VCC1	Input a high- or low-level signal or leave open.
P10_0 to P10_7	Input port P10	I	VCC1	Input a high- or low-level signal or leave open.
P11_0 to P11_7	Input port P11	I	VCC1	Input a high- or low-level signal or leave open.
P12_0 to P12_7	Input port P12	I	VCC2	Input a high- or low-level signal or leave open.
P13_0 to P13_7	Input port P13	I	VCC2	Input a high- or low-level signal or leave open.
P14_0 to P14_1	Input port P14	I	VCC1	Input a high- or low-level signal or leave open.

Table 30.22 Setting of Standard Serial I/O Mode 2

Signal	Input Level
CNVSS	VCC1
$\overline{\text{EPM}}$	VSS
$\overline{\text{RESET}}$	VSS → VCC1
$\overline{\text{CE}}$	VCC2
P6_5/CLK1	VSS



Note:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the CNVSS input with a switch.

Figure 30.21 Circuit Application in Standard Serial I/O Mode 2

30.9.6 Parallel I/O Mode

In parallel I/O mode, program ROM 1, program ROM 2, and data flash can be rewritten using a parallel programmer supporting the M16C/65 Group. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.

30.9.6.1 ROM Code Protect Function

The ROM code protect function inhibits the flash memory from being read or rewritten during parallel I/O mode. Refer to 30.4 "Optional Function Select Address 1 (OFS1)". The OFS1 address is located in block 0 in program ROM 1.

The ROM code protect function is enabled when the ROMCP1 bit is set to 0.

To cancel ROM code protect, erase block 0 including the OFS1 address using standard serial I/O mode or CPU rewrite mode.

30.10 Notes on Flash Memory

30.10.1 Functions to Prevent Flash Memory from Being Rewritten

Addresses 0FFFDFh, 0FFFE3h, 0FFFEBh, 0FFFEFh, 0FFFF3h, 0FFFF7h, and 0FFFFBh store ID codes. When the wrong data is written to these addresses, the flash memory is prevented from being read or written in standard serial I/O mode.
0FFFFFh is OFS1 address. When the wrong data is written to this address, the flash memory is prevented from being read or written in parallel I/O mode.
These addresses correspond to the vector address (H) in fixed vector.

30.10.2 Reading of Data Flash

When 2.7 V ≤ VCC1 ≤ 3.0 V and f(BCLK) ≥ 16 MHz, or 3.0 V < VCC1 ≤ 5.5 V and f(BCLK) ≥ 20 MHz, one wait state is necessary to execute the program on the data flash and read the data. Use the PM17 in the PM1 register or FMR17 bit in the FMR1 register to set one wait state.

30.10.3 CPU Rewrite Mode

30.10.3.1 Operating Speed

Set a CPU clock frequency of 10 MHz or less by the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to 1 (wait state).

30.10.3.2 Prohibited Instructions

Do not use the following instructions in EW0 mode:
UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

30.10.3.3 Interrupts (EW0 Mode and EW1 Mode)

- Do not use an address match interrupt during command execution because the address match interrupt vector is located in ROM.
- Do not use a non-maskable interrupt during block 0 erasure because fixed vector is located in block 0.

30.10.3.4 Rewrite (EW0 Mode)

If the power supply voltage drops while rewriting the block where the rewrite control program is stored, the rewrite control program is not correctly rewritten. This may prevent the flash memory from being rewritten. If this error occurs, use standard serial I/O mode or parallel I/O mode for rewriting.

30.10.3.5 Rewrite (EW1 Mode)

Do not rewrite any blocks in which the rewrite control program is stored.

30.10.3.6 DMA transfer

In EW1 mode, do not generate a DMA transfer while the FMR00 bit in the FMR0 register is set to 0 (auto programming or auto erasing).

30.10.3.7 Wait Mode

To enter wait mode, set the FMR01 bit to 0 (CPU rewrite mode disabled) before executing the WAIT instruction.

30.10.3.8 Stop Mode

To enter stop mode, set the FMR01 bit to 0 (CPU rewrite mode disabled), and then disable DMA transfer before setting the CM10 bit to 1 (stop mode).

30.10.3.9 Low Power Mode and On-Chip Oscillator Low Power Mode

When the CM05 bit is set to 1 (main clock stopped), do not execute the following commands:

- Program
- Block erase
- Lock bit program
- Read lock bit status
- Block blank check

30.10.3.10 PM13 Bit

The PM13 bit in the PM1 register becomes 1 while the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled). The PM13 bit returns to the former value by setting the FMR01 bit to 0 (CPU rewrite mode disabled). When the PM13 bit is changed during CPU rewrite mode, the value of the PM13 bit after being changed is not reflected until the FMR01 bit is set to 0.

30.10.3.11 Area Where Rewrite Control Program is Executed

Bits PM10 and PM13 in the PM1 register become 1 in CPU rewrite mode. Execute the rewrite program in internal RAM or an external area which can be used when both bits PM10 and PM13 are 1. Do not use the area (40000h to BFFFFh) where accessible space is expanded when the PM13 bit is 0 and 4-Mbyte mode is set.

30.10.3.12 Program and Erase Cycles and Execution Time

Execution time of program, block erase and lock bit program command becomes longer as the number of programming and erasing increases.

30.10.3.13 Suspend of Auto-Erase Operation and Auto-Program Operation

When program, block erase, and lock bit program commands are suspended, the blocks for those commands must be erased. Execute program and lock bit program commands again after erasing. Those commands are suspended by the following reset or interrupts:

- Reset
- $\overline{\text{NMI}}$, watchdog timer, oscillation stop/re-oscillation detection, voltage monitor 1, and voltage monitor 2 interrupts.

30.10.4 Standard Serial I/O Mode

30.10.4.1 User Boot Mode

To use user boot mode after standard serial I/O mode, turn off the power when exiting standard serial I/O mode, and then turn on the power again (cold start). The MCU enters user boot mode under the right conditions.

31. Precautions

31.1 OFS1 Address and ID Code Storage Address

OFS1 address and ID code storage address are part of flash memory. When writing a program to flash memory, write an appropriate value to those addresses simultaneously.

In the OFS1 address, the MCU state after reset and the function to prevent rewrite in parallel I/O mode are selected. The OFS1 address is 0FFFFFh. This is the most significant address of block 0 in program ROM and upper address of reset vector. Also, the ID code storage address is in block 0 and upper address of interrupt vector.

When using a compiler to create a program, the reset vector of interrupt vector is created by the compiler and the OFS1 address or ID code storage address becomes FFh. Write the appropriate value to those addresses separately. The following is an example when writing to the OFS1 address by an assembler.

ex) Set FEh to the OFS1 address

When using an address control instruction and logical addition:

```
.org 0FFFCh
RESET:
.lword start | 0FE000000h
```

When using an address control instruction:

```
.org 0FFFCh
RESET:
.addr start
.byte 0FEh
```

31.2 Notes on Noise

Connect a bypass capacitor (approximately 0.1 µF) across pins VCC1 and VSS, and pins VCC2 and VSS using the shortest and thicker possible wiring. Figure 31.1 shows the Bypass Capacitor Connection.

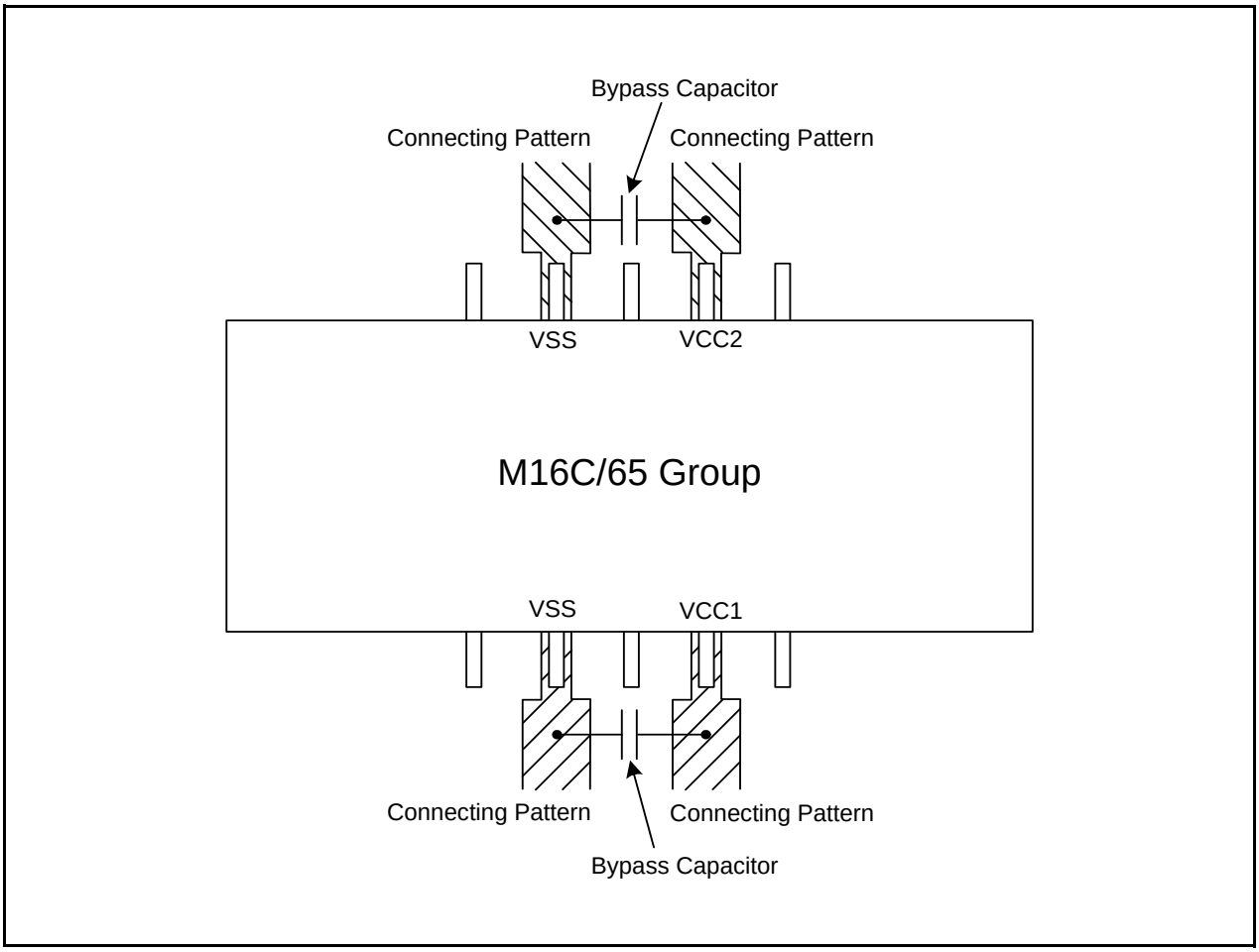


Figure 31.1 Bypass Capacitor Connection

31.3 Notes on SFRs

31.3.1 Register Settings

Table 31.1 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.

Table 31.1 Registers with Write-Only Bits

Register	Symbol	Address
Watchdog Timer Reset Register	WDTR	037Dh
Watchdog Timer Start Register	WDTS	037Eh
Timer A0 Register	TA0	0327h to 0326h
Timer A1 Register	TA1	0329h to 0328h
Timer A2 Register	TA2	032Bh to 032Ah
Timer A3 Register	TA3	032Dh to 032Ch
Timer A4 Register	TA4	032Fh to 032Eh
Timer A1-1 Register	TA11	0303h to 0302h
Timer A2-1 Register	TA21	0305h to 0304h
Timer A4-1 Register	TA41	0307h to 0306h
Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
Dead Time Timer	DTT	030Ch
Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	030Dh
UART0 Bit Rate Register	U0BRG	0249h
UART1 Bit Rate Register	U1BRG	0259h
UART2 Bit Rate Register	U2BRG	0269h
UART5 Bit Rate Register	U5BRG	0289h
UART6 Bit Rate Register	U6BRG	0299h
UART7 Bit Rate Register	U7BRG	02A9h
UART0 Transmit Buffer Register	U0TB	024Bh to 024Ah
UART1 Transmit Buffer Register	U1TB	025Bh to 025Ah
UART2 Transmit Buffer Register	U2TB	026Bh to 026Ah
UART5 Transmit Buffer Register	U5TB	028Bh to 028Ah
UART6 Transmit Buffer Register	U6TB	029Bh to 029Ah
UART7 Transmit Buffer Register	U7TB	02ABh to 02AAh
SI/O3 Bit Rate Register	S3BRG	0273h
SI/O4 Bit Rate Register	S4BRG	0277h
I2C0 Control Register 1	S3D0	02B6h
I2C0 Status Register 0	S10	02B8h

31.4 Notes on Protection

After setting the PRC2 bit to 1 (write enabled), by writing to a given SFR, the PRC2 bit becomes 0. Change the registers protected by the PRC2 bit in the next instruction after setting the PRC2 bit to 1. Make sure there are no interrupts or DMA transfers between the instruction that sets the PRC2 bit to 1 and the next instruction.

31.5 Notes on Resets

31.5.1 Power Supply Rising Gradient

When supplying power to the MCU, make sure that the power supply voltage applied to the VCC1 pin meets the SVCC conditions.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
SVCC	Power supply rising gradient (VCC1) (Voltage range: 0 to 2)	0.05			V/ms

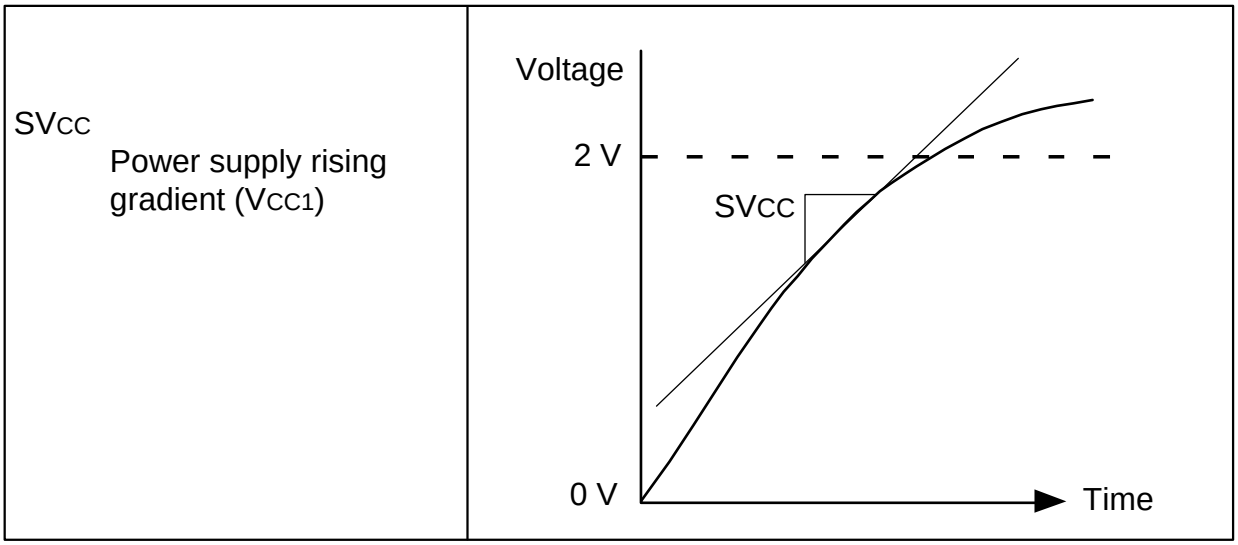


Figure 31.2 Timing of SVcc

31.5.2 Power-On Reset

Use the voltage monitor 0 reset together with the power-on reset. To use power-on reset, set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset). In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1, and the VC25 bit in the VCR2 register is 1) after power-on reset. Do not disable the bits by a program.

31.5.3 OSDR Bit (Oscillation Stop Detection Reset Detection Flag)

When the oscillation stop detection reset is generated, the MCU is reset and then stopped. This state is canceled by hardware reset or voltage monitor 0 reset.

Note that the OSDR bit remains unchanged at hardware reset, but is set to 0 (not detected) at voltage monitor 0 reset.

31.6 Notes on Clock Generator

31.6.1 Oscillation Circuit Using an Oscillator

To connect an oscillator, follow these instructions:

- The oscillation characteristics are tied closely to the user's board design. Perform a careful evaluation of the board before connecting an oscillator.
- Oscillation circuit structure depends on the oscillator. The M16C/65 Group contains a feedback resistor, but an external feedback resistor may be required. Contact the oscillator manufacturer regarding circuit constants, as they are dependent on the oscillator or stray capacitance of the mounted circuit.
- Check output from the CLKOUT pin to confirm that the clock generated by the oscillation circuit is properly transmitted to the MCU. Procedures for outputting a clock from the CLKOUT pin are listed below. Set the clock output from the CLKOUT pin to 25 MHz or below.

Outputting the main clock

(1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
(2) Set the CM11 bit in the CM1 register to 0, the CM07 bit in the CM0 register to 0, and the CM21 bit in the CM2 register to 0 (main clock selected).
(3) Select the clock output from the CLKOUT pin (refer to the following table).
(4) Set the PRC0 bit in the PRCR register to 0 (write disabled)

Table 31.2 Output from CLKOUT Pin When Selecting Main Clock

Bit Setting		Output from CLKOUT Pin
PCLKR Register	CM0 Register	
PCLK5 Bit	Bits CM01 to CM00	
1	00b	Clock with the same frequency as the main clock
0	10b	Main clock divided by 8
0	11b	Main clock divided by 32

Outputting the sub clock

(1) Set the PRC0 bit in the PRCR register to 1 (write enabled).
(2) Set the CM07 bit in the CM0 register to 1 (sub clock selected).
(3) Set the PCLK5 bit in the PCLKR register to 0, and bits CM01 to CM00 in the CM0 register to 01b (fC output from CLKOUT pin).
(4) Set the PRC0 bit in the PRCR register to 0 (write disabled)

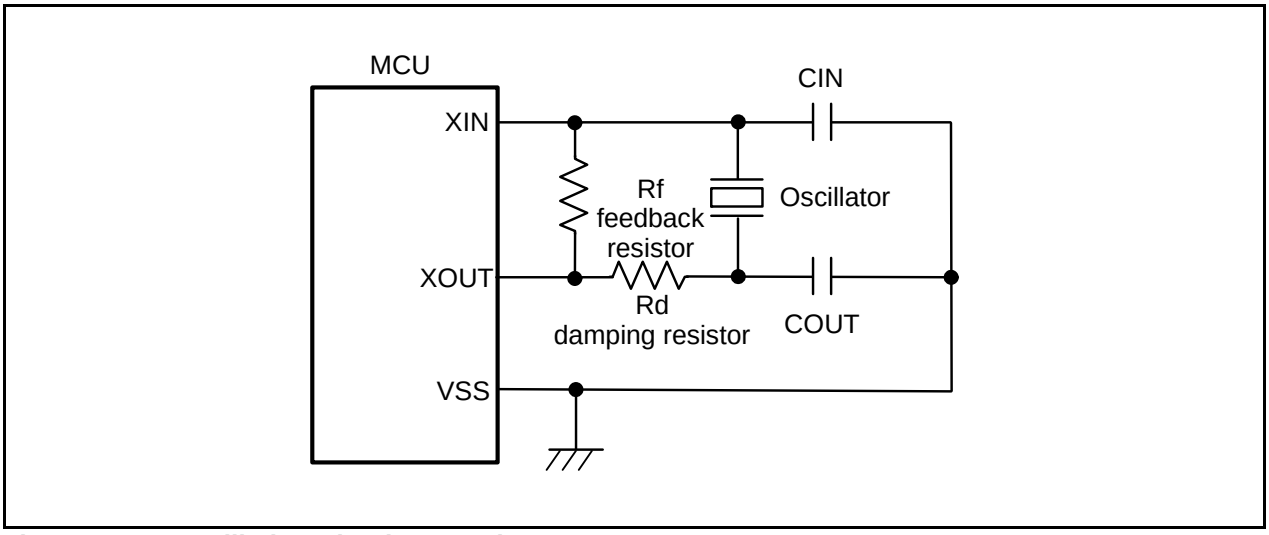


Figure 31.3 Oscillation Circuit Example

31.6.2 Noise Countermeasure

31.6.2.1 Clock I/O Pin Wiring

- Connect the shortest possible wiring to the clock I/O pin.
- Connect (a) the capacitor's ground lead connected to the oscillator, and (b) the MCU's VSS pin, with the shortest possible wiring (maximum 20 mm).

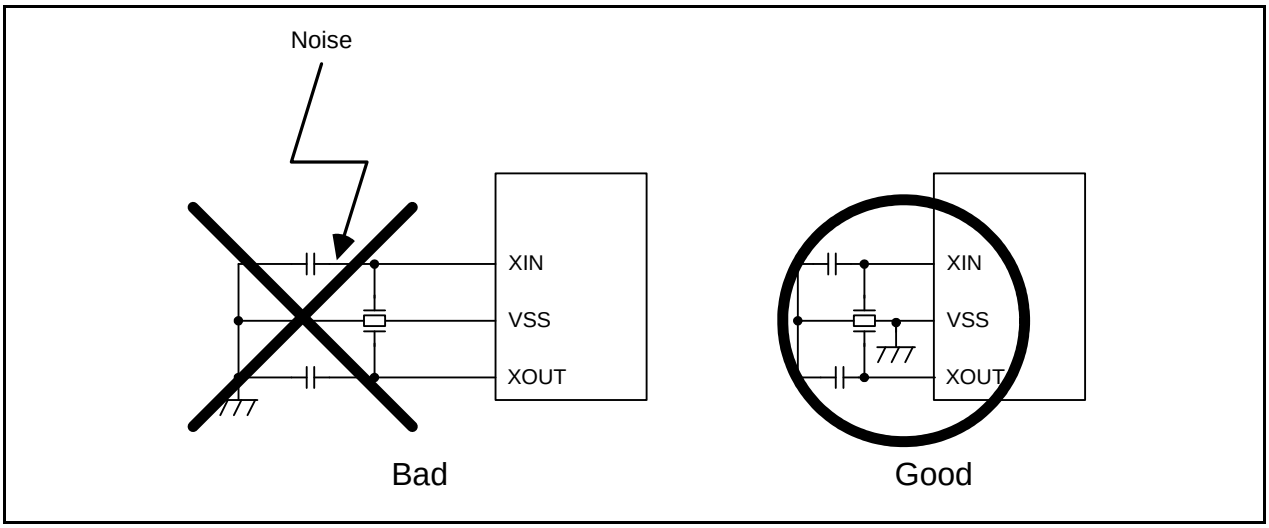


Figure 31.4 Clock I/O Pin Wiring

Reason

If noise enters the clock I/O pin, the clock waveform becomes unstable, which causes an error in operation or a program runaway. Also, if a potential difference attributed to the noise occurs between the VSS level of the MCU and the VSS level of the oscillator, an accurate clock is not input to the MCU.

31.6.2.2 Large Current Signal Line

For large currents that go above the MCU's current range, wire the signal lines as far away from the MCU as possible (especially the oscillator).

Reason

In the system using the MCU, there are signal lines for controlling motors, LEDs, and thermal heads. When a large current flows through these signal lines, noise is generated due to mutual inductance.

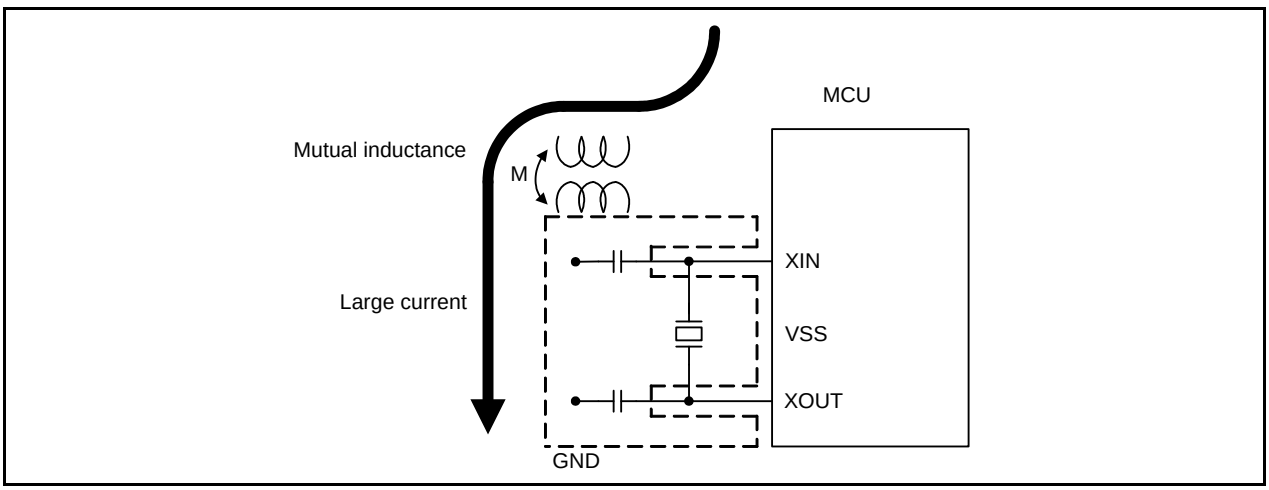


Figure 31.5 Large Current Signal Line Wiring

31.6.2.3 Signal Line Whose Level Changes at a High-Speed

For a signal line whose level changes at a high-speed, wire it as far away from the oscillator and the oscillator wiring pattern as possible. Do not wire it across or extend it parallel to a clock-related signal line or other signal lines which are sensitive to noise.

Reason
A signal whose level changes at a high-speed (such as the signal from the TAOUT pin) affects other signal lines due to the level change at rising or falling edges. Specially when the signal line crosses the clock-related signal line, the clock waveform becomes unstable, which causes an error in operation or a program runaway.

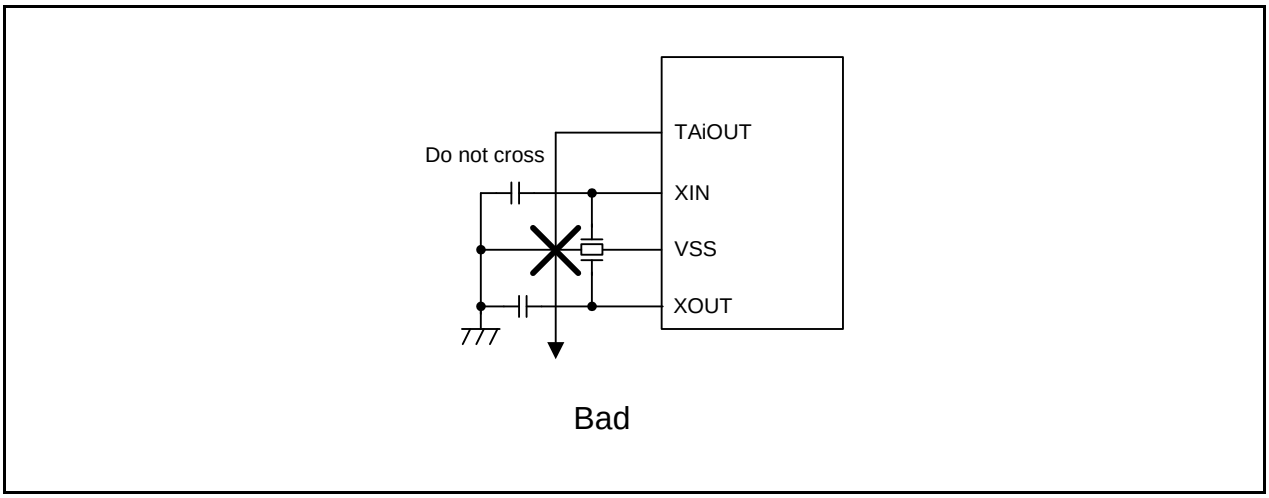


Figure 31.6 Wiring of Signal Line Whose Level Changes at High-Speed

31.6.3 CPU ClockW

- When the external clock is entered from the XIN pin and the main clock is used as the CPU clock, do not stop the external clock.

31.6.4 Oscillation Stop, Re-Oscillation Detect Function

- In the following cases, set the CM20 bit to 0 (oscillation stop/re-oscillation detect function disabled), and then change the status of each bit.
  When the CM05 bit is set to 1 (main clock stopped)
  When the CM10 bit is set to 1 (stop mode)
- To enter wait mode while using the oscillation stop/re-oscillation detection function, set the CM02 bit to 0 (peripheral function clock f1 not turned off during wait mode).
- This function cannot be used if the main clock frequency is 2 MHz or below. In that case, set the CM20 bit to 0 (oscillation stop/re-oscillation detect function disabled).
- While the CM27 bit is 1 (oscillation stop/re-oscillation detect interrupt), when the FRA01 bit is 1 (40 MHz on-chip oscillator selected), set the FRA00 bit to 1 (40 MHz on-chip oscillator on). (Do not set the FRA00 bit to 0 while FRA01 bit is 1, and vice versa.)

31.6.5 PLL Frequency Synthesizer

To use the PLL frequency synthesizer, stabilize the supply voltage to meet the power supply ripple standard.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f (ripple)	Power supply ripple allowable frequency (V_{CC1})				10	kHz
V_{P-P} (ripple)	Power supply ripple allowable amplitude voltage	(V_{CC1} = 5 V)			0.5	V
		(V_{CC1} = 3 V)			0.3	V
V_{CC} ($\lvert\Delta V / \Delta T\rvert$)	Power supply ripple rising/falling gradient	(V_{CC1} = 5 V)			0.3	V/ms
		(V_{CC1} = 3 V)			0.3	V/ms

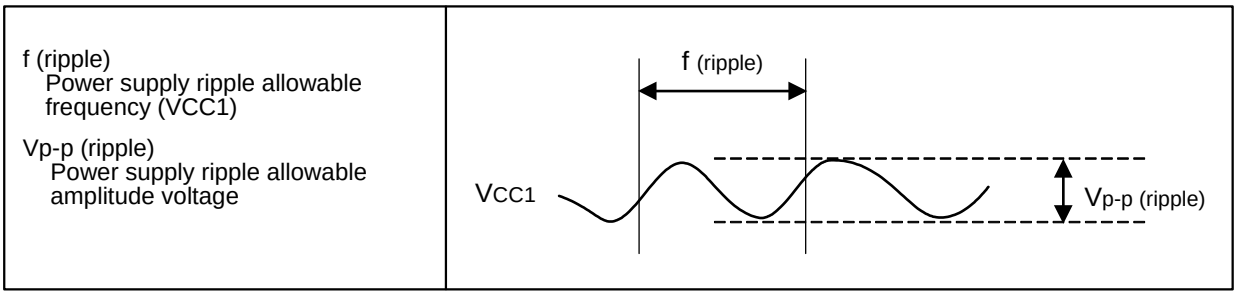


Figure 31.7 Voltage Fluctuation Timing

31.7 Notes on Power Control

31.7.1 CPU Clock

- When switching clock sources of the CPU clock, wait until the clock oscillation switched to is stabilized.

31.7.2 Wait Mode

- After the WAIT instruction, insert at least four NOP instructions. When entering wait mode, the instruction queue reads ahead the instructions following WAIT. Thus, depending on timing, some of the instructions may be executed before the MCU enters wait mode.

  Program example when entering wait mode is shown below.

```
Program Example:  FSET  I   ;
                  WAIT      ; Enter wait mode
                  NOP       ; More than four NOP instructions
                  NOP
                  NOP
                  NOP
```

- Do not enter wait mode when the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled). Set the FMR23 bit to 0 (low current consumption read mode disabled) and the FMR01 bit to 0 (CPU rewrite mode disabled), and disable DMA transfer before entering wait mode.

31.7.3 Stop Mode

- When exiting stop mode by hardware reset, drive the $\overline{\text{RESET}}$ pin low until main clock oscillation is stabilized.
- Set the MR0 bit in the TAiMR register (i = 0 to 4) to 0 (pulse not output) when using timer A to exit stop mode.
- When entering stop mode, insert a JMP.B instruction immediately after executing an instruction that sets the CM10 bit in the CM1 register to 1, and then insert at least four NOP instructions. When entering stop mode, the instruction queue reads ahead the instructions following the instruction which sets the CM10 bit to 1 (all clock stop). Thus, some of the instructions may be executed before the MCU enters stop mode or before the interrupt routine for returning from stop mode.

  Program example when entering stop mode

```
Program Example:  FSET   I
                  BSET   0, CM1   ; Enter stop mode
                  JMP.B  L2       ; Insert a JMP.B instruction
          L2:
                  NOP             ; At least four NOP instructions
                  NOP
                  NOP
                  NOP
```

- The CLKOUT pin outputs a high-level signal in stop mode. Thus, if stop mode is entered right after output on the CLKOUT pin changes state from high to low, the high-level durations of the output signal to the CLKOUT pin becomes shorter.

- When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not enter stop mode. To enter stop mode, execute an instruction to set the CM10 bit in the CM1 register to 1 (stop mode) after setting the FMR23 bit to 0 (low current consumption read mode disabled), setting the FMR01 bit to 0 (CPU rewrite mode disabled), and disabling DMA transfer.

31.7.4 Low Current Consumption Read Mode

- Enter low current consumption read mode through slow read mode (refer to Figure 9.4 “Setting and Canceling of Low Current Consumption Read Mode”).
- When the FMR23 bit in the FMR2 register is 1 (low current consumption read mode enabled), do not set the FMSTP bit to 1 (flash memory stopped). Also, when the FMSTP bit is 1, do not set the FMR23 bit to 1.

31.8 Notes on Processor Mode

Note

Do not use memory expansion mode and microprocessor mode in the 80-pin package.

31.9 Notes on Bus

Note

Do not use bus control pins for the 80-pin package.

31.9.1 Reading Data Flash

When 2.7 V ≤ VCC1 ≤ 3.0 V and f(BCLK) ≥ 16 MHz, or when 3.0 V < VCC1 ≤ 5.5 V and f(BCLK) ≥ 20 MHz, one wait state is necessary to read data flash. Use the PM17 bit or the FMR17 bit to specify one wait state.

31.9.2 External Bus

When a hardware reset, power-on reset or voltage monitor 0 reset is performed with a high-level input on the CNVSS pin, contents of internal ROM cannot be read.

31.9.3 External Access Soon After Writing to the SFRs

When writing to the SFRs is followed by accessing to an external device, the write signal and $\overline{CSi}$ signal switch simultaneously. Thus, adjust the capacity of individual signal not to make a write signal delay.

31.10 Notes on Memory Space Expansion Function

Note

Do not use this function for the 80-pin package.

31.11 Notes on Programmable I/O Ports

Note

P1, P4_4 to P4_7, P7_2 to P7_5, and P9_1 of the 80-pin package have no external connections. Program the direction bits of these ports to 1 (output mode) and the output data to 0 (low level). For the 80-pin and 100-pin packages, do not access the addresses of registers P11 to P14, PD11 to PD14 and PUR3.

31.11.1 Influence of the $\overline{SD}$ Input

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins P7_2 to P7_5 and P8_0 and P8_1 go to the high-impedance state.

31.11.2 Influence of SI/O3 and SI/O4

Setting the SM32 bit in the S3C register to 1 causes the P9_2 pin to go to the high-impedance state. Similarly, setting the SM42 bit in the S4C register to 1 causes the P9_6 pin to go to the high-impedance state.

31.11.3 100-Pin Package

Do not access to the addresses assigned to registers P11 to P14 and the PUR register.

31.11.4 80-Pin Package

Do not access to the addresses assigned to registers P11 to P14 and the PUR register.
Set the direction bits of the ports corresponding to P1, P4_4 to P4_7, P7_2 to P7_5 and P9_1 to 1 (output mode). Set the output data to 0 (low-level signal).

31.12 Notes on Interrupts

Note

Do not use $\overline{INT3}$ to $\overline{INT5}$ for the 80-pin package.

31.12.1 Reading Address 00000h

Do not read the address 00000h by a program. When a maskable interrupt request is accepted, the CPU reads interrupt information (interrupt number and interrupt request priority level) from address 00000h during the interrupt sequence. At this time, the IR bit of the accepted interrupt is cleared to 0.
If the address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. Thus, some problems may be caused: interrupts may be canceled, and an unexpected interrupt request may be generated.

31.12.2 SP Setting

Set a value in the SP (USP, ISP) before accepting an interrupt. The SP (USP, ISP) is set to 0000h after reset. Therefore, if an interrupt is accepted before setting a value in the SP (USP, ISP), the program may go out of control.
Especially when using the $\overline{NMI}$ interrupt, set a value in the ISP at the beginning of the program. For the first instruction after reset only, all interrupts including the $\overline{NMI}$ interrupt are disabled.

31.12.3 $\overline{NMI}$ Interrupt

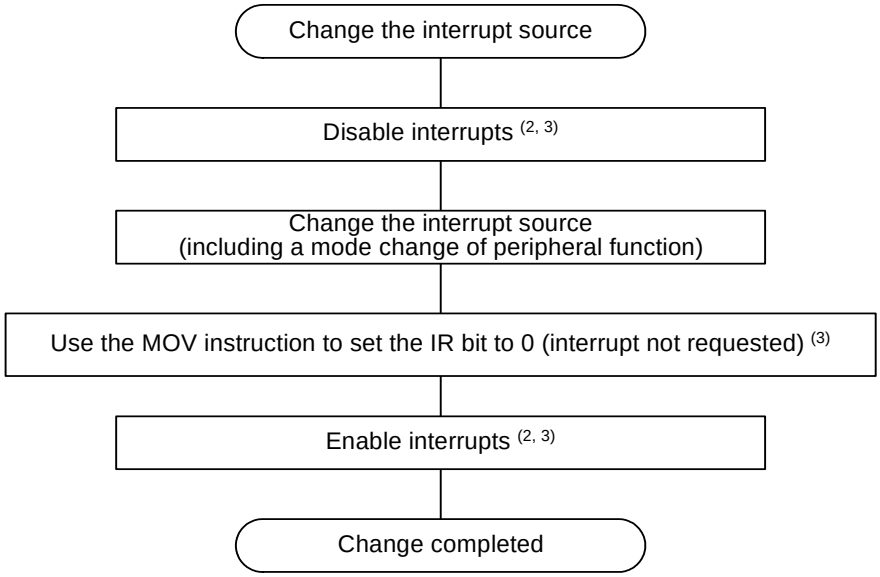
- When the $\overline{NMI}$ interrupt is not used, set the PM24 bit in the PM2 register to 0 ($\overline{NMI}$ interrupt disabled).
- Stop mode cannot be entered while the 24 bit is 1 ($\overline{NMI}$ interrupt enabled) and input on the $\overline{NMI}$ pin is low. When input on the $\overline{NMI}$ pin is low, the CM10 bit in the CM1 register is fixed to 0.
- Do not enter wait mode while the 24 bit is 1 ($\overline{NMI}$ interrupt enabled) and input on the $\overline{NMI}$ pin is low because the CPU clock remains active even though the CPU stops, and therefore, the current consumption of the chip does not drop. In this case, the normal condition is restored by the next interrupt generated.
- Set the low- and high-level durations of the input signal to the $\overline{NMI}$ pin to 2 CPU clock cycles + 300 ns or more.

31.12.4 Changing an Interrupt Source

If the interrupt source is changed, the IR bit in the interrupt control register may inadvertently be set to 1 (interrupt requested). To use an interrupt, change the interrupt source, and then set the IR bit to 0 (interrupt not requested).

In this section, the changing of an interrupt source refers to all elements (e.g. changing the mode of a peripheral function) used in changing the interrupt source, polarity, and timing assigned to each software interrupt number. When using an element to change the interrupt source, polarity, or timing, make the change before setting the IR bit to 0 (interrupt not requested). Refer to the descriptions of the individual peripheral functions for details of the peripheral function interrupts.

Figure 31.8 shows the Procedure for Changing the Interrupt Generate Factor.



IR bit: A bit in the interrupt control register for the interrupt whose interrupt source is to be changed

Notes :

1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. Use the I flag for the $\overline{\text{INTi}}$ interrupt (i = 0 to 7).
   For the interrupts from peripheral functions other than the $\overline{\text{INTi}}$ interrupt, turn off the peripheral function that is the source of the interrupt in order not to generate an interrupt request before changing the interrupt source. In this case, if the maskable interrupts can all be disabled without causing a problem, use the I flag. Otherwise, use the corresponding bits ILVL2 to ILVL0 for the interrupt whose interrupt source is to be changed.
3. Refer to the following “Rewriting the Interrupt Control Register” for details about the instructions to use and the notes to be taken for instruction execution.

Figure 31.8 Procedure for Changing the Interrupt Generate Factor

31.12.5 Rewriting the Interrupt Control Register

(a) The interrupt control register for any interrupt should be modified in places where no requests for that register may occur. If an interrupt request generation is a possibility, disable an interrupt and then rewrite the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling an interrupt, be careful with the instruction used.

- Changing bits other than the IR bit
  When interrupts corresponding to the register occur, the IR bit may not be set to 1 (interrupt requested) and the interrupts may be ignored. If this causes a problem, use one of the following instructions to change the registers.
  Instructions: AND, OR, BCLR, or BSET.
- Changing the IR bit
  Depending on the instruction used, the IR bit may not always be set to 0 (interrupt not requested). Therefore, use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample program code shown below. (Refer to (b) regarding rewriting the contents of the interrupt control registers using the sample program code.)

Examples 1 through 3 show how to prevent the I flag from being set to 1 (interrupt enabled) before the contents of the interrupt control register are rewritten, owing to the effects of the internal bus and the instruction queue buffer.

Example 1: Using the NOP instruction to pause the program until the interrupt control register is modified

```
INT_SWITCH1:
    FCLR    I           ; Disable interrupts.
    AND.B   #00h, 0055h ; Set the TA0IC register to 00h.
    NOP                 ;
    NOP
    FSET    I           ; Enable interrupts.
```

The number of the NOP instructions is as follows.
PM20 = 1 (1 wait): 2, PM20 = 0 (2 waits): 3, when using the $\overline{\text{HOLD}}$ function: 4.

Example 2: Using a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I           ; Disable interrupts.
    AND.B   #00h, 0055h ; Set the TA0IC register to 00h.
    MOV.W   MEM, R0     ; Dummy read.
    FSET    I           ; Enable interrupts.
```

Example 3: Using the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I           ; Disable interrupts.
    AND.B   #00h, 0055h ; Set the TA0IC register to 00h.
    POPC    FLG         ; Enable interrupts.
```

31.12.6 $\overline{\text{INT}}$ Interrupt

- Either a low level of at least tw (INL) width or a high level of at least tw (INH) width is necessary for the signal input to pins $\overline{\text{INT0}}$ through $\overline{\text{INT7}}$ regardless of the CPU operation clock.
- If the POL bit in registers INT0IC to INT7IC, bits IFSR7 to IFSR0 in the IFSR register, or bits IFSR31 to IFSR30 in the IFSR3A register are changed, the IR bit may inadvertently be set to 1 (interrupt requested). Be sure to set the IR bit to 0 (interrupt not requested) after changing any of these register bits.

31.13 Notes on Watchdog Timer

After the watchdog timer interrupt occurs, use the WDTR register to refresh the watchdog timer counter.

31.14 Notes on DMAC

31.14.1 Write to the DMAE Bit in the DMiCON Register (i = 0 to 3)

When both of following conditions are met, follow steps (1) and (2) below.

- Write a 1 (DMAi is in active state) to the DMAE bit when it is 1.
- A DMA request may occur simultaneously when the DMAE bit is being written.

Steps

(1) Write a 1 to the DMAE bit and DMAS bit in the DMiCON register simultaneously (1).
(2) Make sure that the DMAi is in an initialized state (2) in a program.
If the DMAi is not in an initialized state, repeat these two steps.

Notes:

1. The DMAS bit remains unchanged even if a 1 is written. However, if a 0 is written to this bit, it is set to 0 (DMA not requested). In order to prevent the DMAS bit from being modified to 0, 1 should be written to the DMAS bit when 1 is written to the DMAE bit. In this way, the state of the DMAS bit immediately before being written can be maintained.
Similarly, when writing to the DMAE bit with a read-modify-write instruction, write a 1 to the DMAS bit to maintain a DMA request which is generated during execution.
2. Read the TCRi register to verify whether the DMAi is in an initialized state.
If the read value is equal to a value that was written to the TCRi register before DMA transfer start, the DMAi is in an initialized state. (When a DMA request occurs after writing to the DMAE bit, the read value is a value written to the TCRi register minus one.) If the read value is a value in the middle of a transfer, the DMAi is not in an initialized state.

31.14.2 Changing DMA Request Source

When the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed, the DMAS bit in the DMiCON sometimes becomes 1 (DMA requested). Set the DMAS bit to 0 (DMA not requested) after the DMS bit or bits DSEL4 to DSEL0 in the DMiSL register are changed.

31.15 Notes on Timer A

Note

The 80-pin package does not have pins TA1IN, TA1OUT, TA2IN and TA2OUT. Do not use functions associated with these pins.

31.15.1 Timer A (Timer Mode)

31.15.1.1 Register Setting

The timer stops after reset. Set the mode, count source, counter value, etc., using registers TAiMR, TAi, TACS0 to TACS2, TAPOFS, TCKDIVC0, and PCLKR before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 0 to 4).
Always make sure registers TAiMR, TACS0 to TACS2, TAPOFS, TCKDIVC0, and PCLKR are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

31.15.1.2 Read from Timer

While counting is in progress, the counter value can be read at any time by reading the TAi register. However, if the counter is read at the same time as it is reloaded, the value FFFFh is read. Also, if the counter is read before it starts counting and after a value is set in the TAi register while not counting, the set value is read.

31.15.1.3 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT go to the high-impedance state.

31.15.2 Timer A (Event Counter Mode)

31.15.2.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TAiMR register, the TAi register, the UDF register, bits TAZIE, TA0TGL, and TA0TGH in the ONSF register, the TRGSR register, and the TAPOFS register before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 0 to 4).

Always make sure the TAiMR register, the UDF register, bits TAZIE, TA0TGL, and TA0TGH in the ONSF register, the TRGSR register, and the TAPOFS register are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

31.15.2.2 Read from Timer

While counting is in progress, the counter value can be read at any time by reading the TAi register. However, while reloading, FFFFh can be read in underflow, and 0000h in overflow. When the counter is read before it starts counting and after a value is set in the TAi register while not counting, the set value is read.

31.15.2.3 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT go to the high-impedance state.

31.15.3 Timer A (One-Shot Timer Mode)

31.15.3.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TAiMR register, the TAi register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, the TCKDIVC0 register, and the PCLKR register before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 0 to 4).

Always make sure the TAiMR register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, the TCKDIVC0 register, and the PCLKR register are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

31.15.3.2 Stop While Counting

When setting the TAiS bit to 0 (count stops), the following occurs:

- The counter stops counting and the contents of the reload register are reloaded.
- The TAiOUT pin outputs a low-level signal when the POFSi bit in the TAPOFS register is 0 and outputs a high-level signal when it is 1.
- After one cycle of the CPU clock, the IR bit in the TAiIC register is set to 1 (interrupt requested).

31.15.3.3 Delay between the Trigger Input and Timer Output

One-shot timer output synchronizes with a count source generated internally. When an external trigger is selected, a maximum 1.5 cycle delay of the count source occurs between the trigger input to the TAiIN pin and timer output.

31.15.3.4 Operating Mode Change

The IR bit is set to 1 when timer operating mode is set with any of the following procedures:

- Selecting one-shot timer mode after reset
- Changing the operating mode from timer mode to one-shot timer mode
- Changing the operating mode from event counter mode to one-shot timer mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 after the changes listed above are made.

31.15.3.5 Re-Trigger

When a trigger occurs while counting, the counter reloads the reload register to continue counting after generating a re-trigger and counting down once. To generate a trigger while counting, generate a re-trigger after more than one cycle of the timer count source has elapsed following the previous trigger.

When an external trigger occurs, do not generate a re-trigger for 300 ns before the count value becomes 0000h.

The one-shot timer may stop counting.

31.15.3.6 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT enter a high-impedance state.

31.15.4 Timer A (Pulse Width Modulation Mode)

31.15.4.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TAiMR register, the TAi register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, TCKDIVC0 register, the PWMFS register, and the PCLKR register before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 0 to 4).
Always make sure the TAiMR register, bits TA0TGL and TA0TGH in the ONSF register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, TCKDIVC0 register, the PWMFS register, and the PCLKR register are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

31.15.4.2 Operating Mode Change

The IR bit is set to 1 when setting a timer operating mode with any of the following procedures:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

31.15.4.3 Stop While Counting

When setting the TAiS bit to 0 (count stops) during PWM pulse output, the following actions occur.
When the POFSi bit in the TAPOFS register is 0:

- Counting stops.
- When the TAiOUT pin is high, the output level goes low and the IR bit is set to 1.
- When the TAiOUT pin is low, both the output level and the IR bit remain unchanged.

When the POFSi bit in the TAPOFS register is 1:

- Stop counting.
- If the TAiOUT pin output is low, the output level goes high and the IR bit is set to 1.
- If the TAiOUT pin output is high, both the output level and the IR bit remain unchanged.

31.15.4.4 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT go to the high-impedance state.

31.15.5 Timer A (Programmable Output Mode)

31.15.5.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TAiMR register, the TAi register, the TRGSR register, registers TACS0 to TACS2, the TAPOF register, TCKDIVC0 register, the PWMFS register, the PCLKR register, and the TAi1 register before setting the TAiS bit in the TABSR register to 1 (count starts) (i = 1, 2, 4).
Always make sure the TAiMR register, the TRGSR register, registers TACS0 to TACS2, the TAPOFS register, TCKDIVC0 register, the PWMFS register, and the PCLKR register are modified while the TAiS bit is 0 (count stops), regardless of whether after reset or not.

31.15.5.2 Operating Mode Change

The IR bit is set to 1 when setting a timer operating mode with any of the following procedures:

- Selecting PWM mode or programmable output mode after reset
- Changing the operating mode from timer mode to PWM mode or programmable output mode
- Changing the operating mode from event counter mode to PWM mode or programmable output mode

To use the timer Ai interrupt (IR bit), set the IR bit to 0 by a program after the changes listed above are made.

31.15.5.3 Stop While Counting

When setting the TAiS bit to 0 (count stops) during pulse output, the following actions occur.
When the POFSi bit in the TAPOFS register is 0:

- Counting stops.
- When the TAiOUT pin is high, the output level goes low and the IR bit is set to 1.
- When the TAiOUT pin is low, both the output level and the IR bit remain unchanged.

When the POFSi bit in the TAPOFS register is 1:

- Stop counting.
- If the TAiOUT pin output is low, the output level goes high and the IR bit is set to 1.
- If the TAiOUT pin output is high, both the output level and the IR bit remain unchanged.

31.15.5.4 Influence of $\overline{SD}$

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on the $\overline{SD}$ pin enabled), pins TA1OUT, TA2OUT, and TA4OUT go to the high-impedance state.

31.16 Notes on Timer B

Note

The 80-pin package does not have the TB1IN pin. Do not use functions associated with this pin.

31.16.1 Timer B (Timer Mode)

31.16.1.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using registers TBiMR, TBi, TBCS0 to TBCS3, TCKDIVC0, and PCLKR before setting the TBiS bit in the TABSR or the TBSR register to 1 (count starts) (i = 0 to 5).
Always make sure registers TBiMR, TBCS0 to TBCS3, TCKDIVC0, and PCLKR are modified while the TBiS bit is 0 (count stops), regardless of whether after reset or not.

31.16.1.2 Read from Timer

The value of the counter while counting can be read from the TBi register at any time. FFFFh is read while reloading. If the counter is read before it starts counting and after a value is set in the TBi register while not counting, the set value is read.

31.16.2 Timer B (Event Counter Mode)

31.16.2.1 Register Setting

The timer is stopped after reset. Set the mode, count source, counter value, etc., using the TBiMR register and TBi register before setting the TBiS bit in the TABSR or the TBSR register to 1 (count starts) (i = 0 to 5).

Always make sure the TBiMR register is modified while the TBiS bit is 0 (count stops), regardless of whether after reset or not.

31.16.2.2 Read from Timer

While counting is in progress, the counter value can be read out at any time by reading the TBi register. However, if this register is read at the same time the counter is reloaded, the read value is always FFFFh. If the TBi register is read after setting a value in it while not counting but before the counter starts counting, the read value is the value set in the register.

31.16.3 Timer B (Pulse Period/Pulse Width Measurement Modes)

31.16.3.1 Register Setting

The timer is stopped after reset. Set the mode, count source, etc., using registers TBiMR, TBCS0 to TBCS3, TBi, TCKDIVC0, PCLKR, PPWFS1, and PPWFS2 before setting the TBiS bit in the TABSR or TBSR register to 1 (count starts) (i = 0 to 5).

Always make sure registers TBiMR, TBCS0 to TBCS3, TCKDIVC0, PCLKR, PPWFS1, and PPWFS2 are modified while the TBiS bit is 0 (count stops), regardless of whether after reset or not. To clear the MR3 bit to 0 by writing to the TBiMR register while the TBiS bit is 1 (count starts), be sure to write the same value as previously written to bits TMOD0, TMOD1, MR0, MR1, TCK0, and TCK1 and a 0 to bit 4.

31.16.3.2 Interrupts

The IR bit in the TBiIC register is set to 1 (interrupt requested) when an active edge of a measurement pulse is input or timer Bi overflows (i = 0 to 5). The source of an interrupt request can be determined by using the MR3 bit in the TBiMR register within the interrupt routine.

Use the IR bit in the TBiIC register to detect overflows only. Use the MR3 bit only to determine the interrupt source.

31.16.3.3 Operations between Count Start and the First Measurement

When a count is started and the first active edge is input, an undefined value is transferred to the reload register. At this time, timer Bi interrupt request is not generated.

The value of the counter is undefined after reset. If count is started in this state, the MR3 bit may be set to 1 and timer Bi interrupt request may be generated after count start before an effective edge is input. When a value is set in the TBi register while the TBiS bit is 0 (count stops), the same value is written to the counter.

31.16.3.4 Pulse Period Measurement Mode

When an overflow occurs at an active edge, an input is not recognized at the effective edge because an interrupt request is generated only once. Use this mode where an overflow does not occur, or use pulse width measurement.

31.16.3.5 Pulse Width Measurement Mode

In pulse width measurement, pulse widths are measured successively. Use a program to check whether the measurement result is a high-level width or a low-level width.

When an interrupt request is generated, read the TBiIN pin level inside the interrupt routine, and check whether it is the edge of an input pulse or an overflow. The TBiIN level can be read from bits in the P9 register of corresponding ports.

31.17 Notes on Three-Phase Motor Control Timer Function

Note

Do not use this function for the 80-pin package.

31.17.1 Timer A, Timer B

Refer to 17.5 “Notes on Timer A” and 18.5 “Notes on Timer B”.

31.17.2 Forced Cutoff Input

The following pins are affected by the three-phase forced cutoff due to the $\overline{SD}$ pin input:
P7_2/CLK2/TA1OUT/V, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$, P7_4/TA2OUT/W, P7_5/TA2IN/$\overline{W}$, P8_0/TA4OUT/RXD5/SCL5/U, P8_1/TA4IN/$\overline{CTS5}$/$\overline{RTS5}$/$\overline{U}$

31.18 Notes on Real-Time Clock

31.18.1 Starting and Stopping Count

Real-time clock has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the RTCCR1 register.

Real-time clock starts counting and the TCSTF bit becomes 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to two cycles of the count source until the TCSTF bit becomes 1 after setting the TSTART bit to 1. During this time, do not access registers associated with real-time clock (1) other than the TCSTF bit.

Also, real-time clock stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit becomes 0 (count stops). It takes up to three cycles of the count source until the TCSTF bit becomes 0 after setting the TSTART bit to 0. During this time, do not access registers associated with real-time clock other than the TCSTF bit.

Note:

1. Registers associated with real-time clock: RTCSEC, RTCMIN, RTCHR, RTCWK, RTCCR1, RTCCR2, RTCCSR, RTCCSEC, RTCCMIN, and RTCCHR.

31.18.2 Register Setting (Time Data etc.)

Write to the following registers or bits while real-time clock is stopped.

- Registers RTCSEC, RTCMIN, RTCHR, RTCWK, and RTCCR2
- Bits H12H24 and RTCPM in the RTCCR1 register
- Bits RCS0 to RCS4 in the RTCCSR register

Real-time clock is stopped when bits TSTART and TCSTF in the RTCCR1 register are 0 (real-time clock stopped).

Also, set all above-mentioned registers and bits (immediately before real-time clock count starts) before setting the RTCCR2 register.

Figure 20.4 shows Time and Day Change Procedure (No Compare Mode or Compare 1 Mode), and Figure 20.5 shows Time and Day Change Procedure (Compare 2 Mode or Compare 3 Mode).

31.18.3 Register Setting (Compare Data)

Write to the following registers when the BSY bit in the RTCSEC register is 0 (not while data is updated).

- Registers RTCCSEC, RTCCMIN, and RTCCHR

31.18.4 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read time data bits (1) when the BSY bit in the RTCSEC register is 0 (not while data is updated).
When reading multiple registers, if data is rewritten between reading registers, an errant time will be read.
In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of time data bits in the real-time clock interrupt routine.
- Monitoring by a program 1
  Monitor the IR bit in the RTCTIC register by a program and read necessary contents of time data bits after the IR bit in the RTCTIC register becomes 1 (periodic interrupt request generated).
- Monitoring by a program 2
  (1)Monitor the BSY bit.
  (2)Monitor until the BSY bit becomes 0 after the BSY bit becomes 1 (the BSY bit is set to 1 for approximately 62.5 ms).
  (3)Read necessary contents of time data bits after the BSY bit becomes 0.
- Using read results if they are the same value twice
  (1)Read necessary contents of time data bits.
  (2)Read the same bit as (1) and compare the contents.
  (3)Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

Note:
1. Time data bits are shown below.
   Bits SC12 to SC10 and SC03 to SC00 in the RTCSEC register
   Bits MN12 to MN10 and MN03 to MN00 in the RTCMIN register
   Bits HR11 to HR10 and HR03 to HR00 in the RTCHR register
   Bits WK2 to WK0 in the RTCWK
   The RTCPM bit in the RTCCR1 register

31.19 Notes on Pulse Width Modulator

Note

The 80-pin package does not have pins P4_6 and P4_7. Use pins P9_3 and P9_4 for PWM0 and PWM1 output.

31.20 Notes on Remote Control Signal Receiver

Note

The 80-pin package does not have the PMC1 pin. Use the PMC0 pin for external pulse input.

31.20.1 Start/Stop of PMCi

The EN bit in the PMCiCON0 register controls start/stop of PMCi. The ENFLG bit in the PMCiCON2 register indicates that the operation starts or stops.
The PMCi circuit starts operating by setting the EN bit to 1 (operation starts) and the ENFLG bit becomes 1. It takes up to two cycles of the count source until the ENFLG bit becomes 1 after setting the EN bit to 1. During this period, do not access registers associated with PMCi (registers listed in Table 22.3 and Table 22.4 “register structure (PMCi circuit)”) excluding the ENFLG bit.
When the EN bit is set to 0 (operation stops), PMCi circuit stops operating and the ENFLG bit becomes 0 (operation stops). It takes up to one cycle of the count source until the ENFLG bit becomes 0 after setting the EN bit to 0.

31.20.2 Register Reading Procedure

If reading the following registers when the data changes, undefined value may be read.
Each flag in registers PMCiCON2 and PMCiSTS
Registers PMCiTIM, PMC0DAT0 to PMC0DAT5, PMCiBC, and PMC0RBIT
Read above registers as follows to avoid reading the undefined value.

In pattern match mode

- Using interrupt
  Set the DRINT bit in the PMCiINT register to 1 (data reception complete interrupt enabled) and read the registers within PMCi interrupt routine.
- Monitoring by a program 1
  Set the DRINT bit in the PMCiINT register to 1 (data reception complete interrupt enabled) and monitor the IR bit in the PMCiIC register by a program. Read the registers when the IR bit becomes 1 (interrupt request is generated).
- Monitoring by a program 2
  (1) Monitor the DRFLG bit in the PMCiSTS register
  (2) When the DRFLG bit becomes 1, monitor the DRFLG bit until it becomes 0.
  (3) Read the necessary content of the registers when the DRFLG bit becomes 0.

In input capture mode

- Using interrupt
  Set the TIMINT bit in the PMCiINT register to 1 (timer measure interrupt enabled) and read the registers within PMCi interrupt routine.
- Monitoring by a program 1
  Set the TIMINT bit in the PMCiINT register to 1 (timer measure interrupt enabled) and monitor the IR bit in the PMCiIC register by a program. Read the registers when the IR bit becomes 1 (interrupt request is generated).

31.21 Notes on Serial Interface UARTi (i = 0 to 2, 5 to 7)

Note

The 80-pin package does not have pins CLK2 and $\overline{CTS2}$/$\overline{RTS2}$ for UART2. Do not use functions associated with these pins. UART6 and UART7 are not included.

If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the following pins go to high-impedance state:
P7_2/CLK2/TA1OUT/V, P7_3/$\overline{CTS2}$/$\overline{RTS2}$/TA1IN/$\overline{V}$, P7_4/TA2OUT/W, P7_5/TA2IN/$\overline{W}$, P8_0/TA4OUT/RXD5/SCL5/U, P8_1/TA4IN/$\overline{CTS5}$/$\overline{RTS5}$/$\overline{U}$

31.21.1 Clock Synchronous Serial I/O

31.21.1.1 Transmission/Reception

When the $\overline{RTS}$ function is used with an external clock, $\overline{RTSi}$ pin (i = 0 to 2, 5 to 7) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{RTSi}$ pin outputs a high-level signal when a receive operation starts. Therefore, a transmit timing and receive timing can be synchronized by connecting the $\overline{RTSi}$ pin to the $\overline{CTSi}$ pin of the transmitting side. The $\overline{RTS}$ function is disabled when an internal clock is selected.

31.21.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the UiC0 register (i = 0 to 2, 5 to 7) is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transmit and receive clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transmit and receive clock).

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When $\overline{CTS}$ function is selected, input on the $\overline{CTSi}$ pin is low.

31.21.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating a transmitter. Set the UARTi-associated registers for a transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXDi pin (i = 0 to 2, 5 to 7) while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the UiC1 register to 1 (transmission enabled) and placing dummy data in the UiTB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the UiTB register, and input an external clock to the CLKi pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RI bit in the UiC1 register is set to 1 (data present in the UiRB register) and the next receive data is received in the UARTi receive register. And then, the OER bit in the UiRB register is set to 1 (overrun error occurred). At this time, the UiRB register is undefined. When an overrun error occurs, program the transmitting and receiving sides to retransmit the previous data. If an overrun error occurs, the IR bit in the SiRIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the UiTB register per each receive operation.

When an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is 0 (transmit data output at the falling edge and receive data input at the rising edge of the serial clock), or while the external clock is held low when the CKPOL bit is 1 (transmit data output at the rising edge and receive data input at the falling edge of the serial clock).

- The RE bit in the UiC1 register is 1 (reception enabled).
- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).

31.21.2 UART (Clock Asynchronous Serial I/O) Mode

31.21.2.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTSi}}$ pin (i = 0 to 2, 5 to 7) outputs a low-level signal, which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTSi}}$ pin outputs a high-level signal when a receive operation starts. Therefore, a transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTSi}}$ pin to the $\overline{\text{CTSi}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

31.21.2.2 Transmission

When an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the UiC0 register (i = 0 to 2, 5 to 7) is 0 (transmit data output at the falling edge and receive data input at the rising edge of the transmit and receive clock), or while the external clock is held low when the CKPOL bit is 1 (transmit data output at the rising edge and receive data input at the falling edge of the transmit and receive clock).

- The TE bit in the UiC1 register is 1 (transmission enabled).
- The TI bit in the UiC1 register is 0 (data present in the UiTB register).
- When $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTSi}}$ pin is low.

31.21.3 Special Mode 1 (I^2C Mode)

31.21.3.1 Generation of Start and Stop Conditions

When generating start, stop and restart conditions, set the STSPSEL bit in the UiSMR4 register (i = 0 to 2, 5 to 7) to 0 and wait for more than half cycle of the transmit and receive clock. Then set each condition generation bit (STAREQ, RSTAREQ and STPREQ) from 0 to 1.

31.21.3.2 IR Bit

Set the following bits first, and then set the IR bit in the UARTi interrupt control registers to 0 (interrupt not requested).

Bits SMD2 to SMD0 in the UiMR register, the IICM bit in the UiSMR register,
the IICM2 bit in the UiSMR2 register, the CKPH bit in the UiSMR3 register

31.21.4 Special Mode 4 (SIM Mode)

After reset, a transmit interrupt request is generated by setting bits U2IRS and U2ERE in the U2C1 register to 1 (transmission completed) and 1 (error signal output), respectively. Therefore, when using SIM mode, make sure to set the IR bit to 0 (interrupt not requested) after setting these bits.

31.22 Notes on SI/O3 and SI/O4

Note

The 80-pin package does not have the SIN3 pin for SI/O3. SI/O3 is used for transmission only. No reception is possible.

31.22.1 SOUTi Pin Level When SOUTi Output Disabled

When the SMi2 bit in the SiC register is set to 1 (SOUTi output disabled), the target pin goes to high-impedance state regardless of which function of the pin is being used.

31.22.2 External Clock Control

The data written into the SiTRR register is shifted every time the external clock is input. When completing data transmission/reception of the 8th bit, read or write into the SiTRR register before inputting the clock for the next data transmission/reception.

31.22.3 Register Access When Using External Clock

When the SMi6 bit in the SiC register is set to 0 (external clock), write into the SMi7 bit in the SiC register and the SiTRR register under the following conditions:

- When the SMi4 bit in the SiC register is set to 0 (transmit data is output at falling edge of transmit/receive clock and receive data is input at rising edge): CLKi input is high level.
- When the SMi4 bit in the SiC register is set to 1 (transmit data is output at rising edge of transmit/receive clock and receive data is input at falling edge): CLKi input is low level.

31.22.4 SiTRR Register Access

Write transmit data into the SiTRR register while transmission/reception stops. Read receive data from the SiTRR register while transmission/reception stops.
The IR bit in the SiIC register becomes 1 (interrupt request) during output of the 8th bit.
If the SM26 bit (SOUT3) or SM27 bit (SOUT4) in the S32C2 register is set to 0 (high-impedance after transmission), SOUTi pin becomes high-impedance when the transmit data is written into the SiTRR register immediately after an interrupt request is generated, and hold time of the transmit data becomes shorter.

31.22.5 Pin Function Switch When Using Internal Clock

If the SMi3 bit in the SiC register (i = 3, 4) changes from 0 (I/O port) to 1 (SOUTi output, CLK function) when setting the SMi2 bit to 0 (SOUTi output) and the SMi6 bit to 1 (internal clock), SOUTi initial value set to the SOUTi pin by the SMi7 bit may be output about for 10 ns. After that, the SOUTi pin becomes high-impedance.
If the output level from the SOUTi pin when the SMi3 bit changes from 0 to 1 becomes a problem, set the SOUTi initial value by the SMi7 bit.

31.22.6 Operation After Reset When Selecting External Clock

When the SMi6 bit in the SiC register is set to 0 (external clock) after reset, the IR bit in the SiIC register becomes 1 (interrupt request) by inputting the external clock for 8 bits to the CLKi pin. This will also happen even when the SMi3 bit in the SiC register is 0 (serial interface disabled) or before the value is written into the SiTRR register.

31.23 Notes on Multi-Master I²C-bus Interface

31.23.1 Limitation on CPU Clock

When the CM07 bit in the CM0 register is 1 (CPU clock is a sub clock), do not access the registers listed in Table 25.4 “Register Configuration”. Set the CM07 bit to 0 (main clock, PLL clock, or on-chip oscillator clock) to access these registers.

31.23.2 Register Access

Notes are described to access the I2C interface control registers. The period from the rising edge of 1st clock of slave address or one-byte data transmission/reception to the falling edge of an ACK clock is considered as “period of transmission/reception”. When the ACKCLK bit is 0 (no ACK clock), the period of transmission/reception is from the rising edge of 1st clock of slave address or one-byte data transmission/reception to the falling edge of 8th clock.

31.23.2.1 S00 Register

Do not write to the S00 register during transmission/reception.

31.23.2.2 S10 Register

Do not change bits other than the IHR bit in the S10 register during transmission/reception.

31.23.2.3 S20 Register

Do not change bits other than the ACKBIT bit in the S20 register during transmission/reception.

31.23.2.4 S3D0 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S3D0 register.
- Bits ICK1 and ICK0 should be changed when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

31.23.2.5 S4D0 Register

Bits ICK4 to ICK2 should be changed when the ES0 bit in the S1D0 register is 0 (I2C interface disabled).

31.23.2.6 S10 Register

- Do not use the bit managing instruction (read-modify-write instruction) to access the S10 register.
- Do not write to the S10 register when bits MST and TRX change their values.

Figure 25.13 “Start Condition Detection” to Figure 25.15 “Operation After Completion of Slave Address/ Data Transmit/Receive” shows when bits MST and TRX change.

31.24 Notes on CEC (Consumer Electronics Control)

31.24.1 Registers and Bit Operation

The registers and the bits of the CEC function are synchronized with the count source. Therefore, the internal circuit starts to operate from the next count source timing, while the contents of the register is changed immediately after rewriting the value of the register.
When changing the value of the same bit successively or reading the bit changed under the influence of another bit, wait for one or more cycles of the count source.

Example: when changing the value of the same bit successively
(1) Change the bit to 0.
(2) Wait for one or more cycles of the count source.
(3) Change the same bit to 1.

Example: when reading the bit changed under the influence of another bit
(after the reception is disabled, to ensure that the CRERRFLG bit in the CECFLG register becomes 0 (no reception error detected)).
(1) Set the CRXDEN bit in the CECC3 register to 0 (reception disabled)
(2) Wait for one or more cycles of the count source
(3) Read the CRERRFLG bit in the CECFLG register.

31.25 Notes on A/D Converter

31.25.1 Analog Input Pin

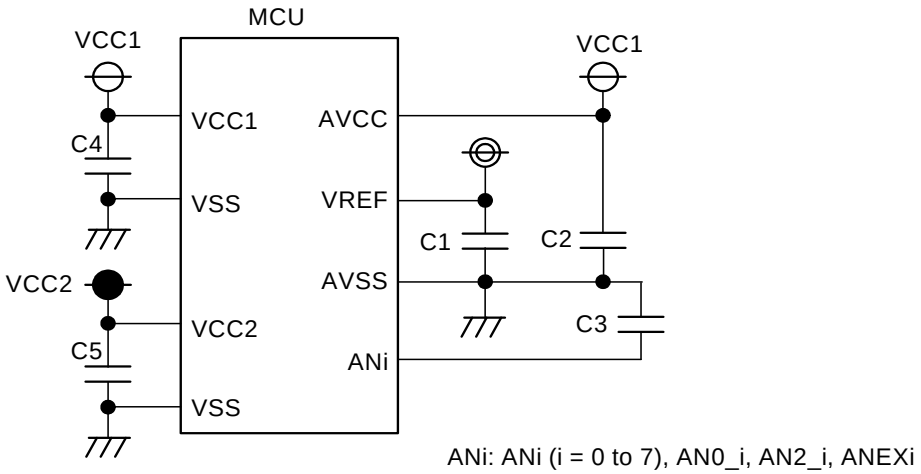
When VCC1 ≥ VCC2, set analog input voltage as follows:
analog input voltage (AN_0 to AN_7, ANEX0, and ANEX1) ≤ VCC1
analog input voltage (AN0_0 to AN0_7 and AN2_7 to AN2_7) ≤ VCC2
Do not use any of four pins AN4 to AN7 as analog input pins if a key input interrupt is to be used (key input interrupt request is generated when analog input voltage becomes low level).

31.25.2 ϕAD Frequency

Set ϕAD to 2 MHz or more, but an upper limit is set as follows:
4.0 ≤ VCC1 ≤ 5.5V: ϕAD ≤ 25 MHz
3.2 ≤ VCC1 ≤ 4.0V: ϕAD ≤ 16 MHz
3.0 ≤ VCC1 ≤ 3.2V: ϕAD ≤ 10 MHz

31.25.3 Pin Configuration

Three capacitors should be respectively put between pins AVCC, VREF, analog input (ANi (i = 0 to 7), ANEXi, AN0_i, and AN2_i) and the AVSS pin to protect from error operations caused by noise, latchup, or to reduce conversion errors. Also, a capacitor between the VCC1 pin and the VSS pin. Figure 31.9 shows Example of Pin Configuration.



Notes:
1.C1 ≥ 0.1 μF, C2 ≥ 0.1 μF, C3 ≥ 100pF, C4 ≥ 0.1 μF, C5 ≥ 0.1 μF (reference values).
2.The traces for the capacitor and MCU should be short and wide as much as physically possible.

Figure 31.9 Example of Pin Configuration

31.25.4 Register Access

Set registers ADCON0 (exclude bit 6), ADCON1, and ADCON2 when A/D conversion stops (before trigger is generated).
Set the ADSTBY bit which is 1 to 0 after A/D conversion stops.

31.25.5 A/D Conversion Start

If the ADSTBY bit in the ADCON1 is changed from 0 (A/D operation stopped) to 1 (A/D operation enabled), wait for 1 ϕA/D cycle or more before starting A/D conversion.

31.25.6 A/D Operation Mode Change

When A/D operation mode has been changed, re-select analog input pins by using bits CH2 to CH0 in the ADCON0 register or bits SCAN1 to SCAN0 in the ADCON1 register.

31.25.7 State When Forcibly Terminated

If A/D conversion in progress is halted by setting the ADST bit in the ADCON0 register to 0, the conversion result is undefined. In addition to that, the unconverted ADi register may also become undefined. Do not use any ADi registers when setting the ADST bit to 0 by a program during A/D conversion.

31.25.8 A/D Open-Circuit Detection Assist Function

The conversion result in open-circuit depends on the external circuit. Use this function only after careful evaluation for the system. Do not use this function when VCC1 > VCC2.

When A/D conversion starts after changing the AINRST register, follow these procedures:

(1) Change bits AINRST1 to AINRST0 in the AINRST register.
(2) Wait for one cycle of ϕAD.
(3) Set the ADST bit in the ADCON0 register to 1 (A/D conversion start).

31.25.9 Detection of Completion of A/D Conversion

In one-shot mode and single sweep mode, use the IR bit in the ADIC register to detect completion of A/D conversion. When not using interrupt, set the IR bit to 0 by a program after the detection.

When 1 is written to the ADST bit in the ADCON0 register, the ADST bit becomes 1 (A/D conversion start) after start processing time (refer to Table 27.7 “Cycles of A/D Conversion Item”) elapses. When reading the ADST bit shortly after writing 1, 0 (A/D conversion stop) may be read.

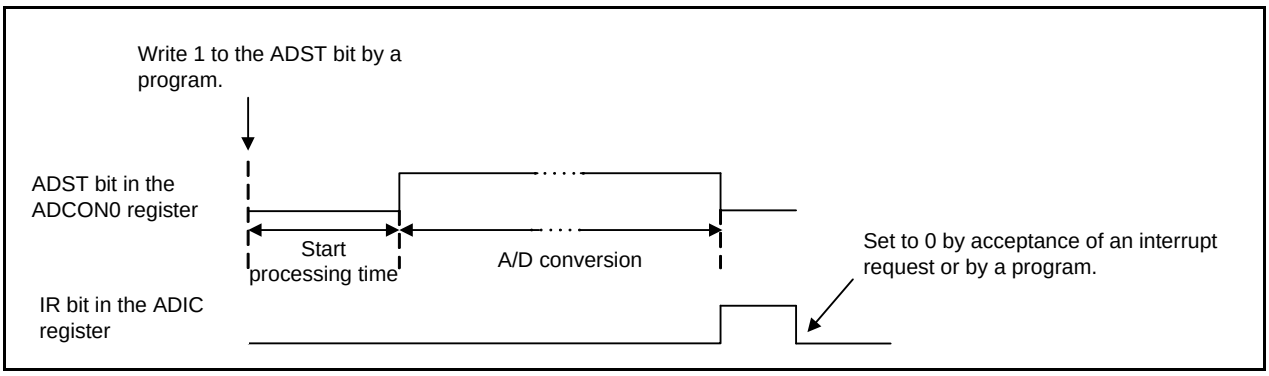


Figure 31.10 ADST Bit Operation

31.25.10 Register Settings

Set the CKS3 bit, and then set other A/D converter related registers. Also, after changing the CKS3 bit, set the A/D converter related registers again. Note that bits in the ADCON2 register and the CKS3 bit can be set simultaneously.

31.26 Notes on D/A Converter

31.26.1 Not Using D/A Converter

When the D/A converter is not used, set the DAiE bit (i = 0 to 1) to 0 (output disabled) and the DAi register to 00h in order to minimize unnecessary current consumption and prevent the flow of a current to R-2R resistor.

31.27 Notes on Flash Memory

Note

P1, P4_4 to P4_7, P7_2 to P7_5, P9_1 of the 80-pin package have no external connections. There are no P11 to P14 in the 80-pin and 100-pin packages. For the 80-pin and 100-pin packages, do not use these pins for the entry of user boot function.

31.27.1 Functions to Prevent Flash Memory from Being Rewritten

Addresses 0FFFDFh, 0FFFE3h, 0FFFEBh, 0FFFEFh, 0FFFF3h, 0FFFF7h, and 0FFFFBh store ID codes. When the wrong data is written to these addresses, the flash memory is prevented from being read or written in standard serial I/O mode.
0FFFFFh is OFS1 address. When the wrong data is written to this address, the flash memory is prevented from being read or written in parallel I/O mode.
These addresses correspond to the vector address (H) in fixed vector.

31.27.2 Reading of Data Flash

When 2.7 V ≤ VCC1 ≤ 3.0 V and f(BCLK) ≥ 16 MHz, or 3.0 V < VCC1 ≤ 5.5 V and f(BCLK) ≥ 20 MHz, one wait state is necessary to execute the program on the data flash and read the data. Use the PM17 in the PM1 register or FMR17 bit in the FMR1 register to set one wait state.

31.27.3 CPU Rewrite Mode

31.27.3.1 Operating Speed

Set a CPU clock frequency of 10 MHz or less by the CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register before entering CPU rewrite mode (EW0 or EW1 mode). Also, set the PM17 bit in the PM1 register to 1 (wait state).

31.27.3.2 Prohibited Instructions

Do not use the following instructions in EW0 mode:
UND instruction, INTO instruction, JMPS instruction, JSRS instruction, and BRK instruction.

31.27.3.3 Interrupts (EW0 Mode and EW1 Mode)

- Do not use an address match interrupt during command execution because the address match interrupt vector is located in ROM.
- Do not use a non-maskable interrupt during block 0 erasure because fixed vector is located in block 0.

31.27.3.4 Rewrite (EW0 Mode)

If the power supply voltage drops while rewriting the block where the rewrite control program is stored, the rewrite control program is not correctly rewritten. This may prevent the flash memory from being rewritten. If this error occurs, use standard serial I/O mode or parallel I/O mode for rewriting.

31.27.3.5 Rewrite (EW1 Mode)

Do not rewrite any blocks in which the rewrite control program is stored.

31.27.3.6 DMA transfer

In EW1 mode, do not generate a DMA transfer while the FMR00 bit in the FMR0 register is set to 0 (auto programming or auto erasing).

31.27.3.7 Wait Mode

To enter wait mode, set the FMR01 bit to 0 (CPU rewrite mode disabled) before executing the WAIT instruction.

31.27.3.8 Stop Mode

To enter stop mode, set the FMR01 bit to 0 (CPU rewrite mode disabled), and then disable DMA transfer before setting the CM10 bit to 1 (stop mode).

31.27.3.9 Low Power Mode and On-Chip Oscillator Low Power Mode

When the CM05 bit is set to 1 (main clock stopped), do not execute the following commands:

- Program
- Block erase
- Lock bit program
- Read lock bit status
- Block blank check

31.27.3.10 PM13 Bit

The PM13 bit in the PM1 register becomes 1 while the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled). The PM13 bit returns to the former value by setting the FMR01 bit to 0 (CPU rewrite mode disabled). When the PM13 bit is changed during CPU rewrite mode, the value of the PM13 bit after being changed is not reflected until the FMR01 bit is set to 0.

31.27.3.11 Area Where Rewrite Control Program is Executed

Bits PM10 and PM13 in the PM1 register become 1 in CPU rewrite mode. Execute the rewrite program in internal RAM or an external area which can be used when both bits PM10 and PM13 are 1. Do not use the area (40000h to BFFFFh) where accessible space is expanded when the PM13 bit is 0 and 4-Mbyte mode is set.

31.27.3.12 Program and Erase Cycles and Execution Time

Execution time of program, block erase and lock bit program command becomes longer as the number of programming and erasing increases.

31.27.3.13 Suspend of Auto-Erase Operation and Auto-Program Operation

When program, block erase, and lock bit program commands are suspended, the blocks for those commands must be erased. Execute program and lock bit program commands again after erasing. Those commands are suspended by the following reset or interrupts:

- Reset
- $\overline{\text{NMI}}$, watchdog timer, oscillation stop/re-oscillation detection, voltage monitor 1, and voltage monitor 2 interrupts.

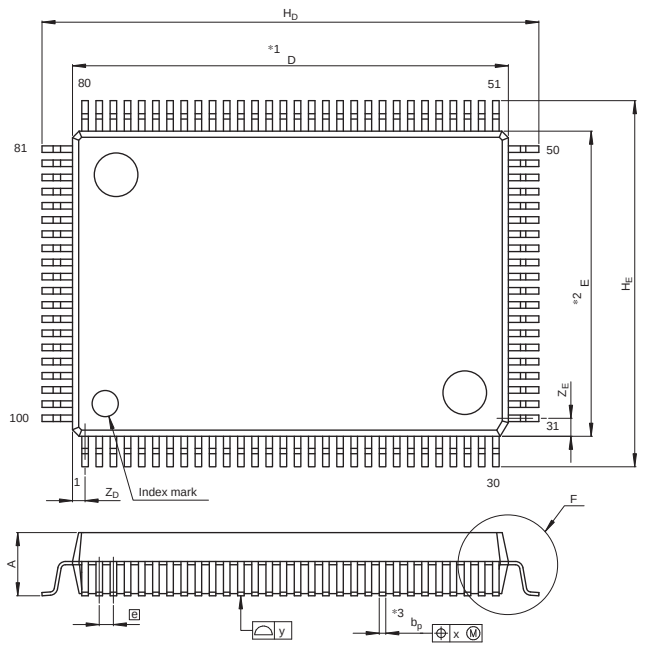
31.27.4 Standard Serial I/O Mode

31.27.4.1 User Boot Mode

To use user boot mode after standard serial I/O mode, turn off the power when exiting standard serial I/O mode, and then turn on the power again (cold start). The MCU enters user boot mode under the right conditions.

Appendix 1. Package Dimensions

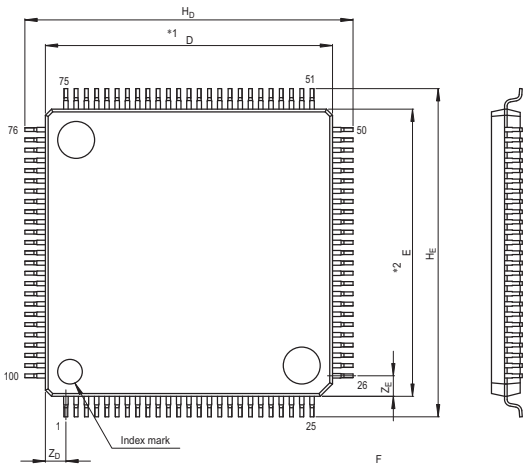
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JD-B	100P6F-A	1.8g



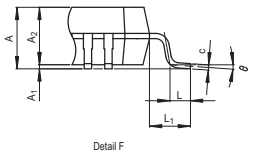
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



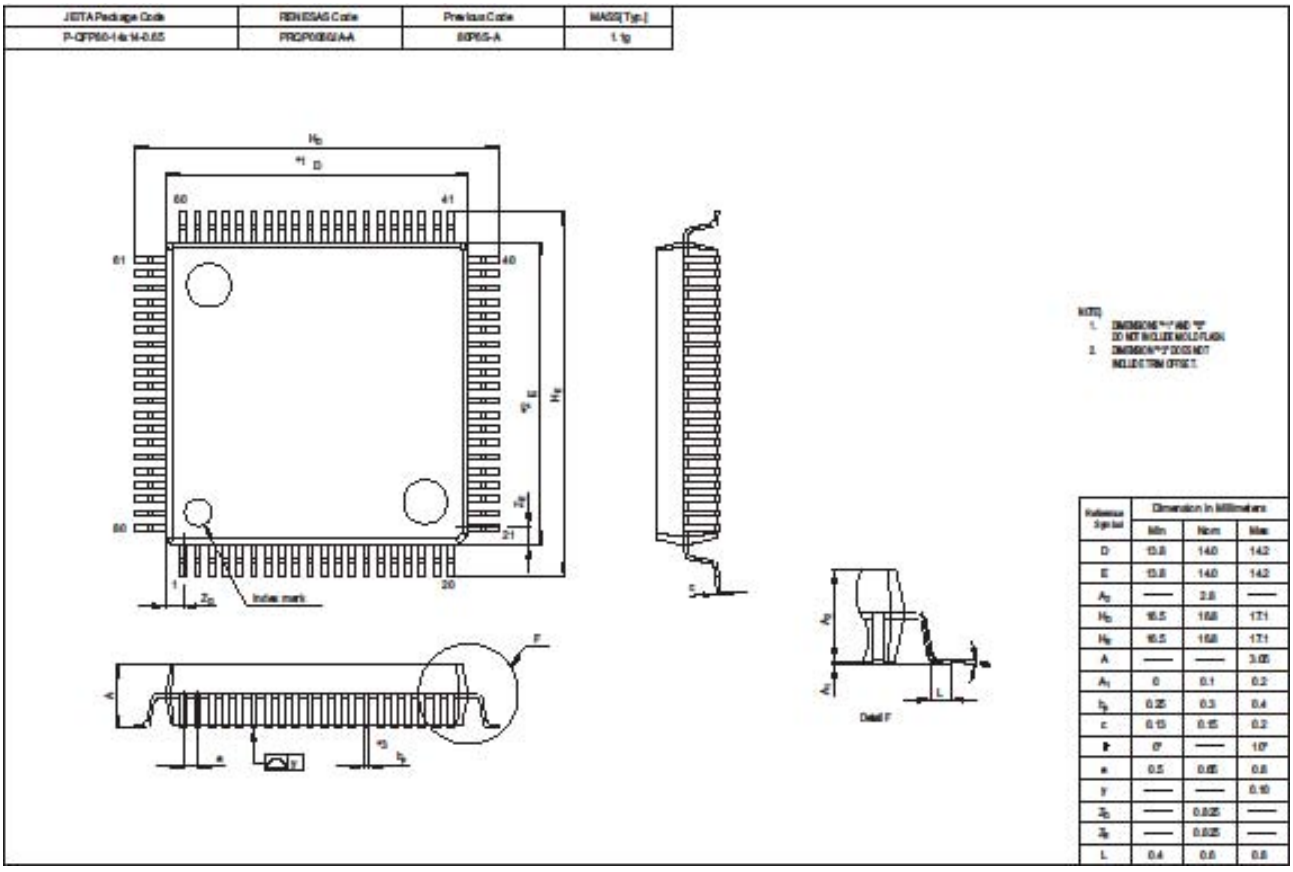
Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—



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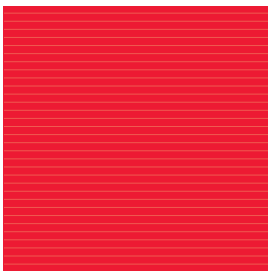

Renesas Technology Corp.
2-6-2, Ote-machi, Chiyoda-ku, Tokyo, 100-0004, Japan